

Preface

Aggressive scaling of CMOS technology in sub-90 nm nodes has created huge challenges for SRAM design. Variations due to fundamental physical limits, subwavelength lithography, and device aging are increasing significantly with technology scaling. In addition, SRAMs typically use the smallest devices in a technology, which make them suffer from the largest variations. Moreover, in recent technologies, there is a high demand to integrate large embedded memories in microprocessors and SoCs, and memory yield has huge impact on the chip cost.

The increase of variations with technology scaling decreases the robustness of SRAM, as a result, memory yield decreases, and the memory minimum supply voltage (V_{\min}) is becoming the limiting factor of voltage scaling in newer technologies. In this book, we offer a comprehensive overview of variation-tolerant techniques used to mitigate the negative impacts of variations, and improve memory robustness. The topic spans a wide area between device technology, custom circuits, statistical CAD, and architecture. This book presents state-of-the-art research in the areas of variability, variation-tolerant SRAM circuits, and assist techniques, statistical design, and SRAM silicon characterization. This book is intended for graduate students, researchers as well as practicing engineers interested in understanding the key challenges facing SRAM design in nanometer technologies, and the techniques used to address them.

San Diego, CA, USA, May 2012
Cairo, Egypt, May 2012

Mohamed H. Abu-Rahma
Mohab Anis

Nanometer Variation-Tolerant SRAM
Circuits and Statistical Design for Yield

Abu Rahma, M.; Anis, M.

2013, XVI, 172 p., Hardcover

ISBN: 978-1-4614-1748-4