

# Preface

The UTLEON3 processor has been derived from the LEON3 processor distributed in the GRLIB package by Aeroflex-Gaisler. The main motivation for this work was the evaluation of the performance and hardware cost of the microthreaded computing model in a single core as the first step to designing novel multi-core systems with better scaling properties. The time we spent researching this topic with our colleagues from the Apple-CORE project belongs to the most inspiring and productive periods in our lives as the project created a rare opportunity for interaction between the ‘software’ and ‘hardware’ people.

This book presents the design, implementation and evaluation of instruction set extensions for fine-grain multithreading implemented in UTLEON3. The first part of the book defines new processor instructions for thread management in a way compatible with the existing SPARC V8 opcodes, proposes the necessary hardware extensions to LEON3 and describes them on a functional level.

The second part describes implementation details of the implemented architectural extensions that are required to execute microthreads both in the processor pipeline and in specialized hardware accelerators. We have tried to describe the structure of the new blocks in a way that would provide guidance to the actual VHDL sources of the blocks without going into unnecessary details.

The description is accompanied with an analysis of performance gains; these were evaluated by comparing the cycle count of microthreaded assembler programs, executed on UTLEON3 in the microthreaded mode, to reference legacy assembler programs, coded using the standard SPARC V8 instructions and executed on LEON3 and UTLEON3 in the legacy mode.

The main text is supplemented with appendices that provide additional information on LEON3 together with a scheduling example and resource requirements for UTLEON3. As the book is released in parallel with the UTLEON3 sources, a tutorial is also provided that gives instructions on the basic set-up of the VHDL package with the UTLEON3 sources.

We hope you will enjoy the book and UTLEON3.

Praha, Czech Republic

Martin Daněk  
Leoš Kafka  
Lukáš Kohout  
Jaroslav Sýkora  
Roman Bartosiński

UTLEON3: Exploring Fine-Grain Multi-Threading in FPGAs

Daněk, M.; Kafka, L.; Kohout, L.; Sýkora, J.; Bartosiński,  
R.

2013, XVIII, 222 p., Hardcover

ISBN: 978-1-4614-2409-3