

Preface

Dear Friends,

In today's world of deep submicron, Timing has become a critical challenge for designers developing Application Specific Integrated Circuits (ASIC) or System on a chip (SoC). Design engineers spend many cycles iterating between different stages of the design flow to meet the timing requirements. Timing is not merely a response time of a chip, but an integral part of the chip functionality that ensures that it can communicate with other components on a system seamlessly. That begs the question, what is timing? How do you specify it?

This book serves as a hands-on guide to writing and understanding timing constraints in integrated circuit design. Readers will learn to write their constraints effectively and correctly, in order to achieve the desired performance of their IC or FPGA designs, including considerations around reuse of the constraints. Coverage includes key aspects of the design flow impacted by timing constraints, including synthesis, static timing analysis, and placement and routing. Concepts needed for specifying timing requirements are explained in detail and then applied to specific stages in the design flow, all within the context of Synopsys Design Constraints (SDC), the industry-leading format for specifying constraints.

We have often heard from many design engineers that there are several books explaining concepts like Synthesis and Static Timing Analysis which do cover timing constraints, but never in detail. This book is our attempt at explaining the concepts needed for specifying timing requirements based on many years of work in the areas of timing characterization, delay calculation, timing analysis, and constraints creation and verification.

Book Organization

Here's how the book is laid out:

Chapters 1, 2, and 3 introduce the subject of Timing Analysis – including its need in the context of design cycle. The descriptions in these chapters are vendor, language, and format-independent.

Chapter 4 provides an overview of the Tcl language, because SDC (Synopsys Design Constraints) acts as an extension to Tcl. The concept of SDC is also introduced in this chapter.

These first four chapters might be thought of as Introduction section.

Chapters 5 through 8 together form a section which talks about clocks, explaining how to apply clock-related constraints. These chapters explain various kinds of clocks and their relationships and how to specify those in SDC.

Chapters 9 and 10 explain how to apply constraints on the remaining (non-clock) ports. With this section, all the primary ports are covered.

Chapters 11, 12, and 13 explain the need for timing exceptions. These chapters then go on to explain how to specify the exceptions correctly in SDC.

Chapters 14 and 15 deal with much more specialized topics. These concepts are less about individual constraints. Rather they delve into how design teams manage the world of constraints as they move across the flow, from front-end to back-end, partitioning the complete design to blocks and when integrating individual blocks.

In Chap. 16, we explain some other commands of SDC, which might have an impact on Timing Analysis.

Some of the commands are still not covered in this book. However, with the fundamental understanding gained on Timing Analysis and SDC through these chapters, it should be possible for a user to easily comprehend any remaining commands, including any extensions that might come in future versions of SDC.

Most tools which support SDC typically also allow some extensions to SDC in order to achieve higher accuracy or better ease of use for the specific tool. Chapter 17 provides an overview of the Xilinx extensions to the SDC timing constraints – for their product Vivado™.

Conventions Used in This Book

In general, the names of SDC keywords and its options are printed in *italics*. *Italics* are also used to represent words that have a special meaning as it relates to this book.

Additional Resources

SDC is an open source format distributed by Synopsys, Inc. SDC Documentation and parsers can be downloaded for free from Synopsys website.

Feedback

We have put in our best efforts to provide an accurate description of the concepts. We also got help from some experts in the industry to review the material for accuracy. However, if you find some descriptions confusing or erroneous, please let us know.

Happy Reading!

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