

Contents

1	Introduction	1
1.1	ASIC Design Flow	1
1.2	FPGA Design Flow	4
1.3	Timing Constraints in ASIC and FPGA Flow	7
1.4	Timing Constraint Issues in Nanometer Design	7
1.5	Conclusion	8
2	Synthesis Basics	9
2.1	Synthesis Explained	9
2.2	Role of Timing Constraints in Synthesis	10
2.2.1	Optimization	10
2.2.2	Input Reordering	11
2.2.3	Input Buffering	12
2.2.4	Output Buffering	12
2.3	Commonly Faced Issues During Synthesis	13
2.3.1	Design Partitioning	13
2.3.2	Updating Constraints	14
2.3.3	Multi-clock Designs	14
2.4	Conclusion	15
3	Timing Analysis and Constraints	17
3.1	Static Timing Analysis	17
3.2	Role of Timing Constraints in STA	19
3.2.1	Constraints as Statements	19
3.2.2	Constraints as Assertions	20
3.2.3	Constraints as Directives	20
3.2.4	Constraints as Exceptions	21
3.2.5	Changing Role of Constraints	21
3.3	Common Issues in STA	22
3.3.1	No Functionality Check	22
3.3.2	No Check on Statements	22

3.3.3	Requirements to be Just Right	23
3.3.4	Common Errors in Constraints	24
3.3.5	Characteristics of Good Constraints	24
3.4	Delay Calculation Versus STA.....	26
3.5	Timing Paths	26
3.5.1	Start and End Points.....	26
3.5.2	Path Breaking.....	28
3.5.3	Functional Versus Timing Paths.....	28
3.5.4	Clock and Data Paths	29
3.6	Setup and Hold.....	29
3.6.1	Setup Analysis.....	29
3.6.2	Hold Analysis.....	30
3.6.3	Other Analysis	30
3.7	Slack.....	31
3.8	On-Chip Variation.....	32
3.9	Conclusion	33
4	SDC Extensions Through Tcl	35
4.1	History of Timing Constraints	35
4.2	Tcl Basics.....	36
4.2.1	Tcl Variables	37
4.2.2	Tcl Lists	38
4.2.3	Tcl Expression and Operators.....	38
4.2.4	Tcl Control Flow Statements	38
4.2.5	Miscellaneous Tcl Commands.....	41
4.3	SDC Overview	41
4.3.1	Constraints for Timing	42
4.3.2	Constraints for Area and Power.....	42
4.3.3	Constraints for Design Rules	42
4.3.4	Constraints for Interfaces.....	43
4.3.5	Constraints for Specific Modes and Configurations	43
4.3.6	Exceptions to Design Constraints	43
4.3.7	Miscellaneous Commands	44
4.4	Design Query in SDC	44
4.5	SDC as a Standard	44
4.6	Conclusion	46
5	Clocks.....	47
5.1	Clock Period and Frequency.....	47
5.2	Clock Edge and Duty Cycle.....	48
5.3	create_clock	50
5.3.1	Specifying Clock Period	50
5.3.2	Identifying the Clock Source	50
5.3.3	Naming the Clock	51
5.3.4	Specifying the Duty Cycle	51
5.3.5	More than One Clock on the Same Source.....	52
5.3.6	Commenting the Clocks.....	53

5.4	Virtual Clocks	54
5.5	Other Clock Characteristics	54
5.6	Importance of Clock Specification.....	54
5.7	Conclusion	55
6	Generated Clocks	57
6.1	Clock Divider	57
6.2	Clock Multiplier.....	58
6.3	Clock Gating	58
6.4	create_generated_clock.....	60
6.4.1	Defining the Generated Clock Object.....	60
6.4.2	Defining the Source of Generated Clock	60
6.4.3	Naming the Clock	61
6.4.4	Specifying the Generated Clock Characteristic	61
6.4.5	Shifting the Edges	65
6.4.6	More than One Clock on the Same Source.....	66
6.4.7	Enabling Combinational Path	67
6.5	Generated Clock Gotchas	68
6.6	Conclusion	68
7	Clock Groups.....	71
7.1	Setup and Hold Timing Check.....	71
7.1.1	Fast to Slow Clocks.....	73
7.1.2	Slow to Fast Clocks.....	74
7.1.3	Multiple Clocks Where Periods Synchronize in More than Two Cycles	74
7.1.4	Asynchronous Clocks	75
7.2	Logically and Physically Exclusive Clocks	75
7.3	Crosstalk	76
7.4	set_clock_group	78
7.5	Clock Group Gotchas.....	80
7.6	Conclusion	80
8	Other Clock Characteristics	81
8.1	Transition Time	81
8.2	set_clock_transition	82
8.3	Skew and Jitter	83
8.4	set_clock_uncertainty	84
8.4.1	Intraclock Uncertainty	84
8.4.2	Interlock Uncertainty	85
8.5	Clock Latency	87
8.6	set_clock_latency	88
8.7	Clock Path Unateness	90
8.8	set_clock_sense.....	91
8.9	Ideal Network.....	93
8.10	Conclusion	94

9	Port Delays	95
9.1	Input Availability	95
9.1.1	Min and Max Availability Time	96
9.1.2	Multiple Clocks	97
9.1.3	Understanding Input Arrival Time	97
9.2	Output Requirement	98
9.2.1	Min and Max Required Time	99
9.2.2	Multiple Reference Events	100
9.2.3	Understanding Output Required Time	100
9.3	set_input_delay	101
9.3.1	Clock Specification	102
9.3.2	-level_sensitive	103
9.3.3	Rise/Fall Qualifiers	103
9.3.4	Min/Max Qualifiers	103
9.3.5	-add_delay	104
9.3.6	Clock Latency	105
9.3.7	Completing Input Delay Constraints	106
9.4	set_output_delay	106
9.4.1	Clock Specification	107
9.4.2	-level_sensitive	107
9.4.3	Rise/Fall Qualifiers	107
9.4.4	Min/Max Qualifiers	107
9.4.5	-add_delay	108
9.4.6	Clock Latency	108
9.4.7	Completing Output Delay Constraints	108
9.5	Relationship Among Input and Output Delay	108
9.6	Example Timing Analysis	110
9.6.1	Input Delay: Max	110
9.6.2	Input Delay: Min	111
9.6.3	Output Delay: Max	112
9.6.4	Output Delay: Min	113
9.7	Negative Delays	114
9.8	Conclusion	114
10	Completing Port Constraints	117
10.1	Drive Strength	117
10.1.1	set_drive	118
10.2	Driving Cell	119
10.2.1	set_driving_cell	120
10.3	Input Transition	125
10.3.1	Input Transition Versus Clock Transition	125
10.4	Fanout Number	126
10.5	Fanout Load	126
10.6	Load	127
10.6.1	Net Capacitance	127
10.6.2	Pin Load Adjustments	128

10.6.3	Load Type	128
10.6.4	Load Versus Fanout Load	129
10.6.5	Load at Input	129
10.7	Conclusion	129
11	False Paths	131
11.1	Introduction	131
11.2	set_false_path	131
11.3	Path Specification	132
11.4	Transition Specification	135
11.5	Setup/Hold Specification	137
11.6	Types of False Paths	137
11.6.1	Combinational False Path	137
11.6.2	Sequential False Path	138
11.6.3	Dynamically Sensitized False Path	139
11.6.4	Timing False Path	139
11.6.5	False Path Due to Bus Protocol	140
11.6.6	False Path Between Virtual and Real Clocks	141
11.7	set_disable_timing	142
11.8	False Path Gotchas	143
11.9	Conclusion	144
12	Multi Cycle Paths	145
12.1	SDC Command for Multi Cycle Paths	145
12.2	Path and Transition Specification	146
12.3	Setup/Hold Specification	147
12.4	Shift Amount	148
12.5	Example Multi Cycle Specification	151
12.5.1	FSM-Based Data Transfer	151
12.5.2	Source Synchronous Interface	152
12.5.3	Reset	154
12.5.4	Asynchronous Clocks	154
12.5.5	Large Data Path Macros	154
12.5.6	Multimode	155
12.6	Conclusion	155
13	Combinational Paths	157
13.1	set_max_delay	157
13.2	set_min_delay	158
13.3	Input/Output Delay	158
13.3.1	Constraining with Unrelated Clock	159
13.3.2	Constraining with Virtual Clock	159
13.3.3	Constraining with Related Clock	160
13.4	Min/Max Delay Versus Input/Output Delay	161
13.5	Feedthroughs	162
13.5.1	Feedthroughs Constrained Imperfectly	164

13.6	Point-to-Point Exception.....	164
13.7	Path Breaking.....	165
13.8	Conclusion	166
14	Modal Analysis.....	167
14.1	Usage Modes.....	167
14.2	Multiple Modes.....	167
14.3	Single Mode Versus Merged Mode.....	169
14.4	Setting Mode.....	169
14.5	Other Constraints	172
14.6	Mode Analysis Challenges	172
14.6.1	Timing Closure Iterations	172
14.6.2	Missed Timing Paths.....	173
14.7	Conflicting Modes.....	173
14.8	Mode Names	175
14.9	Conclusion	175
15	Managing Your Constraints	177
15.1	Top-Down Methodology	177
15.2	Bottom-Up Methodology	178
15.3	Bottom-Up Top-Down (Hybrid) Methodology.....	181
15.4	Multimode Merge	183
15.4.1	Picking Pessimistic Clock.....	185
15.4.2	Mutually Exclusive Clocks	185
15.4.3	Partially Exclusive Clocks	186
15.4.4	Merging Functional and Test Mode.....	188
15.4.5	Merging I/O Delays for Same Clock	189
15.4.6	Merging I/O Delays with Different Clocks.....	189
15.5	Challenges in Managing the Constraints	190
15.6	Conclusion	192
16	Miscellaneous SDC Commands.....	193
16.1	Operating Condition.....	193
16.1.1	Multiple Analysis Conditions	195
16.1.2	set_operating_conditions	195
16.1.3	Derating.....	196
16.2	Units.....	197
16.3	Hierarchy Separator	198
16.3.1	set_hierarchy_separator	198
16.3.2	-hsc	199
16.4	Scope of Design	200
16.4.1	current_instance	200
16.5	Wire Load Models	201
16.5.1	Minimal Size for Wire Load	202
16.5.2	Wire Load Mode	202
16.5.3	Wire Load Selection Group	203

16.6	Area Constraints.....	204
16.7	Power Constraints	205
16.7.1	Voltage Island.....	205
16.7.2	Level Shifters	206
16.7.3	Power Targets.....	207
16.8	Conclusion	207
17	XDC: Xilinx Extensions to SDC	209
17.1	Clocks	209
17.1.1	Primary and Virtual Clocks.....	210
17.1.2	Generated Clocks	210
17.1.3	Querying Clocks	212
17.1.4	Clock Groups	213
17.1.5	Propagated Clocks and Latency	214
17.1.6	Clock Uncertainty	215
17.2	Timing Exceptions	216
17.3	Placement Constraints.....	217
17.4	SDC Integration in Xilinx Tcl Shell	218
17.5	Conclusion	218
	Bibliography	219
	Index.....	221

Constraining Designs for Synthesis and Timing Analysis
A Practical Guide to Synopsys Design Constraints (SDC)

Gangadharan, S.; Churiwala, S.

2013, XXVII, 226 p., Hardcover

ISBN: 978-1-4614-3268-5