

Chapter 2

Data Acquisition Systems: Hardware

Abstract This chapter describes different hardware aspects of the data acquisition systems, in particular the main components such as signal conditioning, analog-to-digital converter, and so on. Moreover, different techniques of interface between analog and digital signals to plug-in boards will be discussed.

2.1 Introduction

Capabilities and the accuracy of data acquisition (DAQ) systems can be founded from analog input specifications. Basic specifications is as follows: number of channels, sampling rate, resolution, and input range. The number of analog channel inputs will be indicated for both single-ended and differential inputs.

The most common way used to transmit electrical signals over wires is the form single-ended. In general, one wire carries a voltage (the signal), while the other wire is connected to a reference voltage (ground). Instead, differential signal is a method of transmission of electrical signals with two complementary signals sent on a couple of wires.

The main advantage of single-ended over differential signaling is that fewer wires are needed to transmit multiple signals. A disadvantage of single-ended signaling is that the return currents for all the signals can be shared with the same conductor, and this can sometimes cause interference (“crosstalk”) between the signals.

Differential signaling technique can be used for the following applications [5, 6]:

- Balanced audio
- Digital signaling
- RS 422, RS 485, PCI express and USB
- Printed circuit board
- Connectors (BNC)

2.2 Plug-in DAQ Systems

Many DAQ systems, known as plug-in boards, are used in scientific application to acquire data and transfer it directly to computer memory. Transference of data can be done by parallel port, serial port, USB port, Ethernet port, and so on [1, 3].

Typically, DAQ plug-in boards (Fig. 2.1) are general-purpose DAQ instruments that are well suited for measuring voltage or current signals or resistance that can include some form of signal conditioning [1].

Usually, application in real time of high frequency analog signals needs a high speed DAQ with a dedicated plug-in processor such as a digital signal processing (DSP) board.

The main components of DAQ system is the analog input (A/D) boards; it converts (Figs. 2.2 and 2.3) analog voltages from external signal sources (sensor, see Chap. 1) into a digital signal, which can be read by the host computer. Moreover, the functional diagram of a typical DAQ system can be described of the following main components:

- Input multiplexer
- Input signal amplifier
- Sample and hold circuit

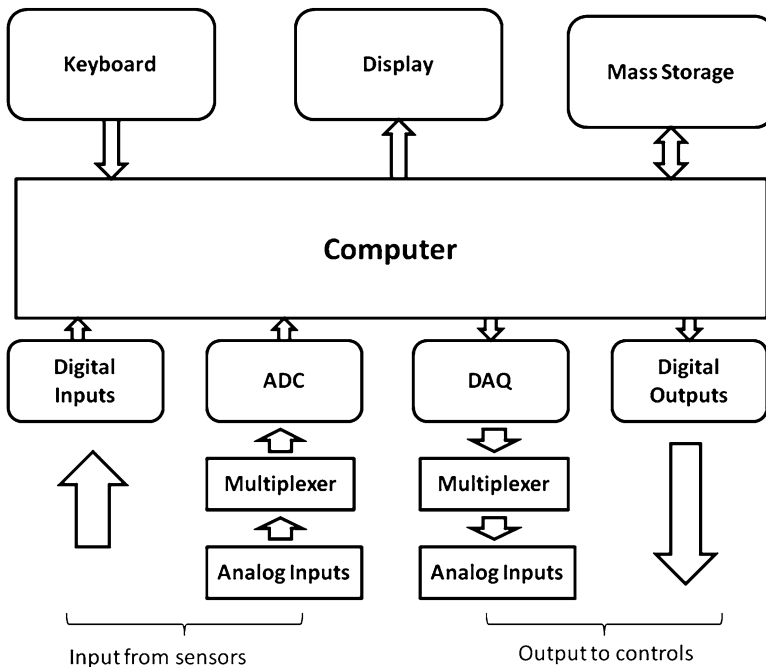


Fig. 2.1 Functional diagram of a basic data acquisition system

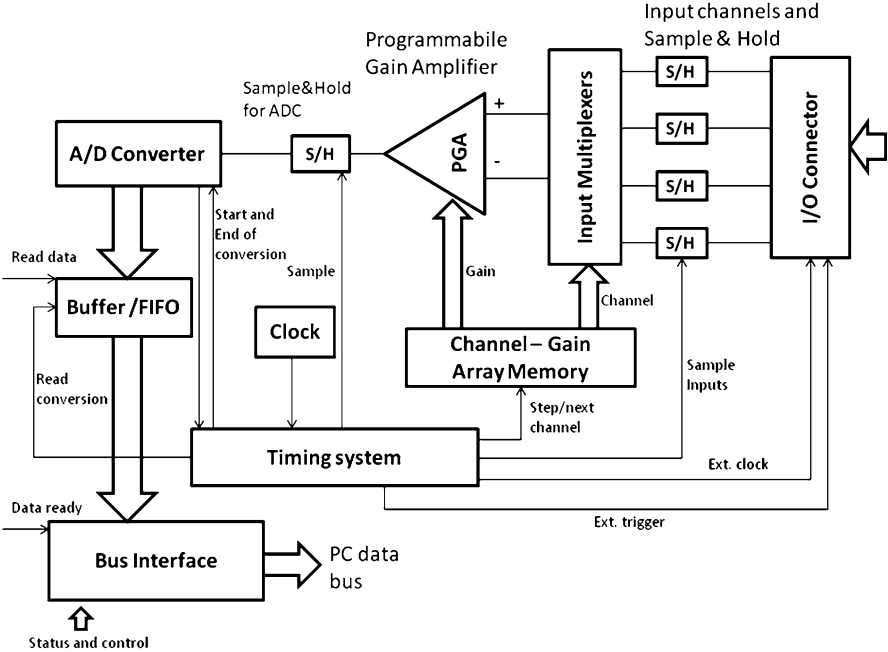


Fig. 2.2 Functional diagram of a generic A/D board

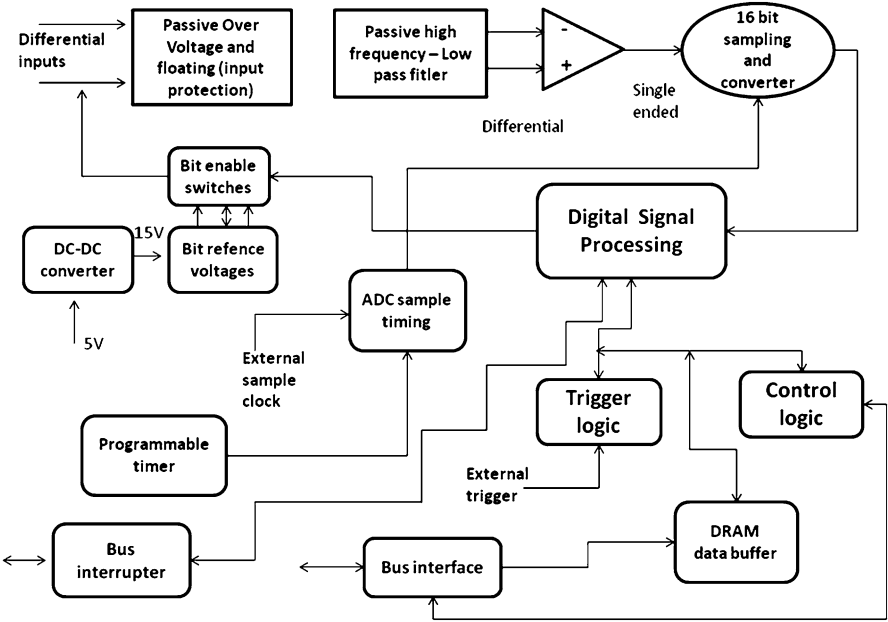


Fig. 2.3 Functional diagram of a typical DAQ system

- A/D converter
- Memory (DMA)
- Timing system and filtering
- Bus interface
- Digital signal processing
- Microprocessor and/or Field-Programmable Gate Array

The performance of DAQ system can be affected from data transfer capacity of the board. Usually, all PCs are capable to program I/O and interrupt transfers.

Computers that have DMA channels can transfer data using much less CPU laden than those which without a DMA channel.

Without DMA, CPU is typically occupied for the entire duration of the read or write operation, and is thus unavailable to perform other work. With DMA, the CPU initiates the transfer, executes other operations while the transfer is in progress, and receives an interrupt from the DMA controller when the operation is done. This feature is useful when the CPU cannot keep up with the rate of data transfer, or where the CPU needs to perform useful work while waiting for a relatively slow I/O data transfer. Many hardware systems use DMA, as for example disk drive controllers, graphics cards, network cards, and sound cards [1, 5, 6].

2.3 Signal Conditioning

The first operation in DAQ system is the conditioning of signal. The signal from the sensor must firstly be sent to electronic system to transform the increasing or decreasing level of amplitude [4]. However, in order to be useful to the interface devices, the signal can be sent in some forms of conditioning. In general, all interface devices are designed to allow interfacing of sensing signals in a voltage range from 0 to 5 V that will be digitized from A/D converter. In general, conditioning devices are designed to be flexible in order to change this range.

The process of conditioning involves a combination of more simple processes that can be used in all types of signals: converting a resistance to a voltage, dividing, amplifying and shifting a voltage.

Regardless of the types of sensors or transducers, the proper signal conditioning equipment can improve the quality and performance of your system. In signal conditioning circuitry with amplification (Fig. 2.4) an amplifier, located on the DAQ board or in external device, applies a gain to the small sensing signal before to be sent it in analog-to-digital converters (ADCs). If ADCs require a positive voltage and the sensors produce output voltage as $-X$ to $+X$, it is necessary to shift the voltage from, for example, 0 to $2X$ Volts.

The circuit for shifting voltage is more complex than circuit in Fig. 2.4. It uses a dual op-amp to add a fixed voltage to the input signal (Fig. 2.5).

Moreover, you can use filters to reject unwanted noise within a certain frequency range. Most common cause of damaged DAQ or problems about measurement is

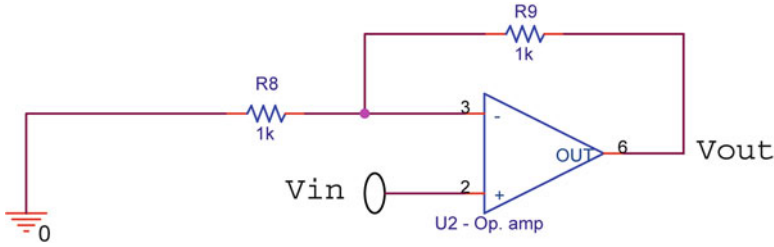


Fig. 2.4 Signal conditioning: amplification

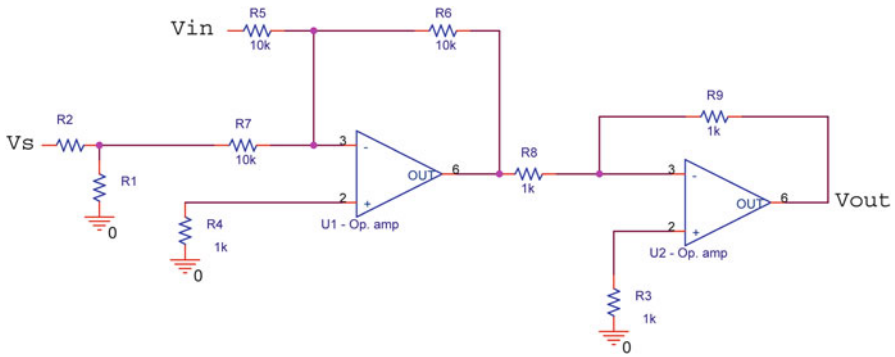


Fig. 2.5 Signal conditioning: shifting voltage

improper grounding of the DAQ system. In order to avoid that, it is necessary to isolate signal conditioners and prevent most of these problems [1, 2, 6, 7].

2.3.1 Example of Design of a Signal Conditioning Circuit

First of all, we must determine input signal range [4]. In this example of design, RTD sensor (resistive Temperature Detector) in Wheatstone bridge configuration will be used as our input signal. The goal of this circuit is to measure temperature in range 0–70°C, and our input will be the potential difference between Node A and Node B.

Resistance of RTD varies from 100Ω to 127Ω which represents 0 to 70°C temperature range. Voltage difference varies from 0 V to 91.94 mV, in steps of 3.74 mV per 1Ω increase (Fig. 2.6).

Next step is to design a circuit that can detect output potential difference between node A and node B. INA333 (instrumentation amplifier) will be implemented for such purpose. INA333 is a type of differential amplifier that does not require input impedance matching through two input buffers. From DC analysis the maximum voltage difference between two nodes is 91.94 mV, so in order to increase resolution

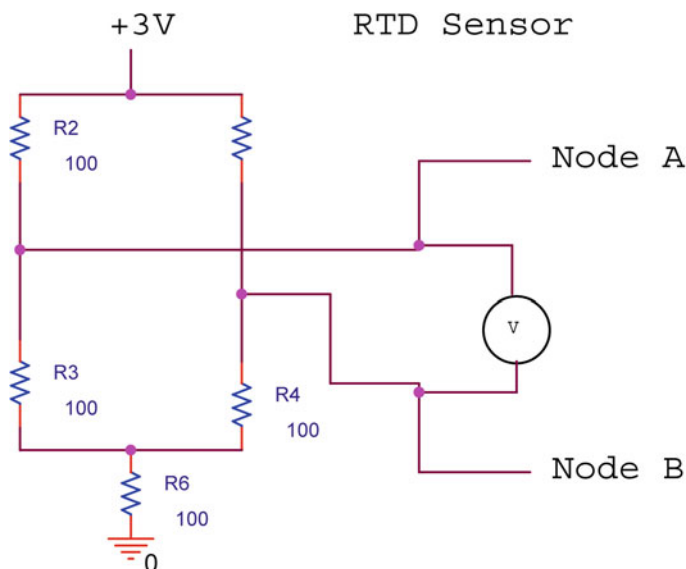


Fig. 2.6 Signal conditioning: PT1206

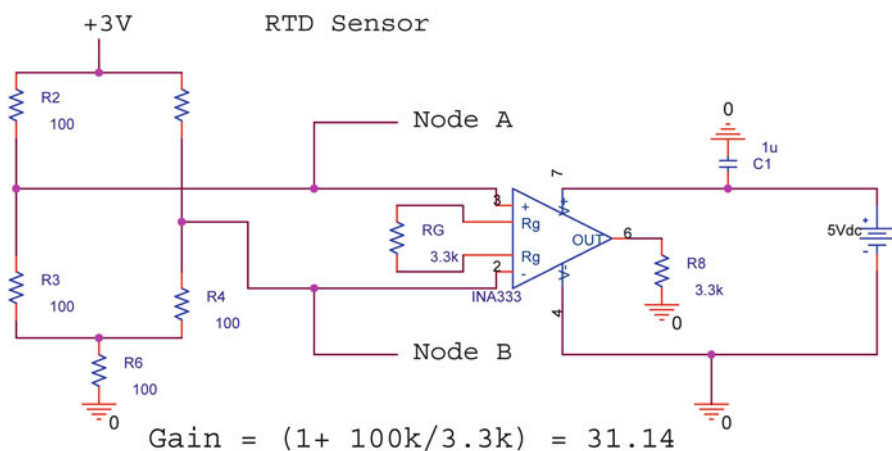


Fig. 2.7 Signal conditioning: amplification

and signal-to-noise-ratio (SNR), we design the amplification circuit with gain of approximately 30; in this way it matches (for example) with reference voltage of ADC in use (Fig. 2.7). After amplification stage of signal conditioning, signal must be filtered and optimized. The design of RC filter is determined by following four parameters of ADC: acquisition time, sampling ADC input capacitance, time constant multiplier, and full-scale input voltage range (Fig. 2.8).

Capacitance is set to be at least bigger than 20 times of ADC input capacitance.

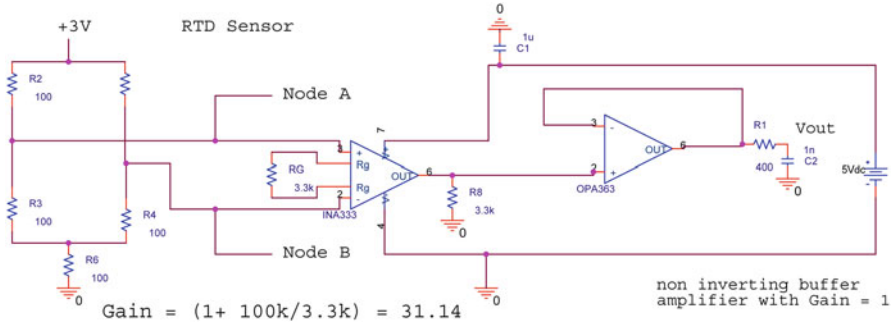


Fig. 2.8 Signal conditioning: filtering

Using a capacitor with capacitance of 1 nF with other parameter, equivalent external resistance has to be at least larger than 398 ohms, which appropriate buffer amplifier needs to be chosen. OPA363 from TI can be ideal as buffer amplifier due to the low common mode rejection ratio (CMRR) and optimized to be used as a driver for ADC input capacitance (Fig. 2.7) [3,4,6,7].

2.4 Converters A/D

The connection of digital circuit to sensing device can be done only if the sensors are inherently digital themselves. However, when analog signals are involved in the project, the interface becomes much more complex. In this case, it needs a way to translate analog signals into digital form: an ADC; digital-to-analog converter or DAC performs the opposite operation.

Typically, an ADC (Figs. 2.9 and 2.10) is an electronic device that converts an input analog voltage or current to a digital number proportional to the magnitude of the voltage or current. However, some non-electronic or only partially electronic devices, such as rotary encoders, can also be considered ADCs. The number of output bits from an ADC doesn't fully specify its behavior. Real A/D converters can differ from ideal behavior in many ways. While static imperfections, such as gain and offset, are easy to quantify, the success of many signal-processing applications depends on the dynamic behavior of the A/D converter. Ultimately, the application determines the requirements, and A/D converter resolution may not be either necessary or sufficient to specify the required performance. In many cases, the quality of the A/D converter must be tested for the specific application. The wide variety of ADC applications leads to a large number of figures of merit for specifying performance. These figures of merit include accuracy, resolution, dynamic range, offset, gain, differential nonlinearity, integral nonlinearity, signal-to-noise ratio, signal-to-noise-and-distortion ratio, effective number of bits, spurious-free dynamic range, intermodulation distortion, total harmonic distortion, effective resolution bandwidth, full-power bandwidth, full-linear bandwidth, aperture delay,

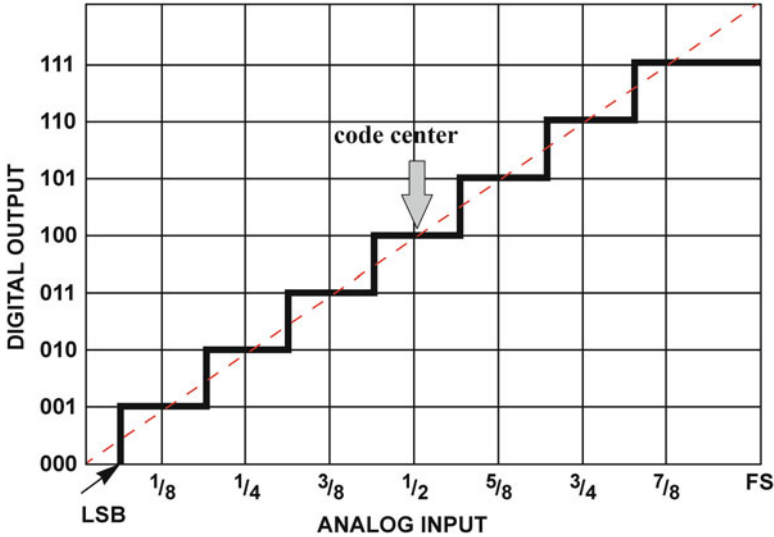


Fig. 2.9 Ideal characteristic of analog to digital converter

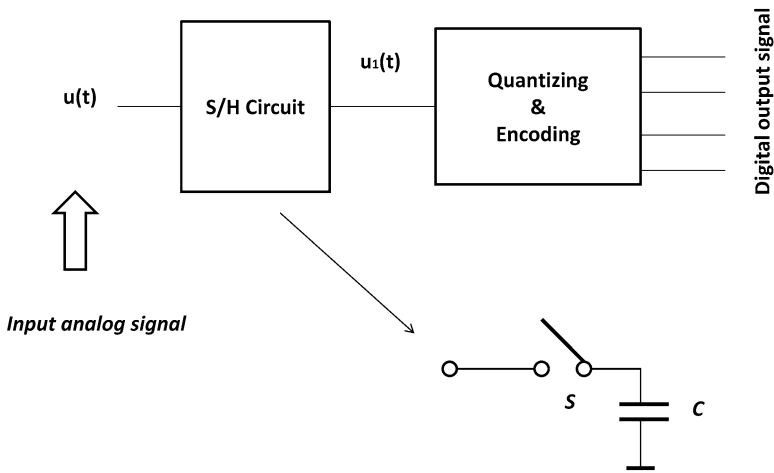


Fig. 2.10 Outline of analog to digital converter

aperture jitter, transient response, and over voltage recovery. Most converters sample with 6–24 bits of resolution, and produce fewer than 1 Mega samples per second. Thermal noise generated by passive components such as resistors masks the measurement when higher resolution is desired.

All ADCs suffer from nonlinearity errors caused by their physical imperfections, permitting their output to deviate from a linear function (or some other function, in the case of a deliberately nonlinear ADC) of their input. These errors can sometimes

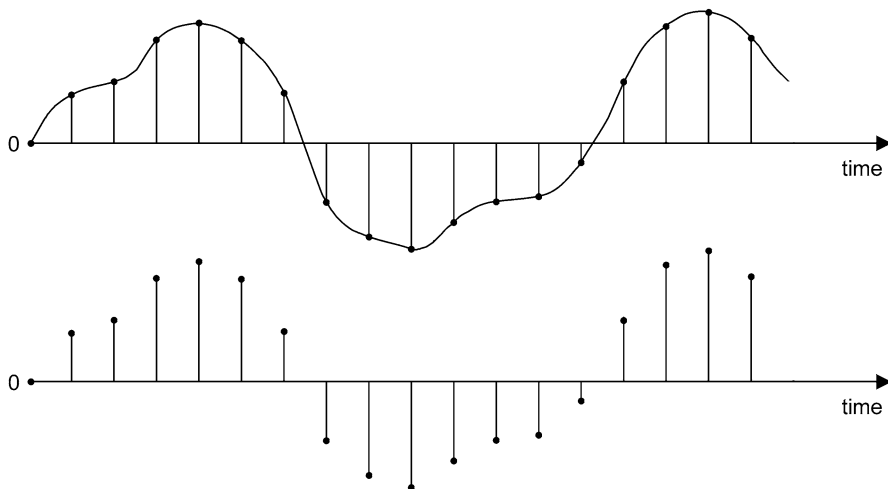


Fig. 2.11 Sampling Theorem

be mitigated by calibration, or prevented by testing. Important parameters are integral nonlinearity (INL) and differential nonlinearity (DNL). These reduce the dynamic range of the analog signals that can be digitized by the ADC, also reducing the effective resolution of the ADC.

The cost of an ADC is proportional to the following parameters: accuracy, number of bits, and stability. But even the most expensive ADC can compromise accuracy when excessive noise interferes with the input signal, whether that signal is in millivolts or much larger.

One technique for reducing noise and ensuring measurement accuracy is to eliminate ground loops that can occur when two or more devices are connected to ground terminals at different locations.

The input signal is continuous in time and is necessary to define a rate according to the extrapolation of new digital values from analog signal. The rate of new value is called sampling rate or sampling frequency of the converter (Sample and Hold, Fig. 2.11).

To process analog signals in computers, we need to convert the signals to “digital” form. To convert an analog signal to a digital form it must first be band-limited and then sampled. Theoretically the maximum frequency that can be useful is half the sampling frequency.

The sampled signals are represented by multiples of sampling period, T , as $s(nT)$ where n is an integer. Typically, an ADC is used to convert voltage (sampling value) to a digital number corresponding to a certain voltage level (Fig. 2.12). The process may be reversed through a DAC.

The sampling theorem indicates that an analog signal can be properly sampled, only if its maximum frequency is not above half of the sampling rate. If frequency components are above this limit, they will be aliased (Aliasing). We consider an analog signal composed of frequencies between DC to 2 kHz. It must be sampling

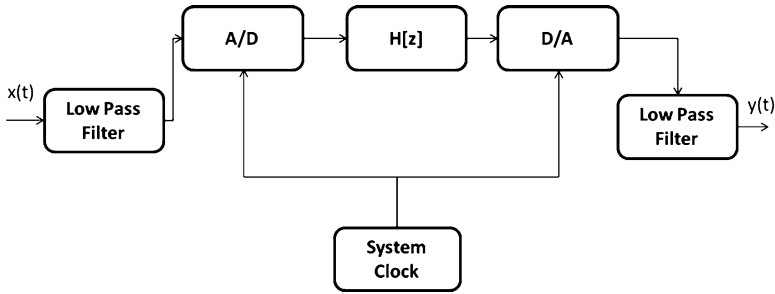


Fig. 2.12 Typical signal processing system

at least 4 samples/s (4 kHz). In this case, we choose 6 kHz, where we can note four important frequencies as parameters: (1) the highest frequency in the signal, 2 kHz; (2) twice this frequency, 4 kHz; (3) the sampling rate, 6 kHz; and (4) one-half the sampling rate, 3 kHz.

In mathematical terms, the sampling theorem (Nyquist theorem) indicates that if an analog signal $s(t)$ has a band limited, its fourier transform $S_a(i\omega)$ is given by

$$S_a(i\omega) = \int_{-\infty}^{+\infty} s(t) * \exp(-i\omega t) dt \quad (2.1)$$

such that

$$S_a(i\omega) = 0 \quad (2.2)$$

for

$$\omega \geq 2\pi W \quad (2.3)$$

Then the analog signal can be sampled with rate of period:

$$T \leq 1/2W \quad (2.4)$$

The quantity W is called the Nyquist frequency. If this rate is not verified, various types of distortion can be occurred; in particular:

- Aliasing. A precondition of the Nyquist theorem is that the signal must be bandlimited. However, in practice, no time-limited signal can be bandlimited. Designing a Sample-Hold with an appropriate guard band is possible to reduce aliasing effect.
- Jitter or deviation from the precise sample timing intervals [3, 6, 7].

The DS1843 of Maxim [11] is a sample-and-hold circuit (Figs. 2.13 and 2.14) useful for capturing fast signals where board space is constrained. It includes a differential, high-speed switched capacitor input sample stage, offset nulling circuitry, and an output buffer. The DS1843 is optimized for utilization in optical line transmission (OLT) systems for burst-mode RSSI measurement in conjunction with an external sense resistor. The input voltage is sampled using a 5 pF capacitor on the positive input and another on the negative input. The capacitors are connected to the input when SEN is high. In addition to the sampling capacitors, the inputs have

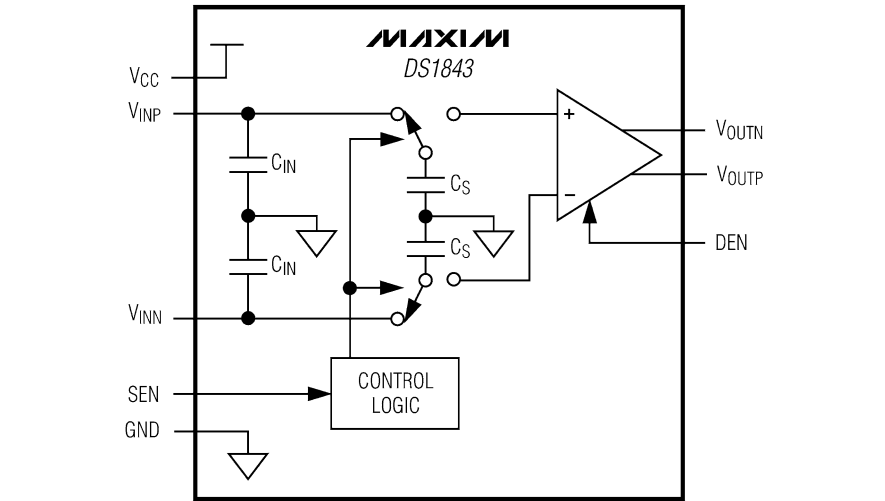


Fig. 2.13 Maxim DS1843 [8]

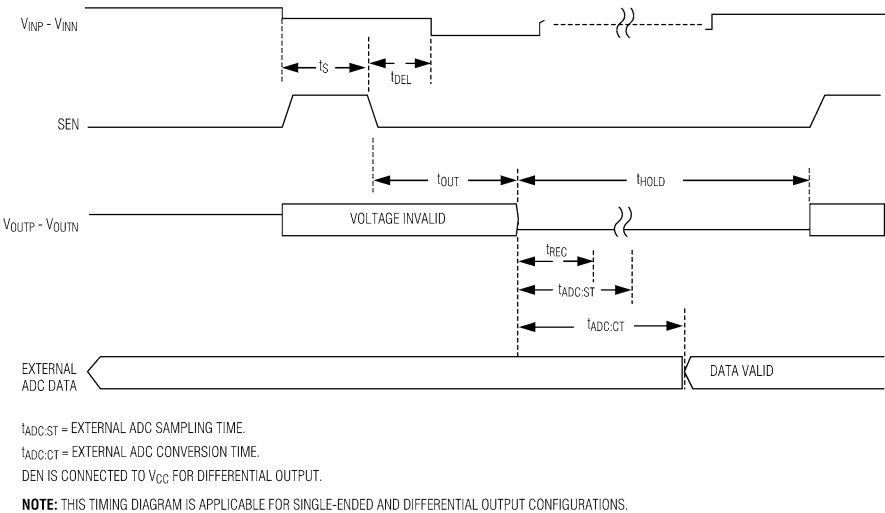


Fig. 2.14 DS1843: Timing diagram [8]

parasitic capacitance (C_{IN}). These capacitors must be fully charged before **SEN** is switched to low in order to ensure the accurate sampling. An RC time constant is created by the resistance of the voltage source connected to the DS1843s input and the capacitances on this node.

An anti-aliasing filter is a filter used before a signal sampler, to restrict the bandwidth of a signal to approximately satisfy the sampling theorem. When selecting a filter, the goal is to provide a cutoff frequency that removes unwanted

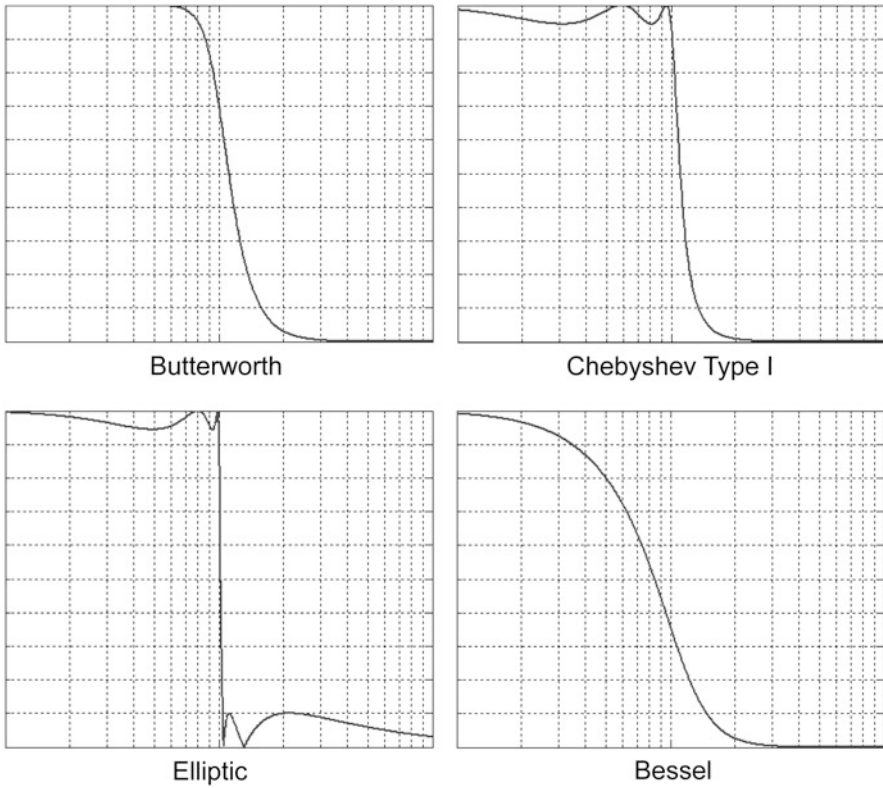


Fig. 2.15 Four basic of filter types

signals from the ADC input or at least attenuates them to the point that they will not adversely affect the circuit; which can be done by low-pass anti-aliasing filter. The key parameters that required the observation are: the amount of attenuation (or ripple) in the pass band, the desired filter roll off in the stop band, the steepness in the transition region, and the phase relationship of the different frequencies as they pass through the filter (Fig. 2.15) [5,6,8].

2.4.1 Parameters

ADC performance specifications are generally categorized in two ways: DC accuracy and dynamic performance. Most applications use ADCs to acquire signal like temperature, force, and so on. Each designer will consider the most important factor to project a specific and efficient ADC. Some important factors can be described in the following points:

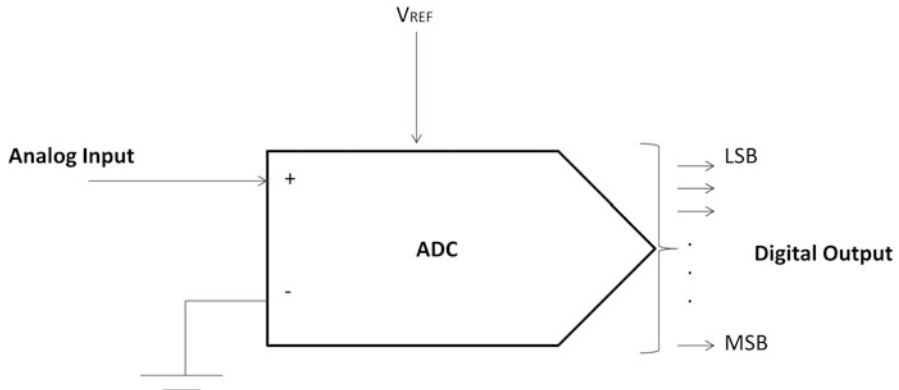


Fig. 2.16 Single ended conversion mode

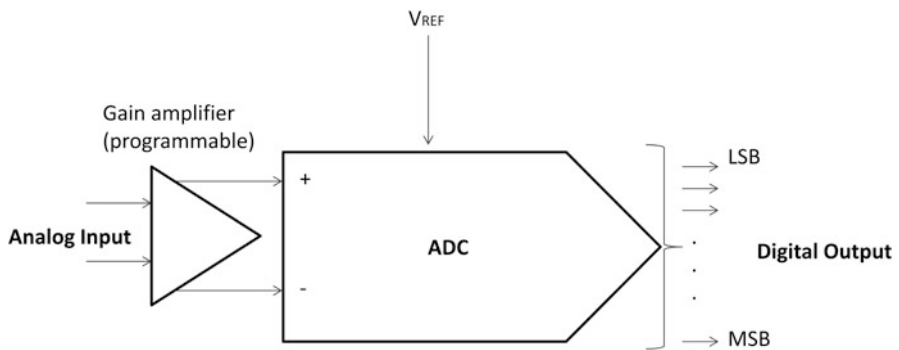
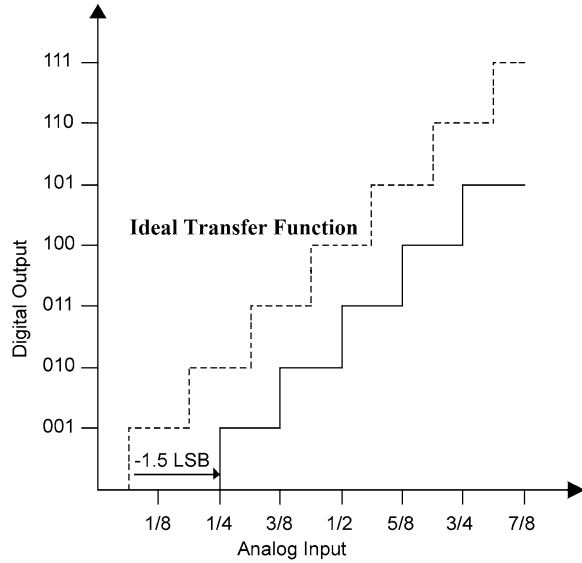


Fig. 2.17 Differential conversion mode

- **Input voltage range:** The input voltage range of an ADC is determined by the reference voltage (V_{REF}) applied to the ADC.
- **Resolution:** The resolution, expressed in bits, of the converter indicates the number of discrete values (binary) that can be produced over the range of analog values.
- **Quantization error:** Quantization error is an artifact of representing an analog signal with a digital number (in other words, an artifact of analog-to-digital conversion).
- **Conversion mode:** A conversion mode is a method in which the ADC processes the input. A standard ADC has two types of conversion modes: single ended conversion mode (Fig. 2.16) and differential conversion mode (Fig. 2.17).
- **Offset error:** The offset error is defined as the deviation of the actual ADCs transfer function from the perfect ADCs transfer function related at the point of LSB (Fig. 2.18).

Fig. 2.18 Example of (positive) offset error



- **Gain error:** The gain error is defined as the deviation of the last steps midpoint of the actual ADC from the last steps midpoint of the ideal ADC, after compensating for offset error (Fig. 2.19).
- **Signal-to-noise-ratio: SNR** is defined as the ratio of the output signal voltage level to the output noise level. It is usually represented in decibels (dB)
- **Total harmonic distortion (THD):** An input signal of a particular frequency passes through a nonlinear device. THD is defined as the ratio of the sum of powers of the harmonic frequency components to the power of the fundamental/original frequency component.
- **Impedances and capacitances of ADC:** From Fig. 2.20 the input impedance of the ADC is the combination of R_{ADC} and the impedance of the capacitor C_{ADC} that is also called as sampling capacitor.

2.4.2 Successive-Approximation ADC

One method of ADC is called successive-approximation (Fig. 2.21). The successive approximation ADC circuit typically consists of four sub circuits:

1. An S-H circuit to sample the input voltage.
2. An analog voltage comparator that compares V_i with the output of the DAC and sends the result to the successive approximation register (SAR).
3. An SAR sub-circuit designed to supply an approximate digital code of V_{in} to the DAC.
4. An internal reference DAC supplies the comparator with an analog voltage equivalent of the digital code output of the SAR for comparison with V_i .

Fig. 2.19 Example of (positive) gain error

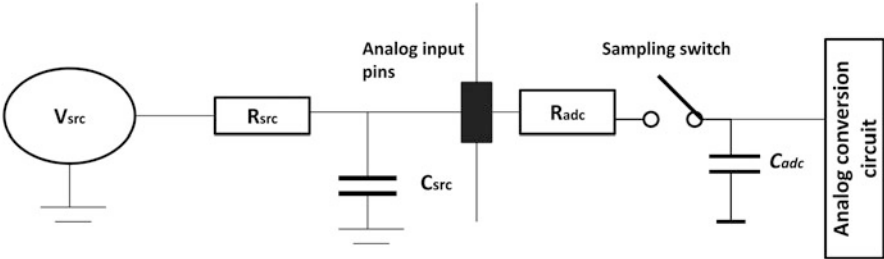
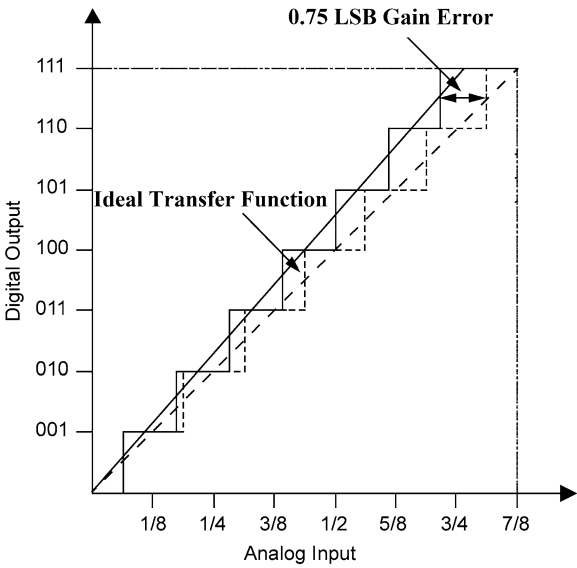
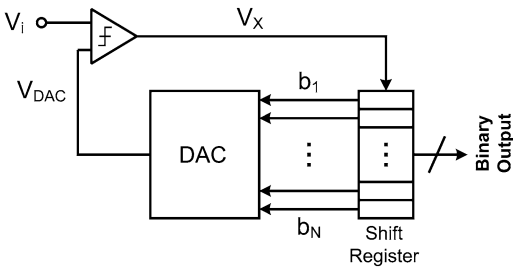


Fig. 2.20 Impedances and capacitances of ADC

Fig. 2.21 Successive-approximation ADC



The SAR is initialized so that the most significant bit (MSB) is equal to a digital 1. Then, the code is sent into DAQ which supplies the analog equivalent of this code ($V_{ref}/2$) into comparator with sampled input voltage. If this analog voltage is more bigger than V_{in} , the comparator causes the SAR to reset this bit. Then same test is done, repeating this process until every bit in the SAR is completed. The

resulting codes represent the digital conversion of the sampled input voltage and considered the output by the DAQ at the end of the conversion (EOC).

Mathematically can be described with the following equation: $V_i = x V_{ref}$, so x in $[-1, 1]$ is the normalized input voltage. The algorithm proceeds as follows:

1. Initial approximation $x_0 = 0$.
2. i th approximation $x_i = x_{i-1} - s(x_{i-1} - x)/2^i$.

where, $s(x)$ is the signum-function $sgn(x)$ ($+1$ for $x \geq 0$, -1 for $x < 0$). Using mathematical induction we have $|x_n - x| \leq 1/2^n$.

Due to the excellent power efficient and digital compatibility, successive approximation converters (SAR ADCs) have been widely used for some applications in this field. Many microcontrollers contain on-chip ADCs. For example the PIC16C7xx microcontrollers contain an 8-bit successive approximation ADC with analog input multiplexers. Most microcontroller ADCs are successive approximation because this gives the best solution between speed and the cost.

2.4.3 Flash ADC

There are several different types of ADCs, depending on the type of the application. They are classified in three main categories:

- Low speed/serial
- Medium speed
- High speed

Many applications require high speed ADCs, Flash ADC (or parallel ADC), which can be a good solution in this field.

The conversion speed in flash ADC is only one clock cycle, hence is the fastest ADC architecture (Fig. 2.22) available and it is limited only by both comparator and gate propagation delays.

In general, an N bit flash ADC consists of a resistors string, a set of comparators, and a digital encoding network implemented using XOR gates. The resistors string is composed of $2N$ resistors which are connected between $Ref+$ and $Ref-$ to produce a reference voltage for each of the comparators as visualized in Fig. 2.22. The voltage difference between these reference voltages is equal to the least significant bit (LSB) voltage [7].

The comparators are typically a cascade of wide band low-gain stages. They are low gain because at high frequencies it is difficult to obtain both wide bandwidth and high gain. The comparators are designed for low-voltage offset, so that the input offset of each comparator is smaller than an LSB of the ADC. Otherwise, the comparator's offset could falsely trip the comparator, resulting in a digital output code that is not representative of a thermometer code. A regenerative latch at each comparator output stores the result. The latch has positive feedback, so that the end state is forced to either a 1 or a 0.

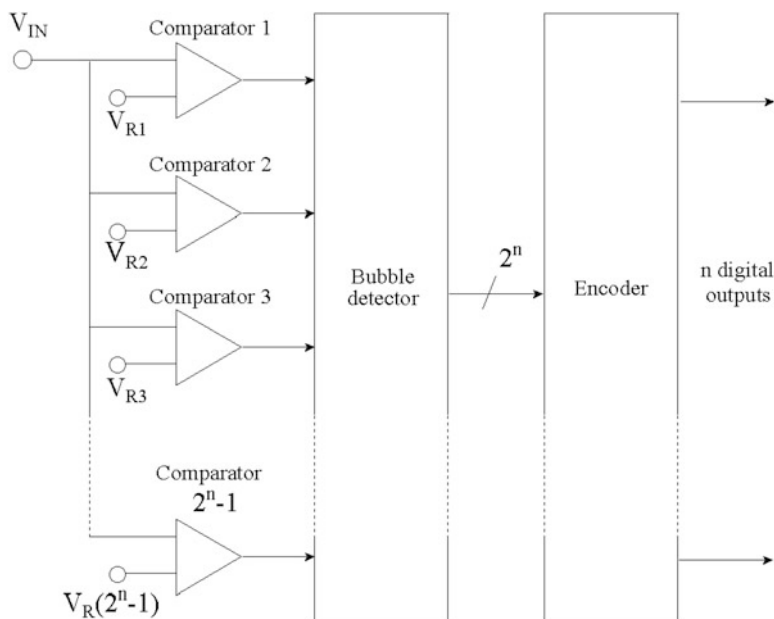


Fig. 2.22 Flash ADC

In an SAR converter, a single high-speed, high-accuracy comparator determines the bits, one bit at a time (from the MSB down to the LSB). This is done by comparing the analog input with a DAC whose output is updated by previously decided bits and thus successively approximates the analog input. This serial nature of the SAR limits its speed to no more than a few mega-samples per second (Msps), while flash ADCs exceed giga-samples per second (Gsps) conversion rates.

SAR converters are available in resolutions up to 16 bits. An example of such a device is the MAX1132. Flash ADCs are typically limited to around 8 bits. The slower speed also allows the SAR ADC to be much lower in power. The SAR architecture is also less expensive. Package sizes are larger for flash converters. In addition to a larger die size requiring a larger package, the package needs to dissipate considerable power and needs many pins for power and ground signal integrity (Fig. 2.23) [9].

Flash ADCs have been implemented in many technologies, from silicon-based bipolar (BJT) to complementary metal oxide FETs (CMOS) technologies. An additional advantage of the flash converter, often overlooked, is the ability for it to produce a nonlinear output.

A pipelined ADC works with a parallel structure where each stage works on one to a few bits of successive samples concurrently. This design improves speed of the ADC. This pipelined ADC requires accurate amplification stage in the DACs and interstages amplifiers [6, 9].

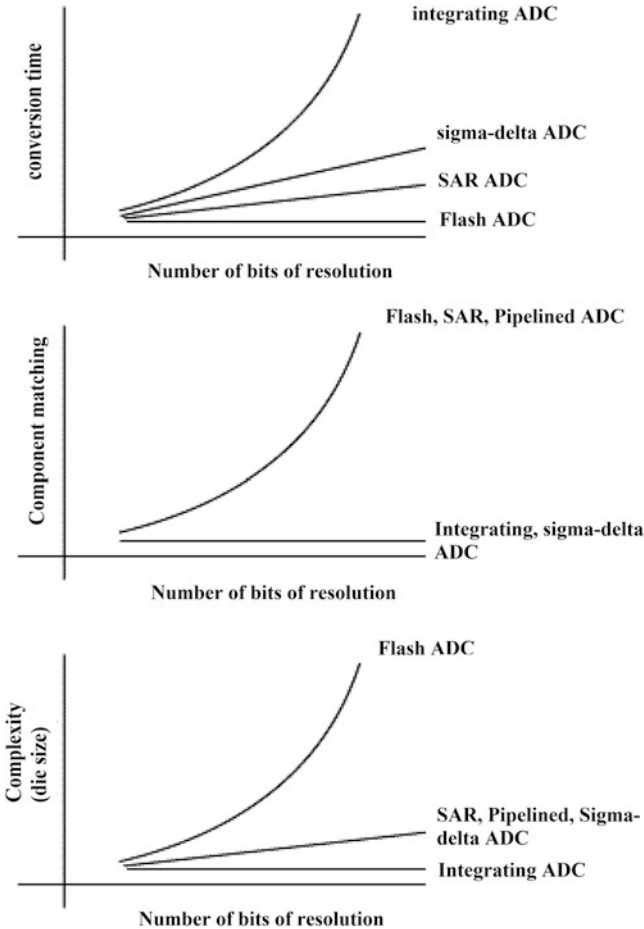


Fig. 2.23 Architectural trade-off

2.4.4 8-Bit, 500 Msps Flash ADC of Maxim

The MAX1150 [9] is a parallel flash ADC capable of digitizing full-scale (0 V to -2 V) inputs into 8-bit digital words at an update rate of 500 Msps (Figs. 2.24 and 2.25). The ECL-compatible outputs are demuxed into two separate output banks, each with differential data-ready outputs to ease the task of data capture. The MAX1150s (Fig. 2.26) wide input bandwidth and low capacitance eliminate the need for external track/hold amplifiers for most applications: DAQ systems, radar, digital oscilloscope. A major advance over previous flash converters is the inclusion of 255 input preamplifiers between the reference ladder and input comparators. The preamplifiers act as buffers to stabilize the input capacitance so that it remains constant over different input voltage and frequency ranges, making the part easier

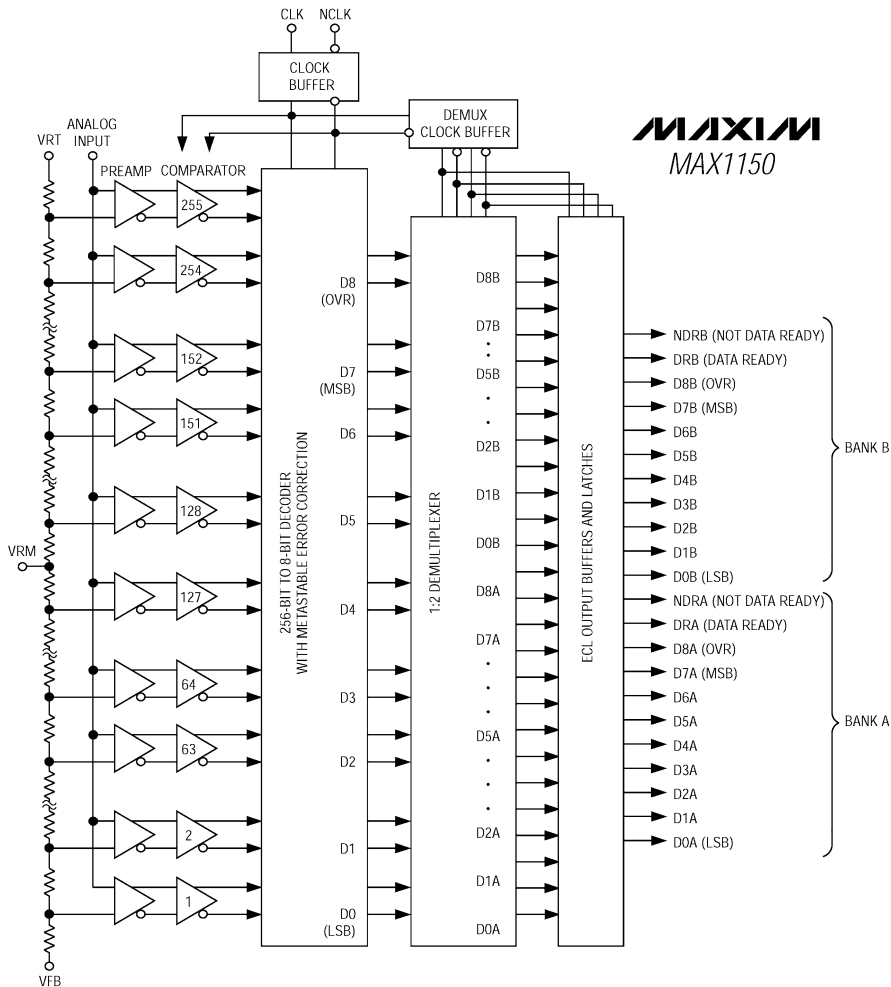


Fig. 2.24 Functional Diagram of MAX1150 [10]

to drive than previous flash converters. The circuit of Fig. 2.25 shows a method of achieving the least error by correcting for integral linearity, input-induced distortion, and power-supply/ground noise (Fig. 2.23) [10].

2.5 Converters D/A

A DAC is an electronic device that converts a digital (usually binary) signal to an analog signal (current, voltage, or electric charge). A common use of DACs is the generation of audio signals from digital information in music players.

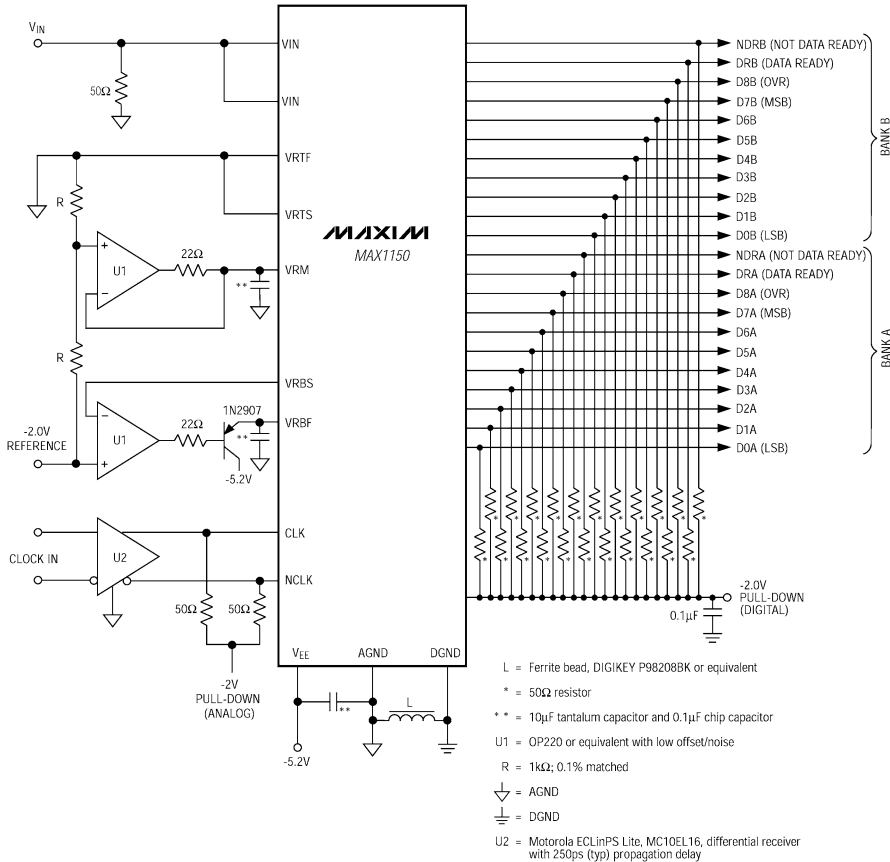


Fig. 2.25 Circuit of ADC with MAX1150 [10]

DACs (Fig. 2.28) are almost exclusively used on integrated circuits; there are many DAC architectures which have different advantages and disadvantages. The choice of a particular DAC for an application is determined by a variety of measurements including some parameters such as speed and resolution [6].

2.5.1 Parameters

DACs are very important to system performance. The most important characteristics of these devices are:

- Resolution: This is the number of possible output levels the DAC is designed to reproduce.

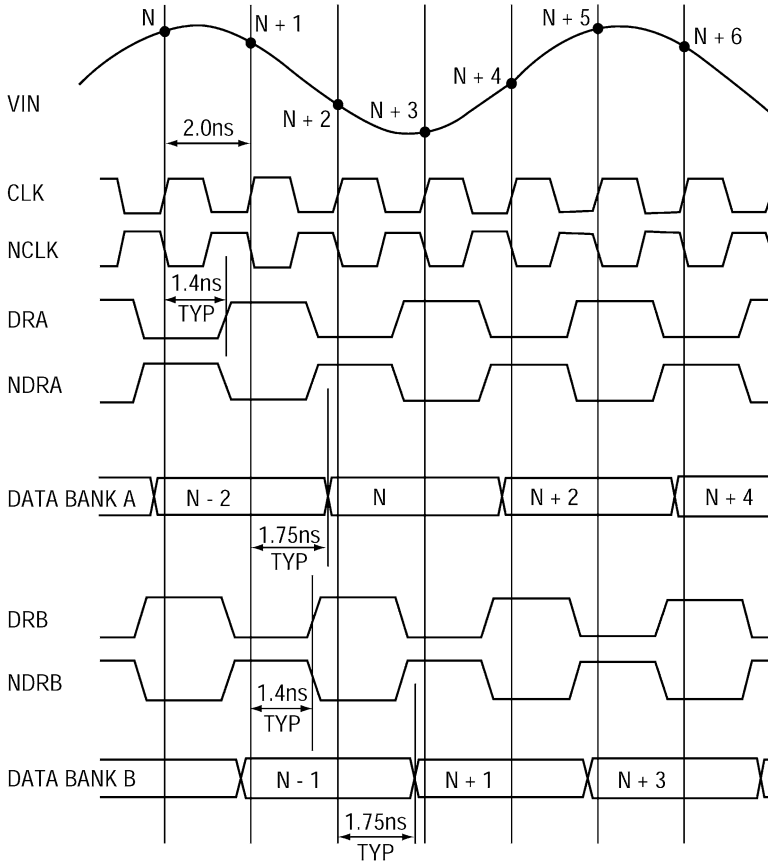


Fig. 2.26 Timing diagram of MAX1150 [10]

- **Monotonicity:** Ability of a DAC's analog output to move only in the direction that the digital input moves.
- **Full scale range (FSR):** Maximum output signal for the DAC.
- **SFDR, Spurious Free Dynamic Range:** The difference between the RMS power of the fundamental frequency and the largest spurious signal in the bandwidth.
- **Glitch (Fig. 2.29):** When a DAC is set to a desired output code, it does not immediately converted to the specific output current or voltage. It changes to the new output value over a finite time (the settling time) and that can cause signal spikes (glitches) rather than transitioning from old to new output values smoothly and monotonically. Because the glitch occurs right after a DAC is updated and disappeared within the first few microseconds, if the DAC output and output buffer amplifier input are decoupled when the DAC is updated and stay decoupled until the glitch disappears, the glitch will not pass through the output buffer amplifier. As shown in Fig. 2.30, this solution uses an S/H concept

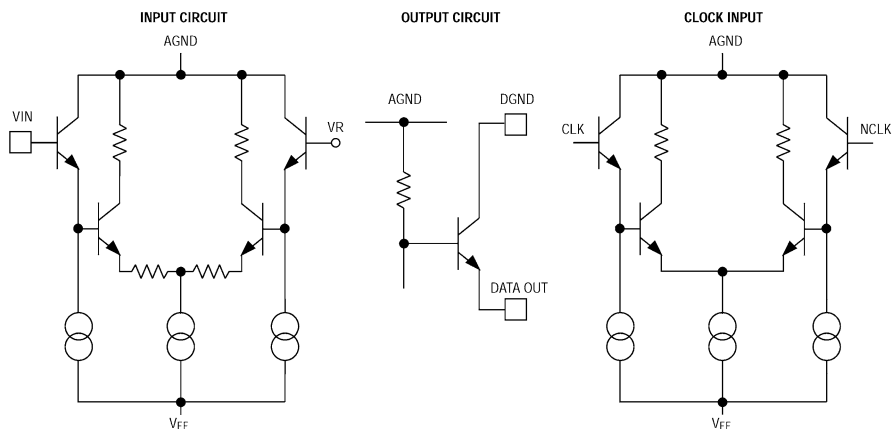


Fig. 2.27 Internal circuit of MAX1150 [10]

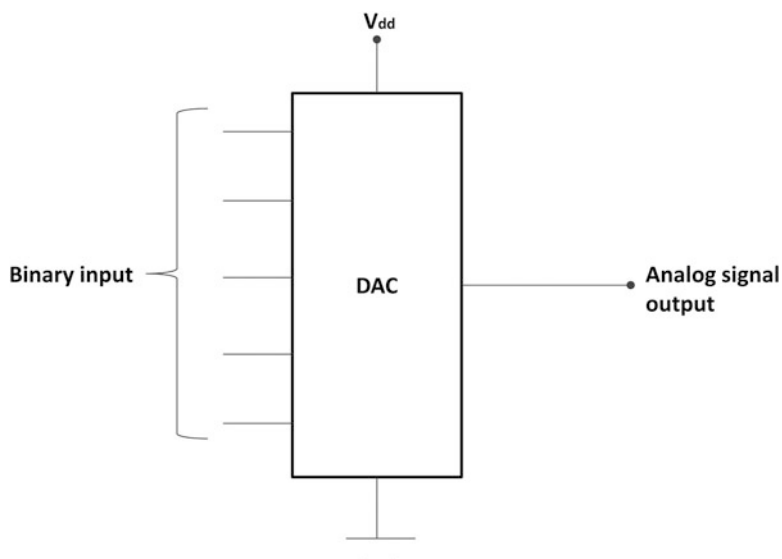


Fig. 2.28 Converter D/A

to eliminate glitches. Before the DAC is updated, switch SW1 is closed. The sampling capacitor samples the DC level of the previous DAC code. During a digital code transition, as the DAC is being updated, the switch is opened and the capacitor (CH) holds the DC level of the previous DAC code. The amplifier output is maintained at this DC level while the glitch occurs. After the glitch disappears, the switch closes again. The value of the T/H capacitor can be much smaller, because this capacitor is used to hold the DC level of the previous DAC code, as opposed to reducing the amplitude of a glitch. Small glitches

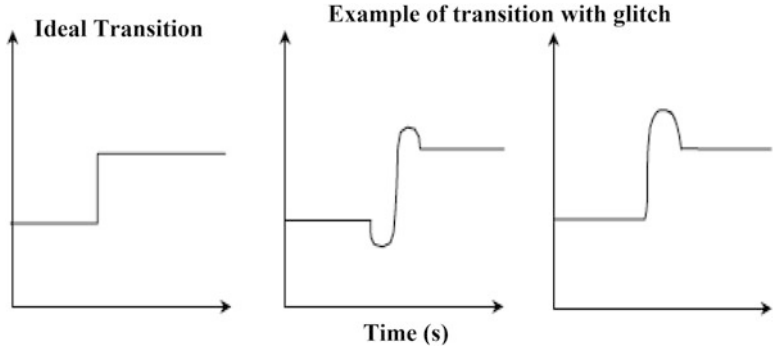


Fig. 2.29 Glitch

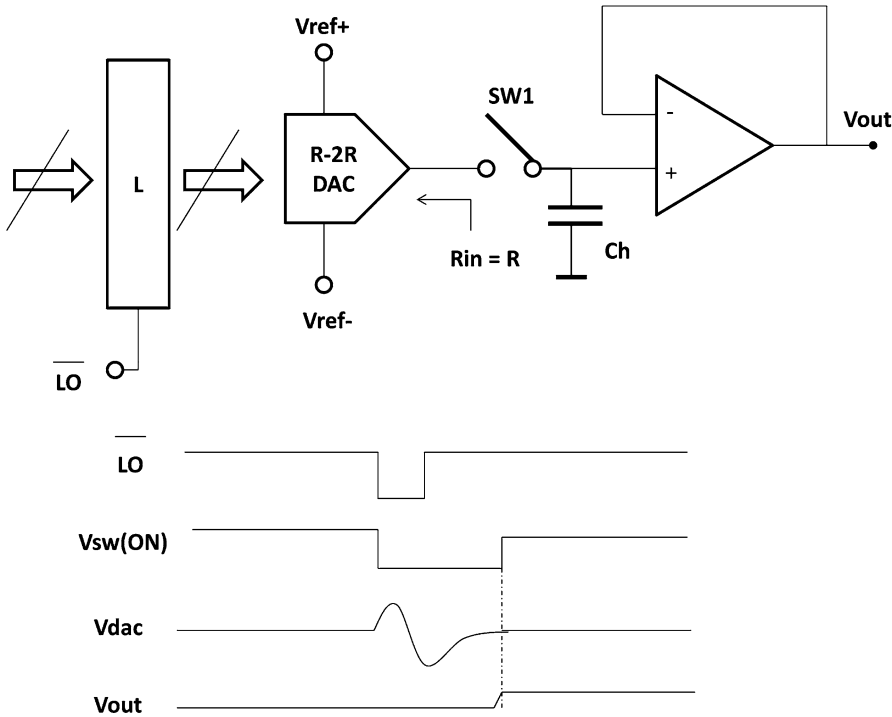


Fig. 2.30 Integrated T/H deglitch architecture [11]

can still occur when the T/H switch is turned on or off due to charge sharing and injection, but the associated glitch amplitude is much smaller. An improved Deglitches Circuit can be visualized in Fig. 2.31: To eliminate the base current of the sampling switch, differential charge cancellation is being used [11].

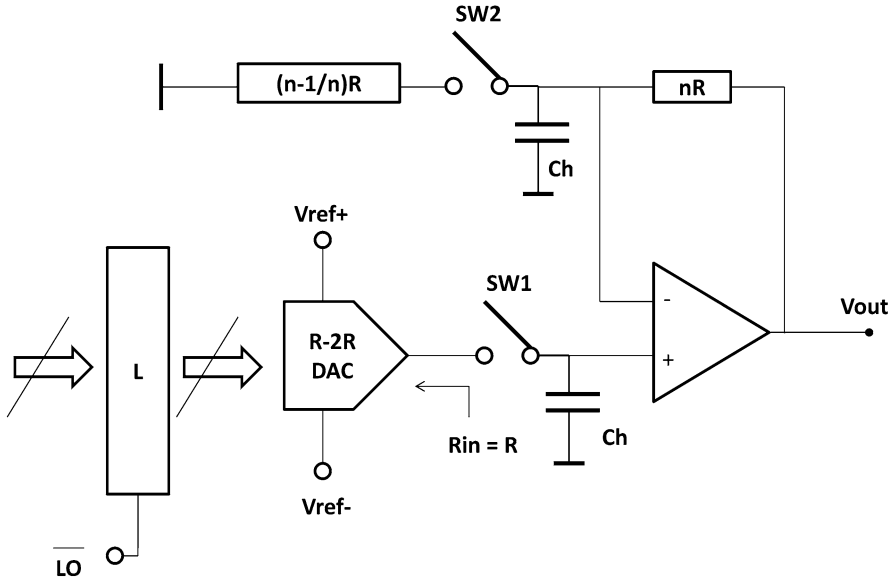


Fig. 2.31 Deglitch architecture [11]

- **Maximum sampling rate:** This is a measurement of the maximum speed at which the DACs can work to produce the correct output.

2.5.2 Binary-Weighted-Input DAC

An example of the DAC architecture is called binary-weighted input; it is a variation on the inverting summer op-amp circuit. The based circuit visualized in Fig. 2.32 is an operational amplifier in negative feedback to control the gain with several inputs. If we drive the inputs of this circuit with digital gates, the output voltage will be an analog representation of the binary value of these three bits (Fig. 2.33).

2.5.3 The R-2R DAC

An alternative to the binary-weighted-input DAC is the R/2R DAC (Fig. 2.34), which uses fewer unique resistor values. A disadvantage of the previous DAC design can be identified in different and precise input resistor values.

In an R-2R DAC design with supply voltages exceeding ± 5 V, large voltage glitches (up to 1.5 V) can occur during the DAC's major-carry transitions. These glitches can propagate through the buffer amplifier and appear at output. The

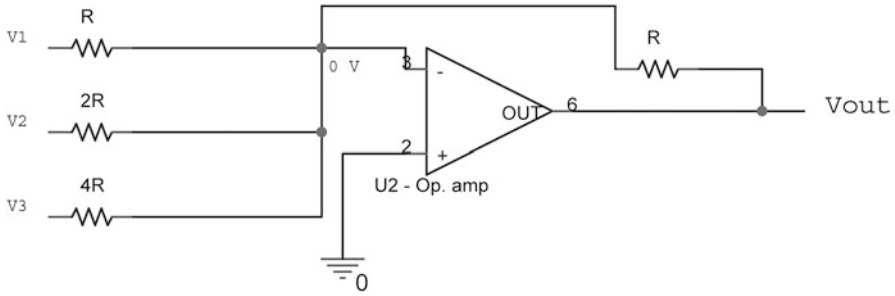


Fig. 2.32 Binary-weighted-input DAC

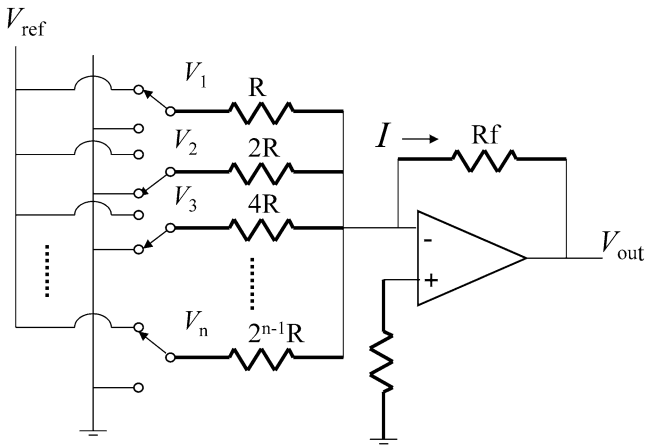


Fig. 2.33 Binary-weighted-input DAC

slewing of the level shifters that control the top (VREF+) and bottom (VREF-) single-pole double-throw switches causes the glitches (Fig. 2.35) [11].

2.5.4 8-Bit DACs with 2-Wire Serial Interface of Maxim

The MAX5109 [12] dual 8-bit DACs feature nonvolatile registers (Figs. 2.36 and 2.37). The MAX5109 has independent high and low reference inputs allowing maximum output voltage range flexibility. The reference rails accept voltage inputs that range from ground to the positive supply rail.

Applications:

- Digital gain and offset adjustments
- Programmable attenuators
- Portable instruments

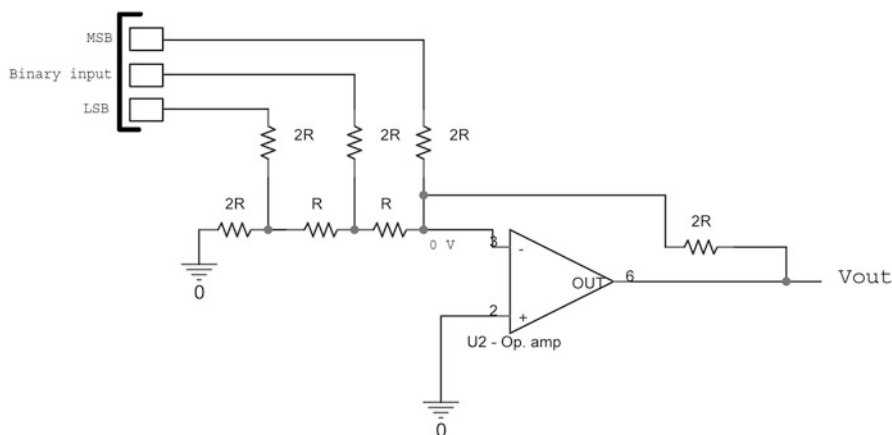
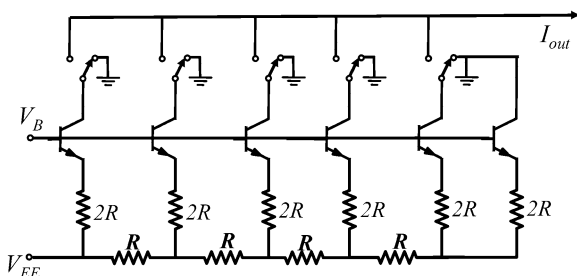


Fig. 2.34 R-2R DAC

Fig. 2.35 The R-2R DAC: simplified circuit



The MAX5109 uses a DAC matrix decoding architecture that saves power. A resistor string divides the difference between the external reference voltages, V_{REFH} and V_{REFL} . Row and column decoders select the appropriate tap from the resistor string, providing the equivalent analog voltage. The resistor string presents a code-independent input impedance to the reference and guarantees a monotonic output. Figure 2.38 shows a simplified diagram of one DAC [12].

The MAX5109 (Fig. 2.39) 8-bit DACs feature internal, nonvolatile registers that store the DAC states for initialization during power-up. This device consists of resistor-string DACs, rail-to-rail output buffers, a shift register, power-on reset (POR) circuitry, and volatile and nonvolatile memory registers (Fig. 2.38). The shift register decodes the control and address bits, routing the data to the proper registers. Writing data to a selected volatile register immediately updates the DAC outputs. The volatile registers retain data as long as the device is powered. Removing power clears the volatile registers. The nonvolatile registers retain data even after power is removed. On startup, when power is first applied, data from the nonvolatile registers is transferred to the volatile registers to automatically initialize the device. Read data from the nonvolatile or volatile registers using the 2-wire serial interface [12].

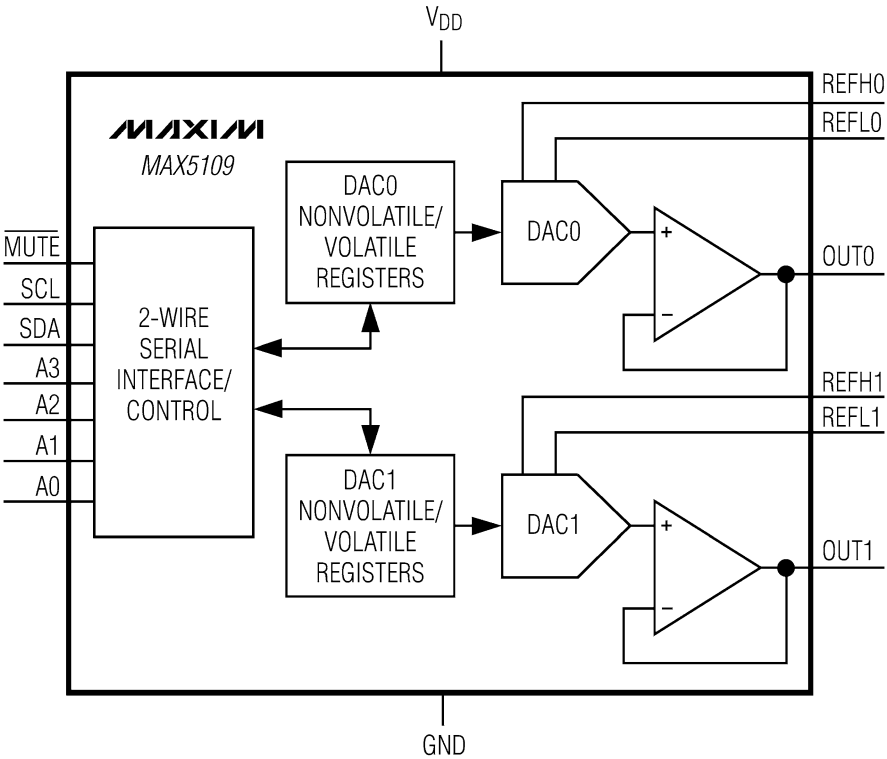


Fig. 2.36 MAX5109: Outline [12]

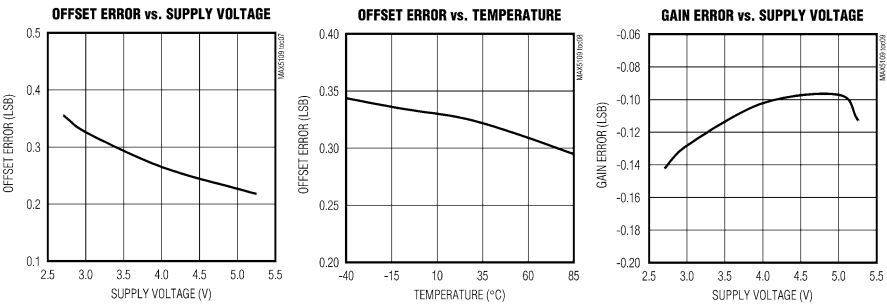


Fig. 2.37 MAX5109: Typical operating characteristics [12]

The MAX5109 features an I2C-compatible, 2-wire serial interface consisting of a bidirectional serial data line (SDA) and a serial clock line (SCL). SDA and SCL facilitate bidirectional communication between the MAX5109 and the master at rates up to 400 kHz (Fig. 2.40). The master (typically a microcontroller) initiates data transfer on the bus and generates SCL. SDA and SCL require pullup resistors

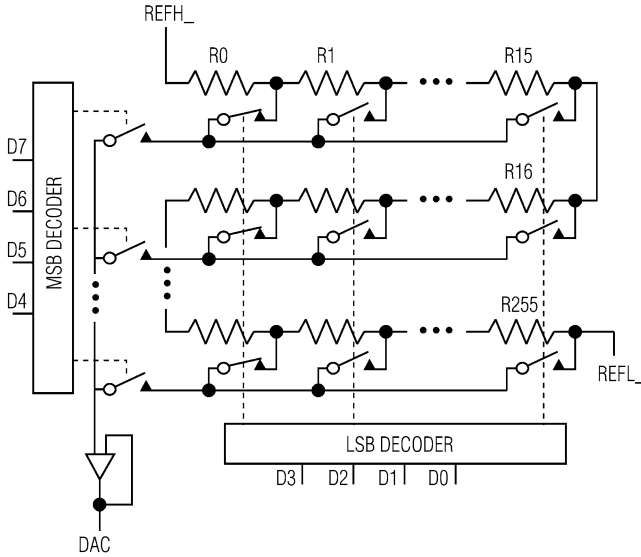


Fig. 2.38 MAX5109: DAC simplified circuit diagram [12]

(2.4 k Ω or greater). Optional resistors (24 Ω) in series with SDA and SCL protect the device inputs from high-voltage spikes on the bus lines. Series resistors also minimize crosstalk and undershoot of the bus signals.

The MAX5109 is compatible with existing I2C systems. SCL and SDA are high-impedance inputs; SDA has an open-drain output. The typical operating circuit shows an I2C application. The communication protocol supports standard I2C 8-bit communications. The general call address is ignored, and CBUS formats are not supported. The device's address is compatible with 7-bit I2C addressing protocol only. No 10-bit address formats are supported [12].

2.5.5 MAX5893 High Speed A/D

The MAX5893 (Figs. 2.41 and 2.42) programmable interpolating, modulating, 500 Msps, dual DAC offers superior dynamic performance and is optimized for high performance wide band, single-carrier transmit applications. The device integrates a selectable 2x/4x/8x interpolating filter, a digital quadrature modulator, and dual 12-bit high-speed DACs on a single integrated circuit. At 30 MHz output frequency and 500 Msps update rate, the in-band SFDR is 84 dBc while consuming 1.1 W. The device also delivers 72 dB ACLR for single-carrier WCDMA at a 61.44 MHz output frequency. The selectable interpolating filters allow lower input data rates while taking advantage of the high DAC update rates. These linear-phase interpolation filters ease reconstruction filter requirements and enhance the pass band dynamic

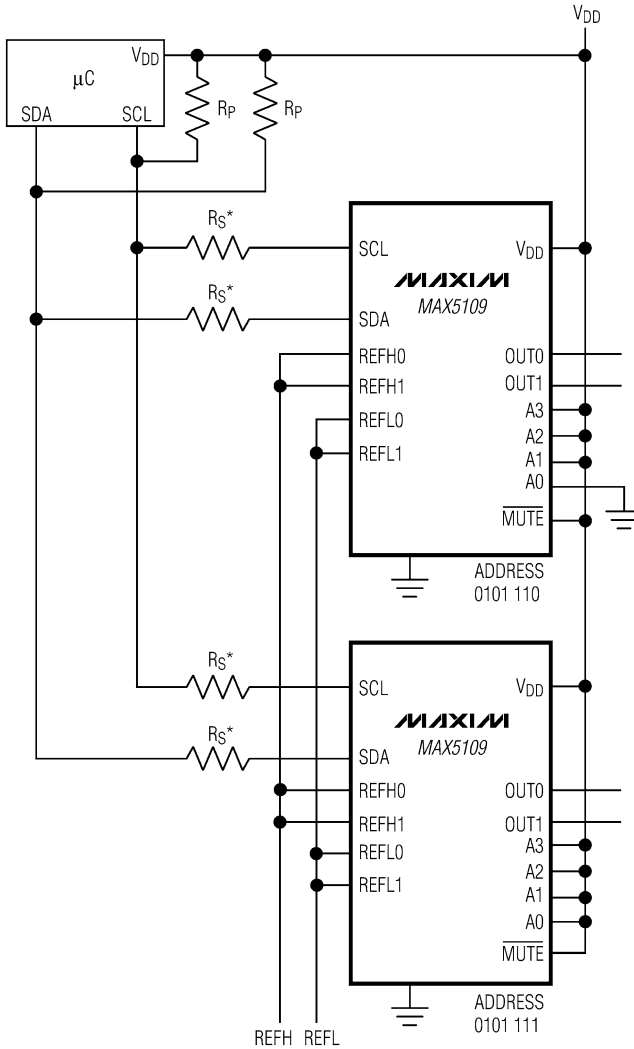


Fig. 2.39 MAX5109: Typical operating circuit [12]

performance. Individual offset and gain programmability allow the user to calibrate out local oscillator (LO) feedthrough and sideband suppression errors generated by analog quadrature modulators. The MAX5893 features a standard 1.8 V CMOS, 3.3 V tolerant data input bus for easy interface. A 3.3 V SPI port is provided for mode configuration. The programmable modes include the selection of 2x/4x/8x interpolating filters, $f_{IM}/2$, $f_{IM}/4$ or no digital quadrature modulation with image rejection, channel gain and offset adjustment, and offset binary or twos complement data interface [13].

2.6 Digital Signal Processing

Digital Signal Processing (DSP) is one of the core technologies in quickly growing. Applications can be found in wireless communications, audio and video processing, and industrial control. DSP has become a key electronic component in many of the medical and industrial products. In Math, DSP can be defined as manipulation of an information to modify or improve it in some way.

The general purpose of digital signal processors (Fig. 2.43) is dominated by applications in embedded. They also found application in cellular phones, modem, high definition television, and so on.

Some features of DSP are as follows:

- Efficient memory access
- Circular buffering: Circular buffers are used to store the most recent values of a continually updated signal
- Specialized instruction sets

DSP computes using sampled digital data; all applications require filter device. Filtering is done using finite impulse response (FIR) filter. The output of this filter is a weighted linear combination of current. The operation is described by the following equation, which defines the output sequence $y[n]$ in terms of its input sequence $x[n]$:

$$y[n] = \sum_{i=0}^N b_i x[n-i] \quad (2.5)$$

where:

- $x[n]$ is the input signal
- $y[n]$ is the output signal
- b_i are the filter coefficients, also known as tap weights, that make up the impulse response
- N is the filter order

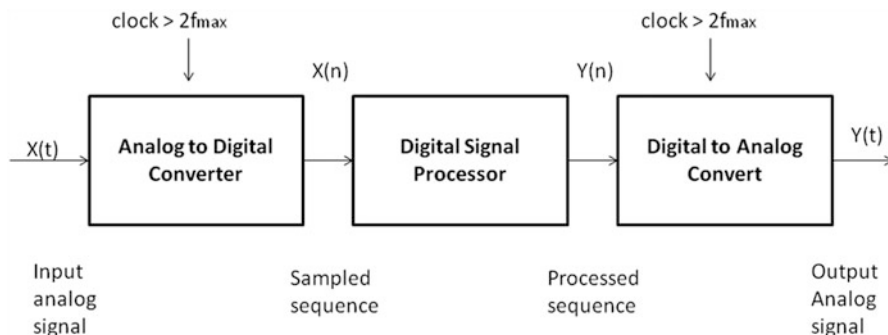


Fig. 2.43 Digital signal processing

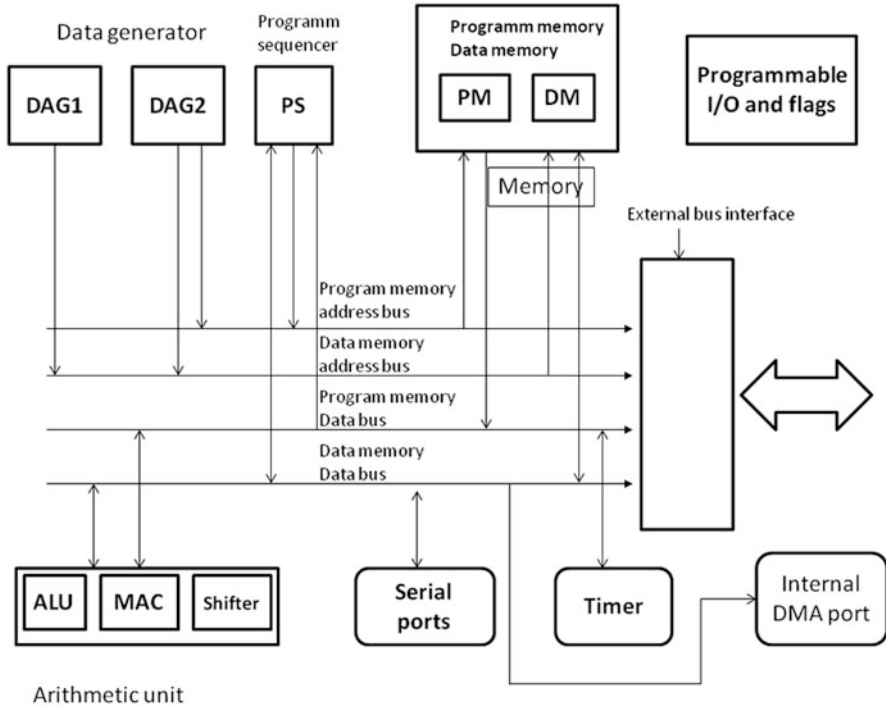


Fig. 2.44 Architecture of a DSP

The properties of an FIR can be described in the following points:

- Require no feedback
- Are inherently stable
- They can easily be designed to be linear phase

2.6.1 Architecture of a DSP

The architecture of a DSP can be described by Fig. 2.44. Data memory and program memory with relative address and data buses are connected to the ALU. DSPs have two calculation units: data address generators (DAGs). Besides DAGs, a unit called program sequencer is also provided in many DSP chips. The most important characteristic of the computing unit of a DSP is a fast multiply-accumulate unit known as MAC. On-chip serial and parallel I/O ports and DMA controller are normally provided [5].

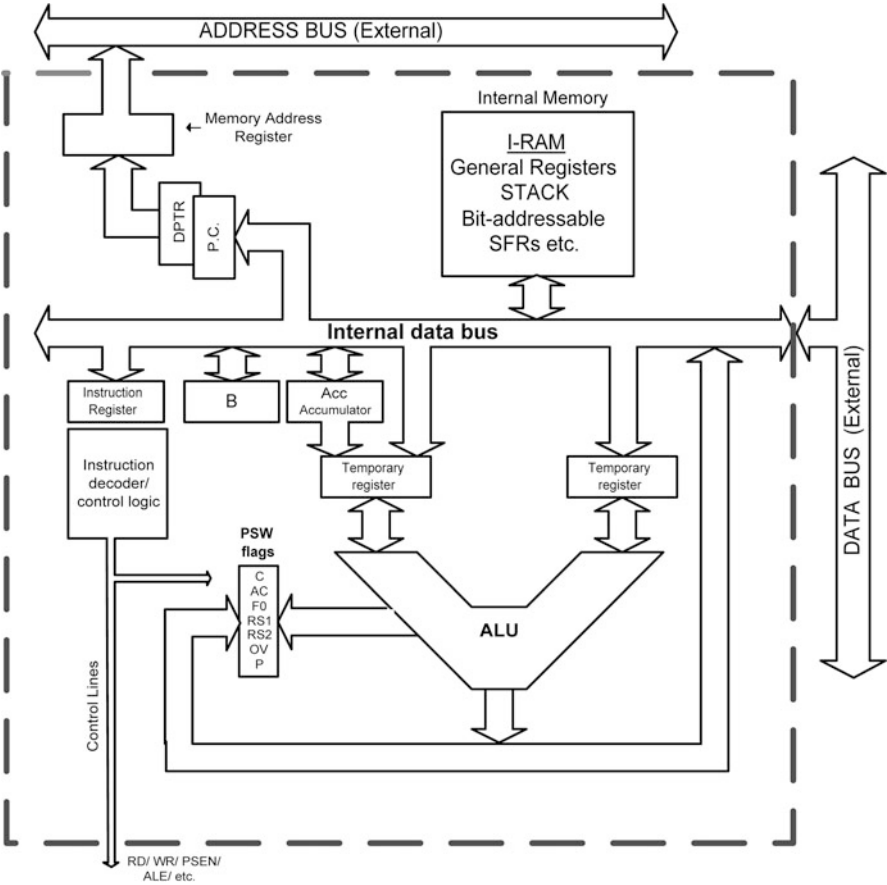


Fig. 2.45 Internal part of a microprocessor

2.7 Microprocessor and Microcontrollers

The functions of a computer’s central processing unit (CPU) can be incorporated in a microprocessor. It is a programmable device that accepts digital data in input and can be defined as an example of sequential logic circuit (Fig. 2.45).

2.7.1 CPU Structure

The CPU can be composed of the following units:

Arithmetic and Logic Unit (ALU): The goal is the execution of operations such as addition, subtraction, and so on.

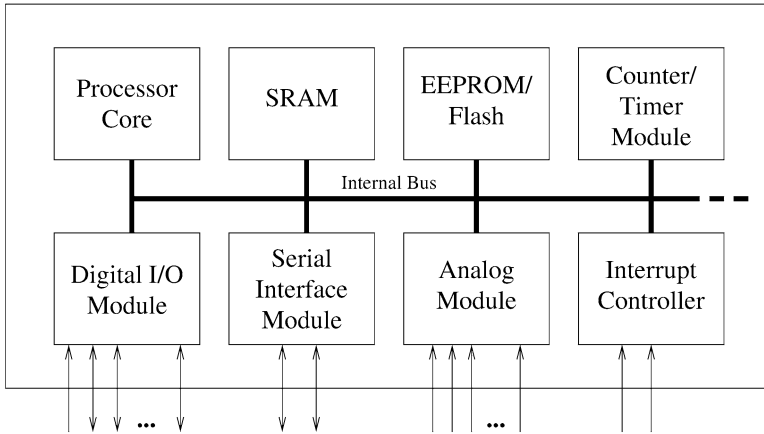


Fig. 2.46 Microcontroller: basic layout

Control Unit (CU): It checks the instructions in and out of the processor, and also controls the operation of the ALU.

Register Array: It is used for the fast storage and recovery of data and instructions.

System Bus: It is used for connections between the processor, memory, and peripherals.

Memory: An distinction of memory types can be made in the following ways:

- **Register File:** relatively small memory embedded on the CPU.
- **Data Memory:** for longer term storage.
- **Instruction Memory:** like the data memory, the instruction memory is usually a relatively large external memory (at least with general CPUs).

The instruction set is an important feature of any CPU. It influences the code size and much memory space the program is contained. The metrics of the instructions set that are important for a design decision are: instruction size, execution speed, available instructions, and addressing modes.

2.7.2 Microcontrollers

A microcontroller (Fig. 2.46) differs from a microprocessor in many ways. The most important difference is its functionality. The microprocessor must be used with other components such as memory or components for data transfer. Simply, in order to communicate with peripheral environment, the microprocessor must use specialized devices. On the other hand, the microcontroller is designed to be all in one. As example, we consider the microcontroller of Maxim: MAXQ612/MAXQ622. In the Fig. 2.46 it is visualized the block diagram of a typical microcontroller. All components are connected via an internal bus and all devices are on chip:

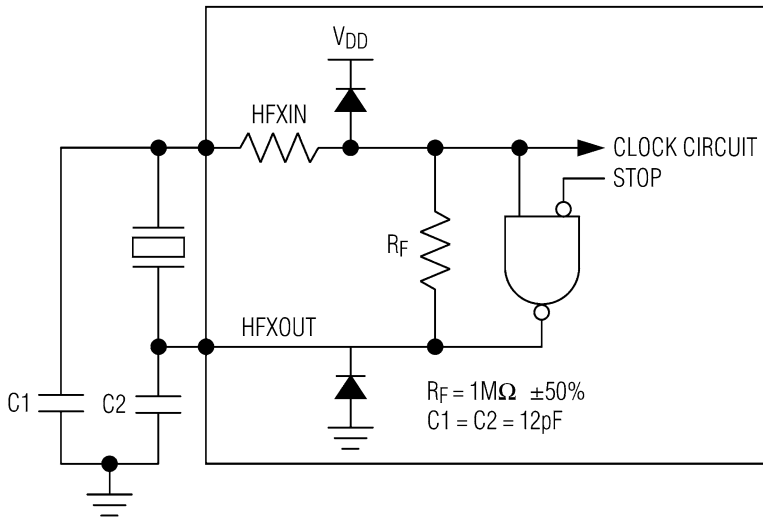


Fig. 2.47 Microcontroller MAXQ612/MAXQ622: on-chip oscillator [14]

- Processor Core: Arithmetic logic unit, the control unit, and the registers (stack pointer, program counter, accumulator register, register file, ...)
- Memory
- Interrupt controller
- Digital I/O
- Interfaces
- Watchdog timer
- Debugging unit
- Timer/counter
- Interrupts

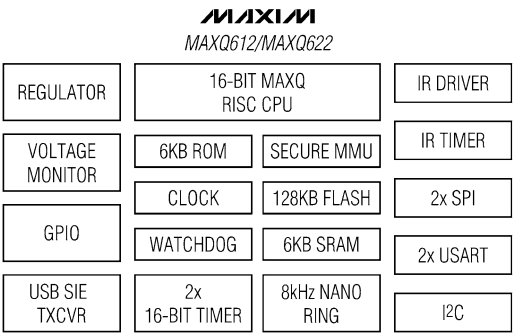
The basic purpose of any such interface is to allow microcontroller to communicate with other units, microcontrollers, peripherals, or a host PC:

- The Serial Communication Interface (SCI): asynchronous communication interface (Universal Asynchronous Receiver Transmitter, UART).
- The Serial Peripheral Interface (SPI) is a simple synchronous point-to-point interface based on a master–slave principle.
- The Inter-IC bus (IIC) is a synchronous bus that operates on a master–slave principle.

2.7.3 Microcontroller MAXQ612/622

The MAXQ612/MAXQ622 (Figs. 2.47, 2.48) is based on a low-power implementation of the new 16-bit MAXQ family of RISC cores. The core supports the Harvard memory architecture with separate internal 16-bit program and data address buses.

Fig. 2.48 Microcontroller
MAXQ612/MAXQ622:
block diagram [14]



A fixed 16-bit instruction word is standard, but data can be arranged in 8 or 16 bits. The MAXQ core is a pipelined processor with performance approaching 1 MIPS per MHz. The 16-bit data path is implemented around register modules, and each register module contributes specific functions to the core. The accumulator module consists of sixteen 16-bit registers and is tightly coupled with the arithmetic logic unit (ALU). Program flow is supported by a configurable soft stack. Execution of instructions is triggered by data transfer between functional register modules or between a functional register module and memory. Because data movement involves only source and destination modules, circuit switching activities are limited to active modules only. For power-conscious applications, this approach localizes power dissipation and minimizes switching noise. The modular architecture also provides a maximum of flexibility and reusability that are important for a microprocessor used in embedded applications [14]. The microcontroller incorporates several memory types:

- 128 KB program flash memory
- 6 KB SRAM data memory
- 6 KB utility ROM
- Soft stack

A 16-bit-wide internal stack provides storage for program return addresses and can also be used for general purpose data storage. The internal watchdog timer greatly increases system reliability. The timer resets the device if software execution is disturbed. The watchdog timer is a free-running counter designed to be periodically reset by the application software. The dual-integrated SPI interfaces provide independent serial communication channels that communicate synchronously with peripheral devices in a multiple master or multiple slave system. The interface allows access to a 4-wire, full-duplex serial bus, and can be operated in either master mode or slave mode. Collision detection is provided when two or more masters attempt a data transfer at the same time. The microcontroller integrates an internal I2C bus master/ slave for communication with a wide variety of other I2C-enabled peripherals. The I2C bus is a 2-wire, bidirectional bus using two bus lines—the serial data line (SDA) and the SCL—and a ground line. Both the SDA and SDL lines must be driven as open collector/ drain outputs. External resistors are required to pull the lines to a logic-high state [14].

2.8 Amplifier

Signal amplifiers are electronic devices with the ability to amplify a relative small signal of a sensor (temperature sensors, magnetic field sensor, and so on). The quality of an amplifier can be described by a number of parameters, listed below:

- Gain: The ratio between output and input power or amplitude; it is usually measured in decibels.
- Bandwidth: The range of frequencies for which the amplifier works correctly.
- Noise: The noise level introduced in the amplification process.
- Slew rate: The maximum rate of voltage change per unit time.
- Overshoot: The output exceeds in its final value.

A particular amplifier is the feedback amplifier (Fig. 2.49): an amplifier which combines the output with the input so that a negative feedback opposes the original signal. Feedback in amplifiers gives better performance, in particular [6]:

- Increases the stability in the amplification
- Reduces distortion
- Increases the bandwidth of the amplifier

2.8.1 Design of Low-Noise Pre-amplifier

Low-noise amplifier (LNA) is an electronic amplifier used to amplify possibly very weak signals. A preamplifier is an electronic device which amplifies an analog signal. Generally is the stage that anticipates the high power amplifier.

In this example we design a simple preamplifier with background noise of the order of 0.8 nV/Hz@1 kHz. The circuit diagram is shown in Fig. 2.50. The main components used are LT1128 dell Linear Tech. and the JFET IF3602 of

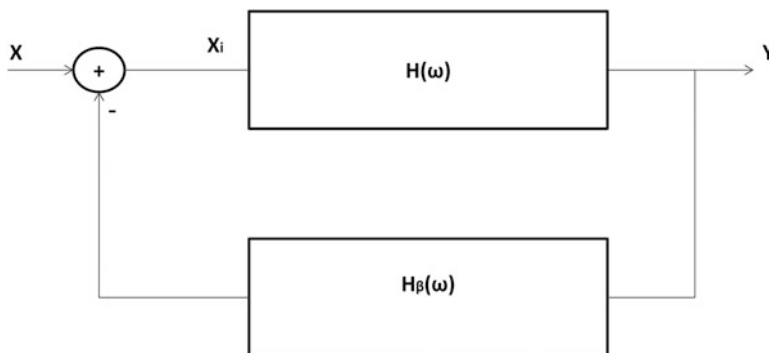


Fig. 2.49 Model of a feedback amplifier

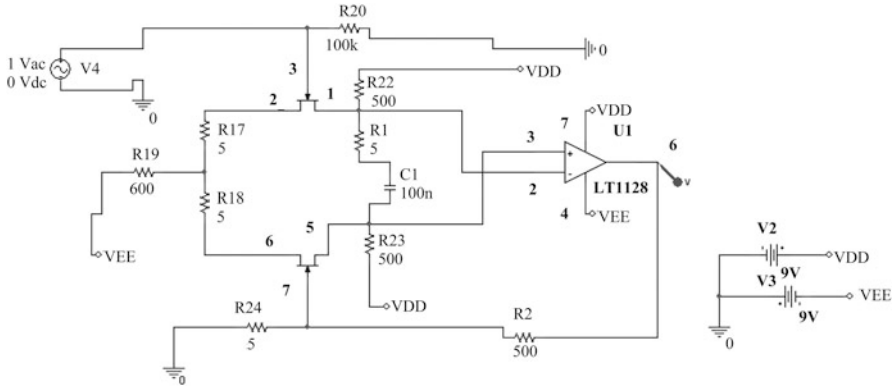


Fig. 2.50 Low noise preamplifier

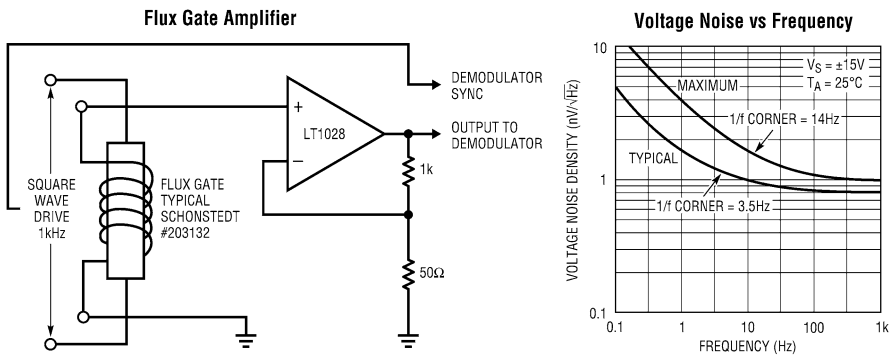


Fig. 2.51 Voltage noise LT1128 [15]

InterfetCorporation [15]. LT1128 (Figs. 2.51 and 2.52) is an operational amplifier ultra noise at high speed. Main characteristics are the following:

- Noise voltage: 0.85 nV/z@1 kHz
- Bandwidth: 13 MHz
- Slew rate: 5 V/uS
- Offset voltage: 40 uV

The IF3602, instead, is a Dual-N JFET used as stage for input of the operational amplifier.

The op-amp is one type of differential amplifier (Fig. 2.53). The inputs of the differential amplifiers consist of a $V+$ and a $V-$ input, and ideally the op-amp amplifies only the difference in voltage between the two, which is called the differential input voltage [6].

The operational amplifier can be realized with bipolar junction transistor (BJT, as in the case of the LT1128) or MOSFET, which works at higher frequencies, with an

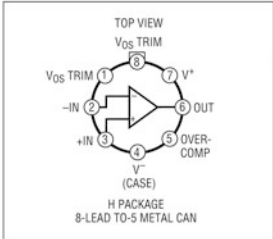
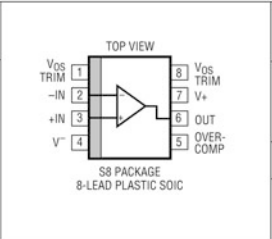
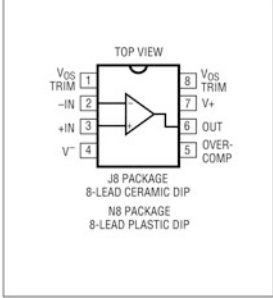
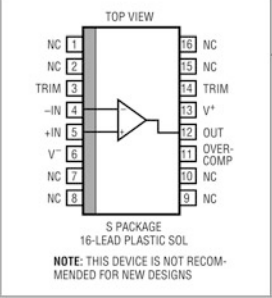
	ORDER PART NUMBER		ORDER PART NUMBER
	LT1028AMH LT1028MH LT1028ACH LT1028CH		LT1028CS8 LT1128CS8
			S8 PART MARKING
	ORDER PART NUMBER		ORDER PART NUMBER
	LT1028AMJ8 LT1028MJ8 LT1028ACJ8 LT1028CJ8 LT1028ACN8 LT1028CN8 LT1128AMJ8 LT1128MJ8 LT1128CJ8 LT1128ACN8 LT1128CN8		LT1028CS16

Fig. 2.52 Pin-outs of LT1128 [15]

input impedance higher and a lower energy consumption. The differential structure is used in those applications where it is necessary to eliminate the undesired common components to the two inputs. In this way, in output are eliminated eventual DC components on the input signal such as, for example, the thermal drift. The block diagram of the differential amplifier is shown in Fig. 2.54. We can define a differential gain ($A_d = A_2 - A_1$) and a common-mode gain ($A_c = A_1 + A_2/2$). An important parameter is the CMRR which is the ratio of common-mode gain to the differential-mode gain. This parameter is used to measure the performance of the differential amplifier. The differential circuit proposed is shown in Fig. 2.55. In this case the gain of mode-common is about $R_D/2R_1 + R_s + r_s$, while the differential gain is about $R_d/R_s + r_s$.

The circuit proposed in Fig. 2.50 is analyzed with P-spice simulator. We consider separately two principal blocks:

- The network $R_1 - C_1$
- The network of the feedback resistor

Feedback resistor has been regulated so as to obtain a gain of about 100. The maximum gain that the circuit can give is about 200. It is not recommended to use a potentiometer for adjusting the gain because it introduces noise to the system (Fig. 2.56).

The network $R_1 - C_1$ has the feature to adjust the band of the system; by varying R_1 and having constant at 10 nF C_1 , we have obtained a series of curves that represented the response curve of the system in frequency (Fig. 2.57). Similar tests with R_1 constant at 10 ohms, and C_1 variable (Fig. 2.58).

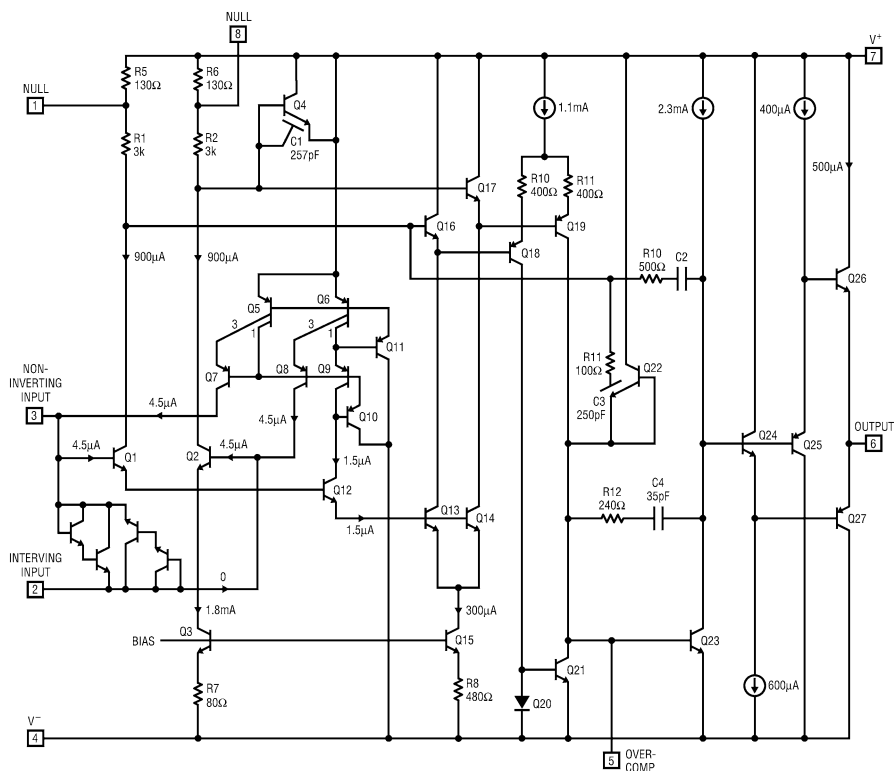


Fig. 2.53 The internal structure of the LT1128 [15]

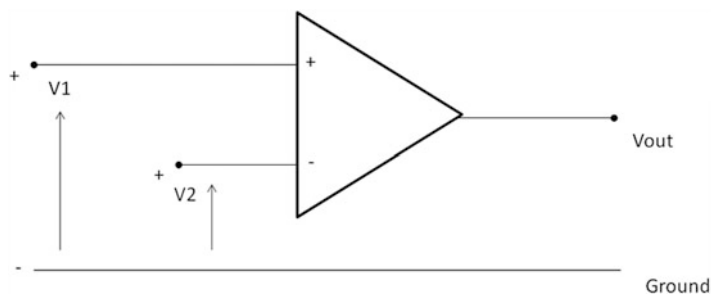


Fig. 2.54 Differential amplifier

The flexibility of the system can facilitate the choice of the response in frequency (Figs. 2.59, 2.60 and 2.61). The response curve of the system as function of the noise is shown in Fig. 2.62. The noises of internal current and voltage of the amplifiers depend on the intrinsic physical phenomena and are by their nature random, aperiodic, and uncorrelated. Typically have a distribution of amplitude of

Fig. 2.55 Differential circuit (JFET)

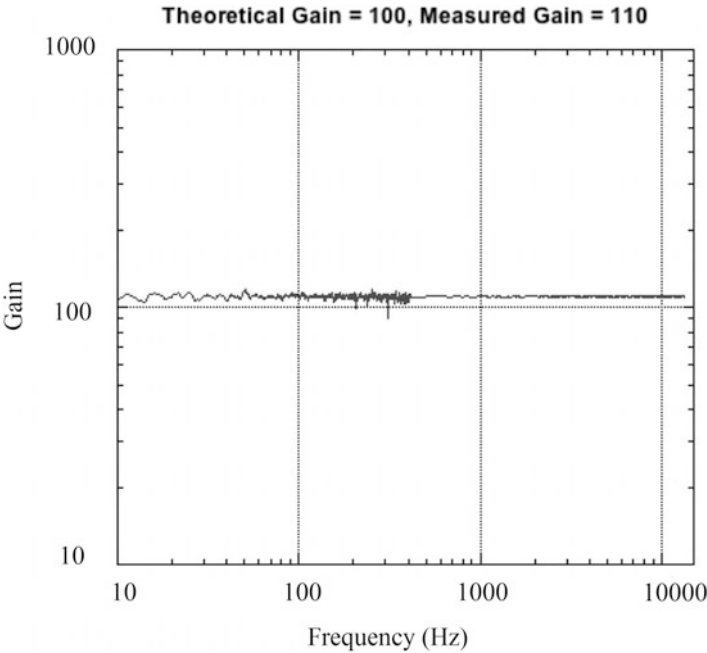
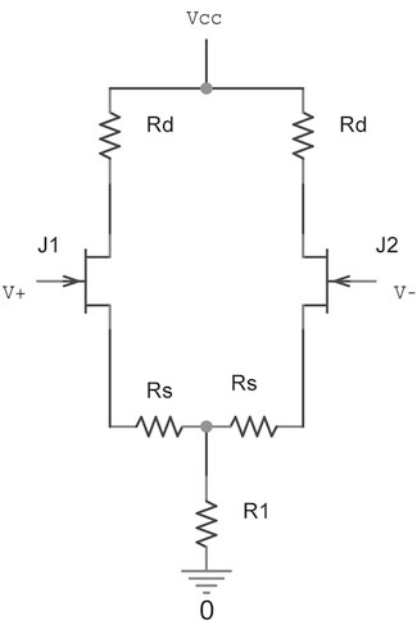


Fig. 2.56 Transfer function

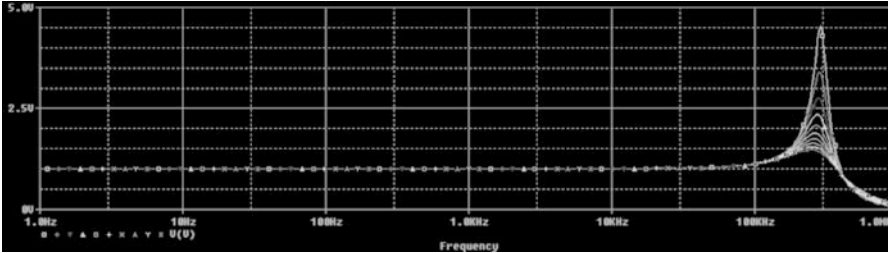


Fig. 2.57 Frequency response: R_1 variable and C_1 fixed

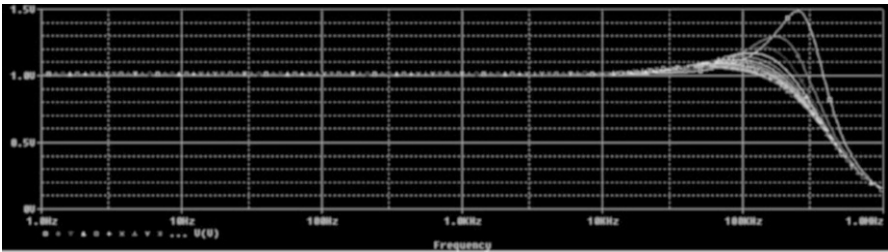


Fig. 2.58 Frequency response: R_1 fixed e C_1 variable

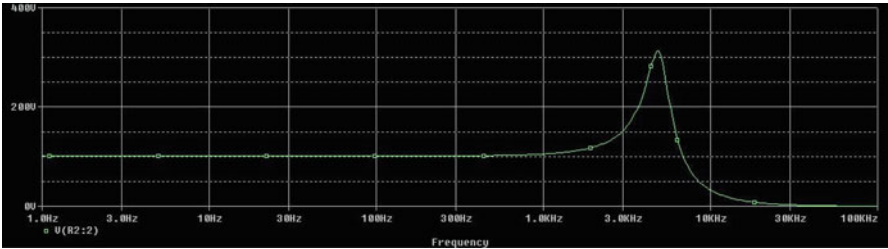


Fig. 2.59 Frequency response: $R_1 = 15 \, \Omega$, $C_1 = 100 \, \text{nF}$ ($G = 100$)

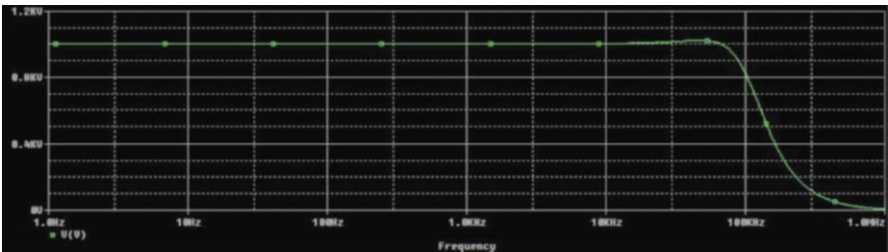


Fig. 2.60 Frequency response: $R_1 = 100 \, \Omega$, $C_1 = 10 \, \text{nF}$ ($G = 100$)

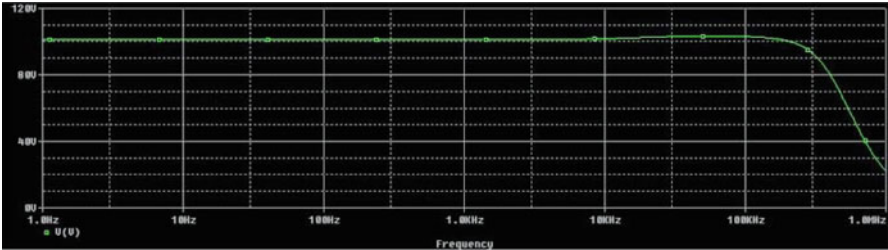


Fig. 2.61 Frequency response: $R_1 = 1\text{ k}\Omega$, $C_1 = 10\text{ nF}$ ($G = 100$)

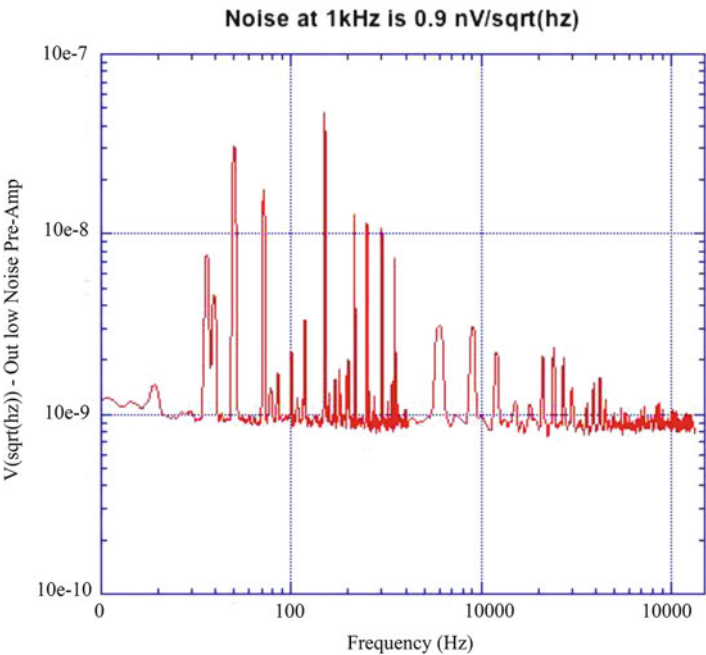


Fig. 2.62 System noise

Gaussian. The relationship between the peak to peak value and the effective value of these components is statistical. A possible qualitative rule is that the RMS value multiplied by 6 does not exceed the peak to peak in the 99.73 % of cases. In the evaluation of noise (0.8 nV/Hz to the frequency of about 1 kHz) in the operational is used to report all sources of noise at the input. In Fig. 2.63 the PCB of the circuit (Fig. 2.64) is visualized, and it uses SMD resistive and capacitive components to obtain a mini preamplifier.

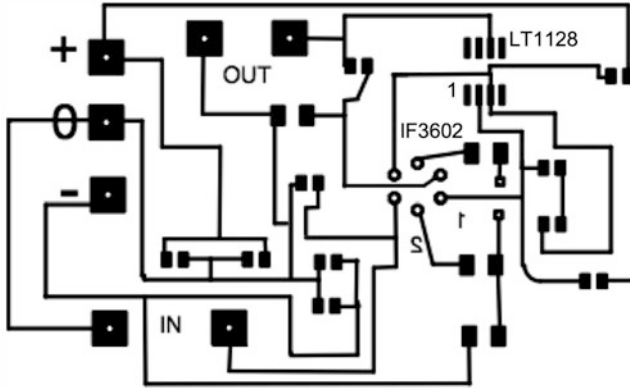


Fig. 2.63 PCB

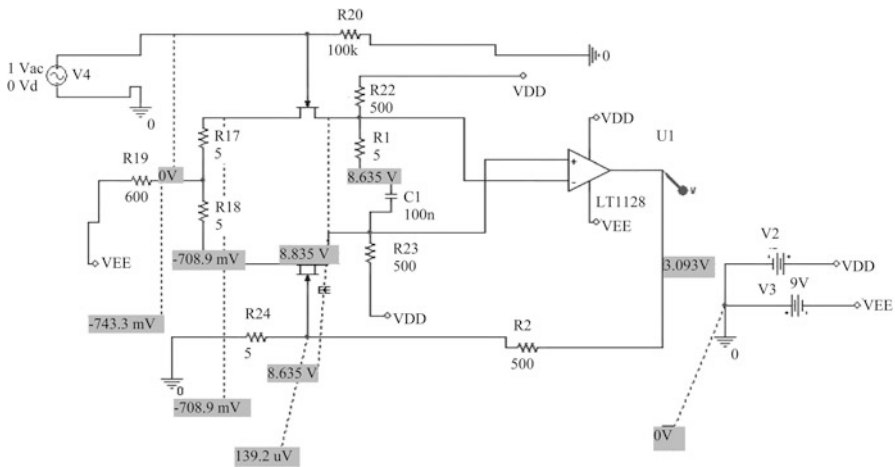


Fig. 2.64 Simulation of the circuit: values of voltages and currents

2.8.2 Low Noise Amplifier of the Maxim Integrated, MAX9632

The MAX9632 (Figs. 2.65, 2.66, 2.67, and 2.68) is a low-noise, precision, wide-band operational amplifier that can operate in a very wide $+4.5\text{ V}$ to $+36\text{ V}$ supply voltage range. The IC operates in dual ($\pm 18\text{ V}$) mode. The IC is designed for extremely low-noise applications such as professional audio equipment, very high performance instrumentations, automated test equipment, and medical imaging. The low noise, combined with fast settling time, makes it ideal to drive high-resolution sigma delta or SARs ADCs. The IC is also designed for ultra-low-distortion performance [16].

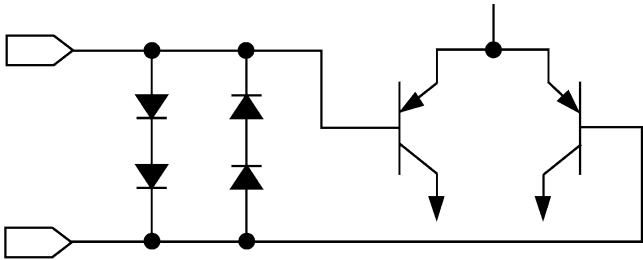


Fig. 2.65 MAX9632: input protection circuit [16]

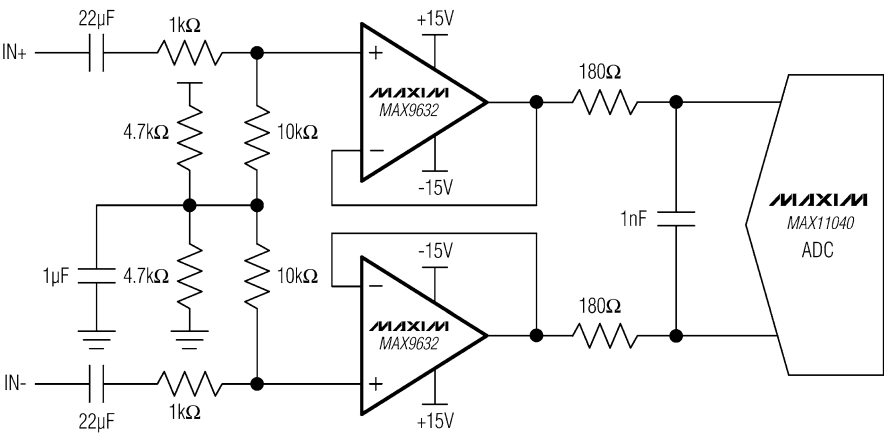


Fig. 2.66 MAX9632: typical application circuit [16]

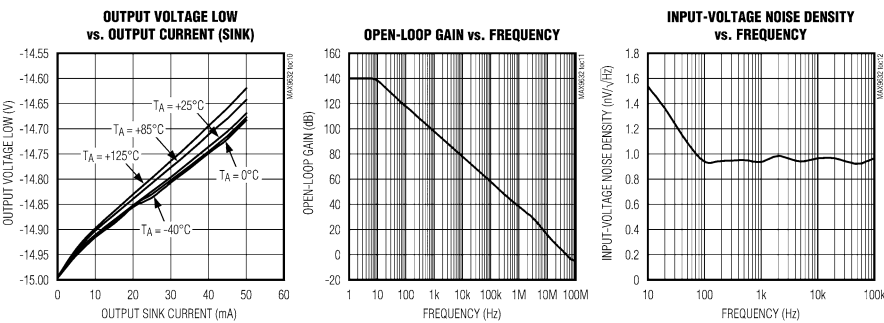


Fig. 2.67 MAX9632: typical operating characteristics [16]

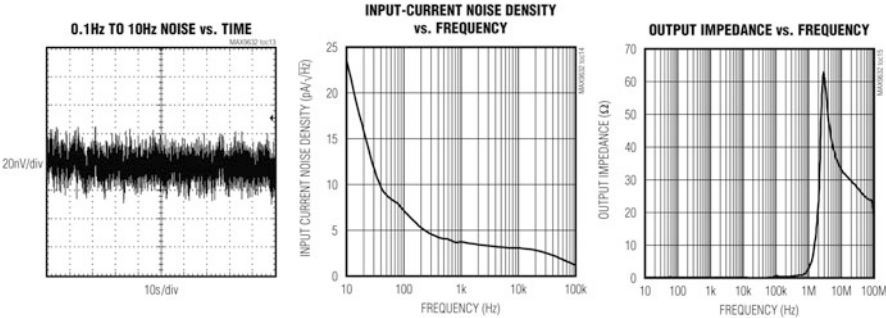


Fig. 2.68 MAX9632: typical operating characteristics [16]

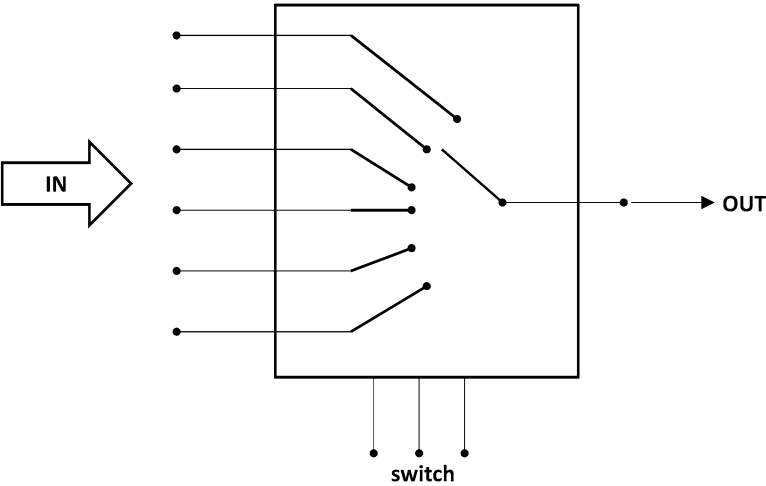


Fig. 2.69 MUX 8x1

2.9 Multiplexer/Demultiplexer

A multiplexer (Figs. 2.69 and 2.70) or data selector (abbreviated MUX) consists of a group of data inputs and a group of control inputs. The control inputs are used to select exactly one data input to be outputted. A MUX with n control inputs can select from a maximum of 2^n data inputs. When $n = 2$, there are $2^2 = 4$ data inputs that can be selected. When $n = 3$, there are $2^3 = 8$ data inputs that can be selected. An 8X1 ($n = 3$) MUX uses three control inputs to select exactly one of eight data inputs to be outputted. The three control inputs are labeled as A, B, and C (Fig. 2.69). On the other hand, a demultiplexer (or demux) is a device that sends in one of many data-output-lines a single input signal and getting out it in one of many data-output-lines [6].

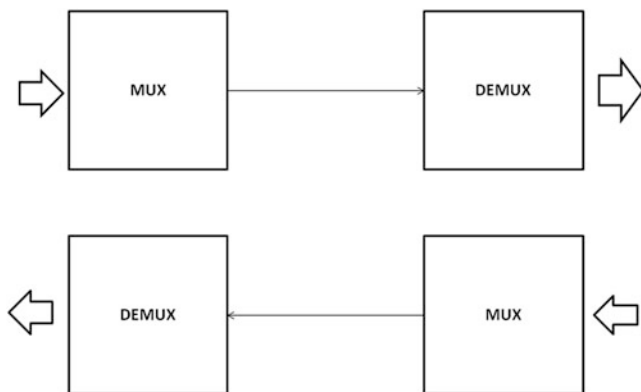


Fig. 2.70 MUX–DEMUX

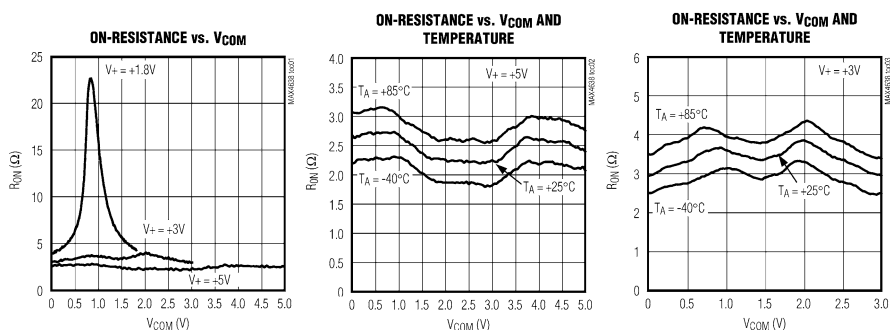


Fig. 2.71 MAX4638/4639: Typical operating characteristics [17]

2.9.1 Multiplexer/Demultiplexer of Maxim Integrated, MAX4638/4639

The MAX4638/MAX4639 (Figs. 2.71, 2.72, 2.73, 2.74, and 2.75) are low-voltage, CMOS analog muxes. The MAX4638 is an 8:1 mux that switches one of eight inputs (NO1–NO8) to a common output (COM) as determined by the 3-bit binary inputs A0, A1, and A2. The MAX4639 is a 4:1 dual mux that switches one of four differential inputs to a common differential output as determined by the 2-bit binary inputs A0 and A1. Both the MAX4638/MAX4639 have an EN input that can be used to enable or disable the device. When disabled all channels are switched off.

A +1.8 V to +5.5 V operating range makes the MAX4638/MAX4639 ideal for battery-powered, portable instruments. All channels guarantee break-before-make switching. All control inputs are TTL/CMOS-logic compatible. Decoding is in standard BCD format, and an enable input is provided to simplify cascading

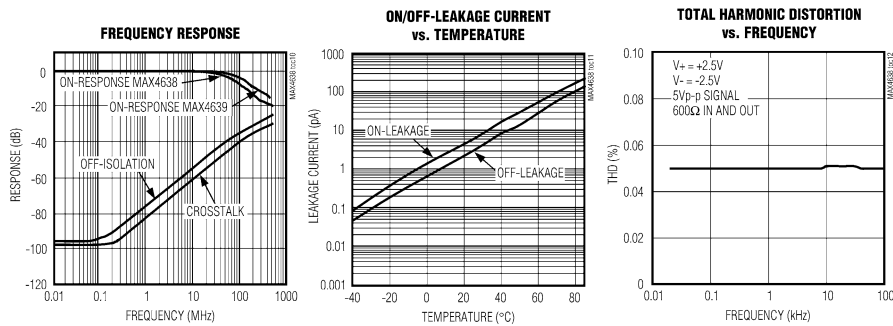


Fig. 2.72 MAX4638/4639: Typical operating characteristics [17]

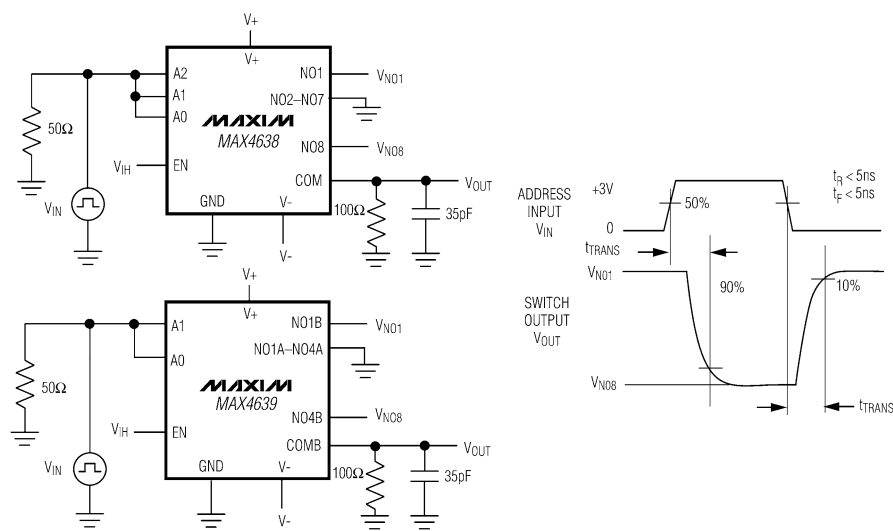


Fig. 2.73 MAX4638/4639: Test circuit and timing diagram (transition time) [17]

of devices. These devices are available in small 16-pin TQFN, TSSOP, and SO packages, as well as a 20-pin TQFN package [17].

Proper power-supply sequencing is recommended for all CMOS devices. Always sequence $V+$ on first, then $V-$, followed by the logic inputs. If power-supply sequencing is not possible, add two small-signal diodes (D1, D2) in series with the supply pins for over voltage protection (Fig. 2.76). Adding diodes reduces the analog signal range to one diode drop below $V+$ and one diode drop above $V-$, but does not affect the devices low switch resistance [17].

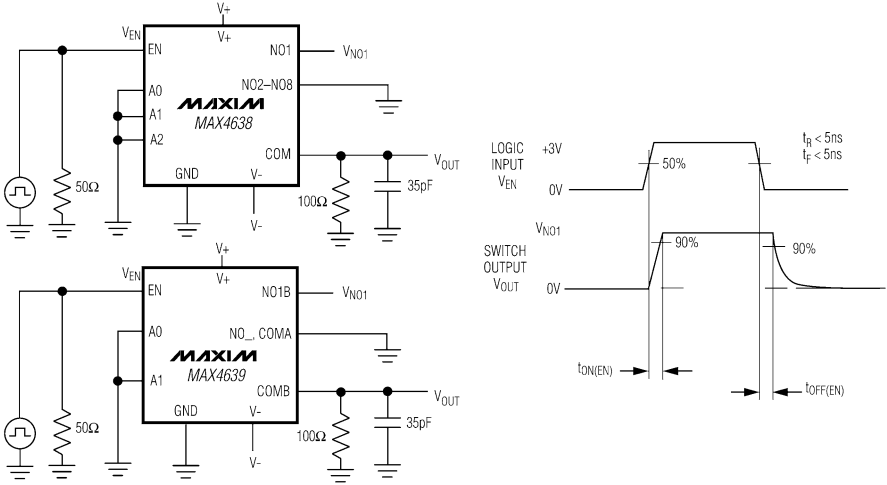


Fig. 2.74 MAX4638/4639: Test circuit and timing diagram (enabling time) [17]

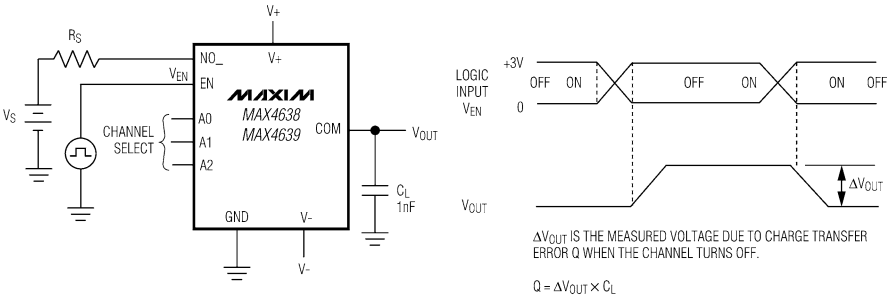
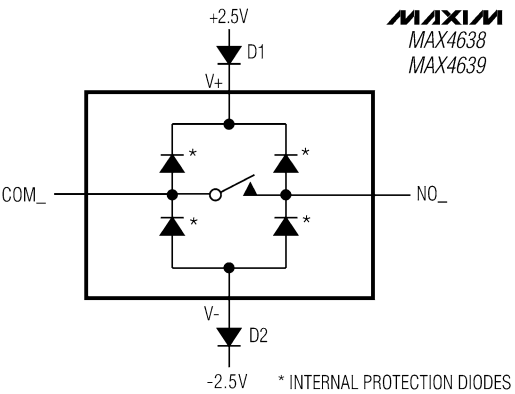


Fig. 2.75 MAX4638/4639: Test circuit and timing diagram (charge injection) [17]

Fig. 2.76 MAX4638/4639:
Over voltage protection using
external blocking diodes [17]



2.10 Power Management

Power management is critical in battery-powered applications. Differences of microamperes can translate into months or years of operating life, which can make or break a product in the marketplace. The single largest factor in power consumption of a microcontroller is clock frequency. The power consumed by a microprocessor is directly proportional to its operating speed, so it follows that a device operating at the lowest possible frequency will produce the maximum power savings. The speed chosen depends on the system requirements, most notably interrupt service time. Temperature can also affect power consumption. The High-Speed Microcontrollers support four clock management modes: Stop, PMM1 (Power Management Mode 1), PMM2 (Power Management Mode 2), and Idle. They can dynamically switch between these modes, allowing the user to optimize the speed of the device while minimizing power consumption.

Power Management Mode 1 (PMM1) allows the user to run at a reduced speed to save power. Setting the clock divider rate bits will force the part from its default 4 clocks per machine cycle (divide by 4) to 64 clocks per machine cycle (divide by 64). The external crystal continues to operate at full speed. All peripherals and instructions will operate at this reduced speed. The microcontroller can resume divide by 4 operation by setting the appropriate clock divider rate bits or by utilizing the switchback feature.

Power Management Mode 2 (PMM2) allows the user to run at an even slower speed to improve power savings. Setting the clock divider rate bits will force the part from its default 4 clocks per machine cycle (divide by 4) to 1,024 clocks per machine cycle (divide by 1,024). The external crystal continues to operate at full speed. All peripherals and instructions will operate at this reduced speed. The microcontroller can resume full-speed (divide by 4) operation by setting the appropriate clock divider rate bits or by utilizing the switchback feature. This mode permits an even greater power savings over PMM1.

The Stop mode is the lowest power state available. While in this mode the crystal oscillator is stopped, and all internal clocking, including the Watchdog Timer, is halted. The real time clock is unaffected by Stop mode. The Stop mode is exited by an external interrupt, real-time clock interrupt, an external reset via the RST pin, or a power-on reset. Each interrupt will cause the device to vector to the corresponding interrupt routine to resume execution.

The Idle mode halts operation of the microcontroller processor core but leaves internal clocks, serial ports, and timers running. Use of this mode is not recommended on new designs, as lower power operation can be achieved by placing the part in PMM2 and executing NOPs. Its inclusion provides backward software compatibility [19].

The greatest power savings come from utilizing the power management modes. Unlike other techniques, Power Management Modes 1 and 2 (PMM1 and PMM2) allow the user to reduce power consumption without sacrificing performance. Although the power management features are an important part of a power efficient

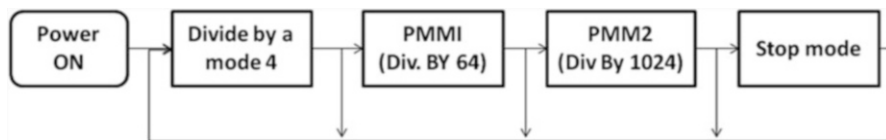


Fig. 2.77 Progression of clock speed modes

design, a thorough understanding of the microprocessor will allow the system designer to achieve maximum power savings. The clock speed management modes are designed to be part of a progressive level of power reduction, based on external activity and performance needs. PMM1 and PMM2 provide the lowest level of power consumption while still permitting full computational and peripheral operation. Figure 2.77 demonstrates the progression of clock management modes. As explained later, transitions between PMM1 and PMM2 must be made through divide by 4 mode [18, 19].

Numerous diverse and conflicting constraints burden the designer of small handheld products. Aside from the customary restrictions on size and weight, these constraints include cost limitations, strict time schedules, battery-life goals measured in weeks instead of hours, and host computers that are (sometimes) overtaxed with the demands of power management [18, 19].

Because power requirements for handheld applications vary widely with product use, no single “best” power source exists for these applications. A device used intermittently is more concerned with no-load quiescent current than with full-load efficiency, and can operate satisfactorily with alkaline batteries. Cell phones, however, must contend with high peak loads and frequent use. This mode of operation emphasizes conversion efficiency over quiescent current, so cell phones are better served with a rechargeable battery.

In handheld product design, size limitations often dictate the number of battery cells early in the process. This is frustrating to the electrical engineer, and a substantial constraint, since the number (and type) of cells allowed determines the operating-voltage range. This, in turn, strongly affects the cost and complexity of the power supply. High cell counts enable the use of linear regulators and simple circuitry at the cost of extra weight and limited efficiency. Low cell counts compel the use of a more costly switching regulator, but the low cost of the battery may justify this expense [18]. A design with four single-cell batteries often provides an attractive compromise between weight and operating life. That number is particularly popular for alkaline batteries because they are commonly sold in multiples of four. Four-cell power for 5 V circuitry presents a design challenge, however. As a battery discharges, the regulator must first step down and then step up. This requirement precludes use of the simpler, one-function regulator topologies that can only step down, step up, or invert. One effective solution to this problem is the single-ended primary inductance converter (SEPIC), in which VOUT is capacitively coupled to the switching circuitry (Fig. 2.78). The absence of

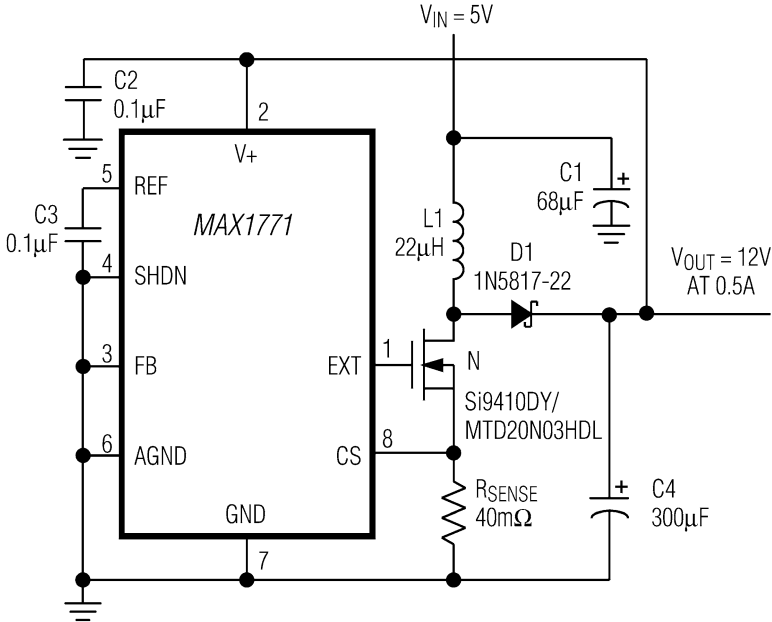


Fig. 2.78 MAX1771 step-up controller [18]

a transformer is one of several advantages that this configuration has over flyback-transformer regulators and combination step-up/linear regulators [18, 19].

2.10.1 Automotive Power-Management MAX16920

The MAX16920 (Figs. 2.79 and 2.80) power-management IC integrates three high-voltage step-down DC–DC converters, one high-voltage linear regulator, and an overvoltage protection block. The MAX16920 is optimized for high efficiency and low standby current. The power dissipation of the MAX16920 is made up of three components: power dissipation due to the DC–DC converters, power dissipation due to the linear regulator, and internal power dissipation [20].

2.10.2 Power-Management ICs for Single-Cell, MAX8662/MAX8663

The MAX8662/MAX8663 highly integrated PMICs are designed for use in smart cellular phones, PDAs, Internet appliances, and other portable devices (Fig. 2.81).

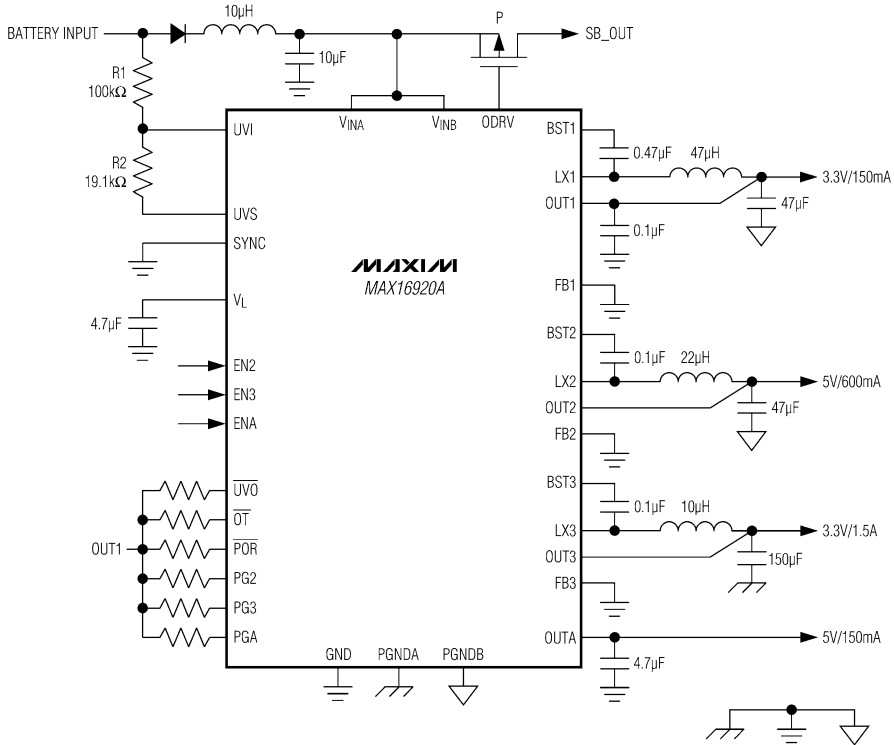


Fig. 2.79 MAX16920: Typical operating circuit [20]

They integrate two synchronous buck regulators, a boost regulator driving two to seven white LEDs (MAX8662 only), four low dropout (LDO) linear regulators, and a linear charger for a single-cell Li+ battery. Figure 2.81 is the block diagram and application circuit. SPS circuitry offers flexible power distribution between an AC adapter or USB source, battery, and system load, and makes the best use of available power from the AC adapter/USB input. The battery is charged with any available power not used by the system load. If a system load peak exceeds the current limit, supplemental current is taken from the battery. Thermal limiting prevents overheating by reducing power drawn from the input source. Two step-down DC–DC converters achieve excellent light-load efficiency and have on-chip soft-start circuitry; 1 MHz switching frequency allows for small external components. Four LDO linear regulators feature low quiescent current and operate from inputs as low as 1.7 V. This allows the LDOs to operate from the stepdown output voltage to improve efficiency. The white LED driver features easy adjustment of LED brightness and open-LED overvoltage protection. A 1-cell Li+ charger has programmable charge current up to 1.25A and a charge timer [21].

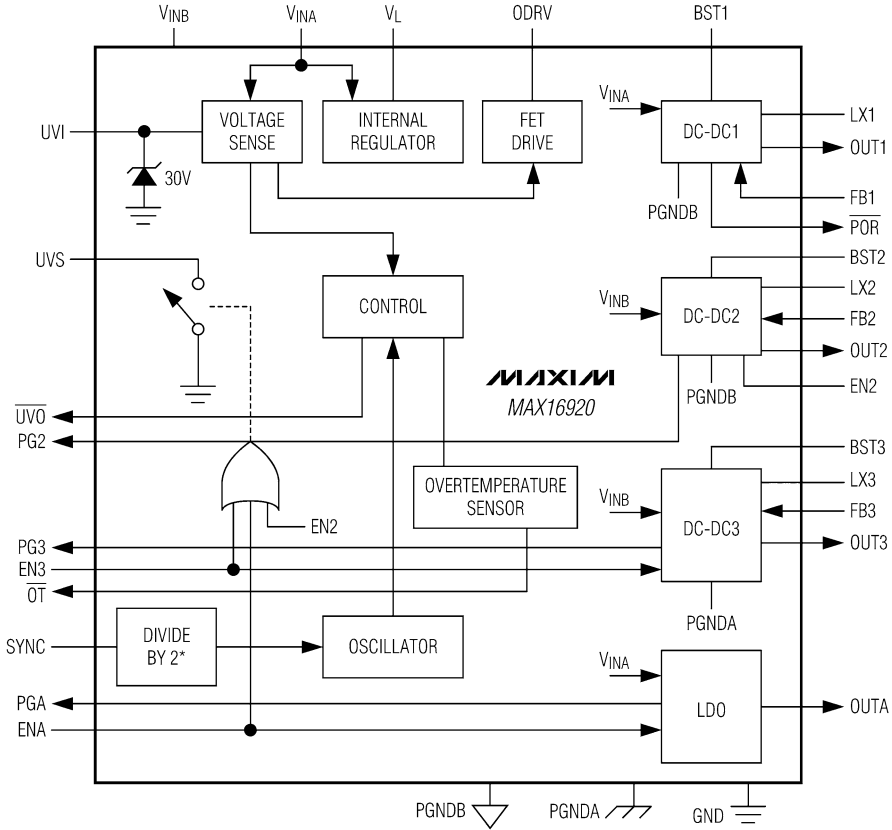


Fig. 2.80 MAX16920: Functional diagram [20]

2.11 Timing System

In the DAQ systems are required the design of timing and synchronization. The timing system management tasks between various electronics stages that required hardware synchronization. Example of timing system can be the following: hand-shaking, phase-lock looping, synchronizing an RF device, and so on. They are based on two main assumptions: all signals are digital and all components share a common and discrete notion of time; it is defined as clock signal located throughout the circuit.

The advantages of asynchronous circuits can be described below:

- Low power consumption
- High operating speed
- Better modularity

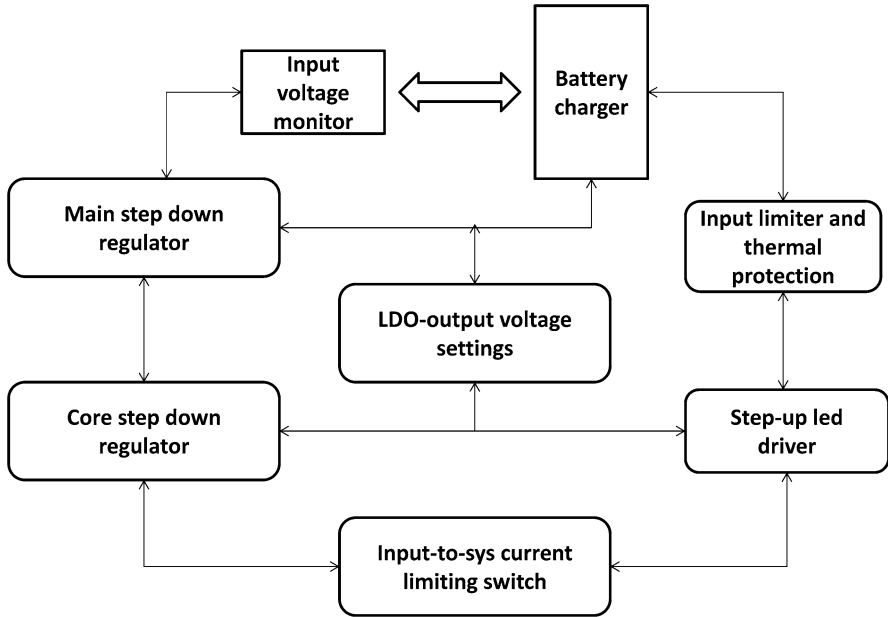


Fig. 2.81 MAX8662/MAX8663: Functional diagram [21]

- Robustness in terms of variations in supply voltage, temperature, and fabrication process parameters.

2.11.1 Timing Parameters for Combinational Logic

Timing characteristics can be defined by Fig. 2.82:

- Propagation delay (t_{pd}): The amount of time needed for a change in a logic input to result in a permanent change at an output.
- Contamination delay (t_{cd}): The amount of time needed for a change in a logic input to result in an initial change at an output [6].

2.11.2 Timing Parameters for Sequential Logic

Timing system with sequential circuits implemented certain timing characteristics that are specified in relation of the clock input.

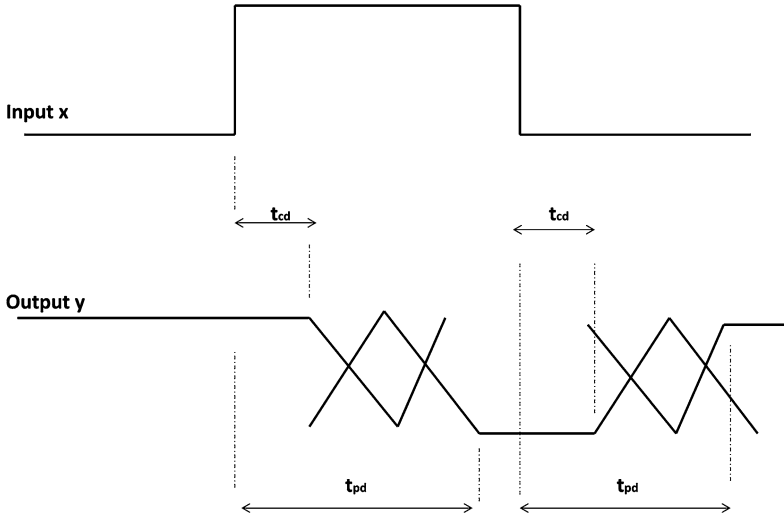


Fig. 2.82 Propagation and contamination delay

Latch vs. Flip-Flop: A latch is level-sensitive while a flip-flop is edge triggered. A latch stores digital data when the clock level is low and doesn't work when the level is high. A flip-flop, instead, stores digital data when the clock rises. Timing characteristics can be specified in relation to the rising (for positive edge-triggered) or falling (for negative-edge triggered) clock edge. In the following text we can specify parameters to explain sequential circuit behavior [7]:

- Propagation delay ($t_{\text{clk-q}}$): Time needed for a change in the flip-flop clock input D to result in a change at the flip-flop output Q .
- Contamination delay (t_{cd}): Time needed for a change in the flip-flop clock input to result in the initial change at the flip-flop output Q .
- Setup time (t_{su}): time before the clock edge that data input D must be stable the rising clock edge arrives.
- Hold time (t_{hold}): time after the clock edge arrives that data input D must be held stable in order for the flip-flop to latch the correct value.

2.11.3 Clock Skew and Clock Jitter

Clock skew is the spatial variation in arrival time of a clock transition (δ). It is a constant from cycle to another and given by $t_j - t_k$, where $t_j - t_k$ is the rising edge of the clock with respect to the reference between two points j and k (Figs. 2.83 and 2.84).

Clock jitter is related to the temporal variation of the clock period; the clock period can increase or reduce on a cycle-by-cycle basis (Fig. 2.85) [22].

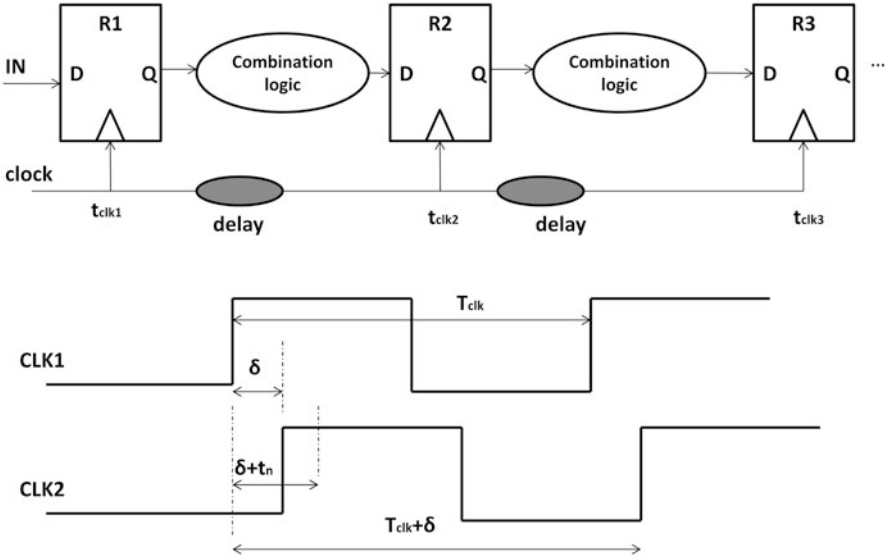


Fig. 2.83 Positive skew

2.11.4 MAX9155-Clock

The MAX9155 (Figs. 2.86 and 2.87) is a low-voltage differential signaling (LVDS) repeater, which accepts a single LVDS input and duplicates the signal at a single LVDS output. Its low-jitter, low-noise performance makes it ideal for buffering LVDS signals sent over long distances or noisy environments, such as cables and backplanes.

The MAX9155's tiny size makes it especially suitable for minimizing stub lengths in multidrop backplane applications. The SC70 package (half the size of a SOT23) allows the MAX9155 to be placed close to the connector, thereby minimizing stub lengths and reflections on the bus. The point-to-point connection between the MAX9155 output and the destination IC, such as an FPGA or ASIC, allows the destination IC to be located at greater distances from the bus connector [23].

2.12 Filtering

The most common filter are the Butterworth, Chebyshev, and Bessel (Figs. 2.88 and 2.89) types. Many other types are available, but 90 % of all applications can be solved with one of these three. Butterworth ensures a flat response in the pass-band and an adequate rate of roll-off; it is simple to understand and suitable for

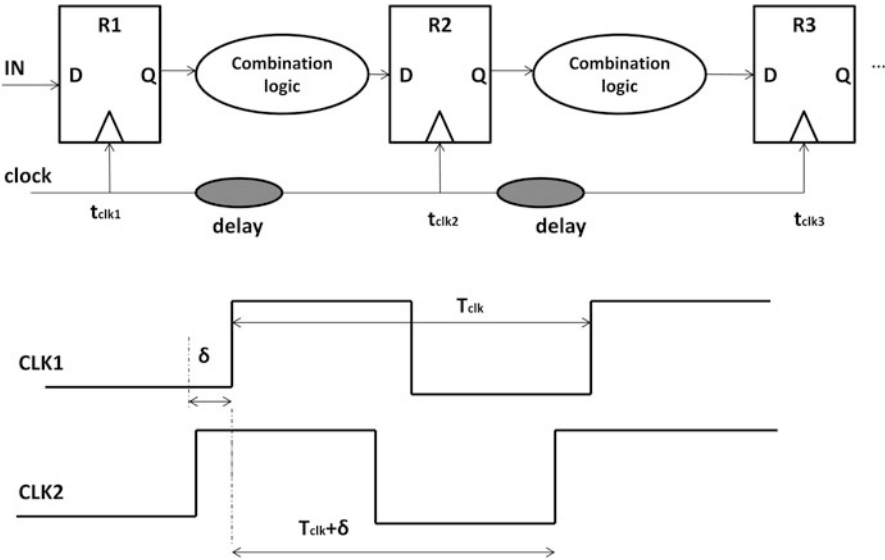


Fig. 2.84 Negative skew

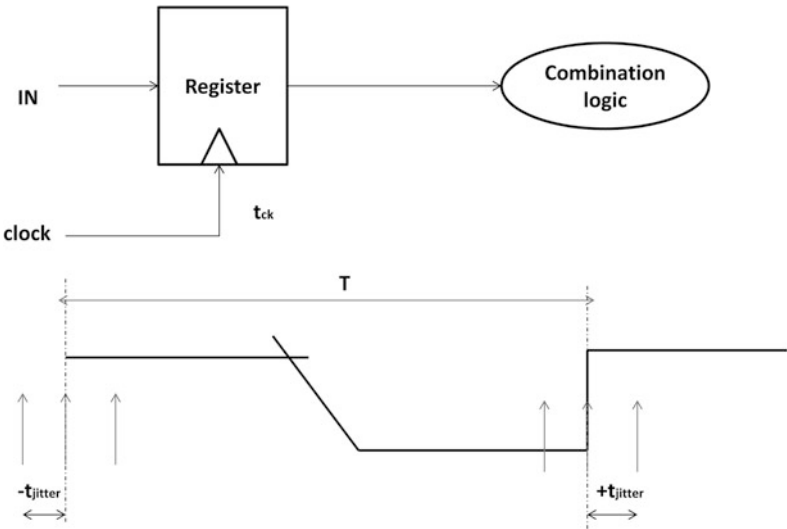


Fig. 2.85 Clock jitter

Fig. 2.86 Transition time and propagation delay test circuit [23]

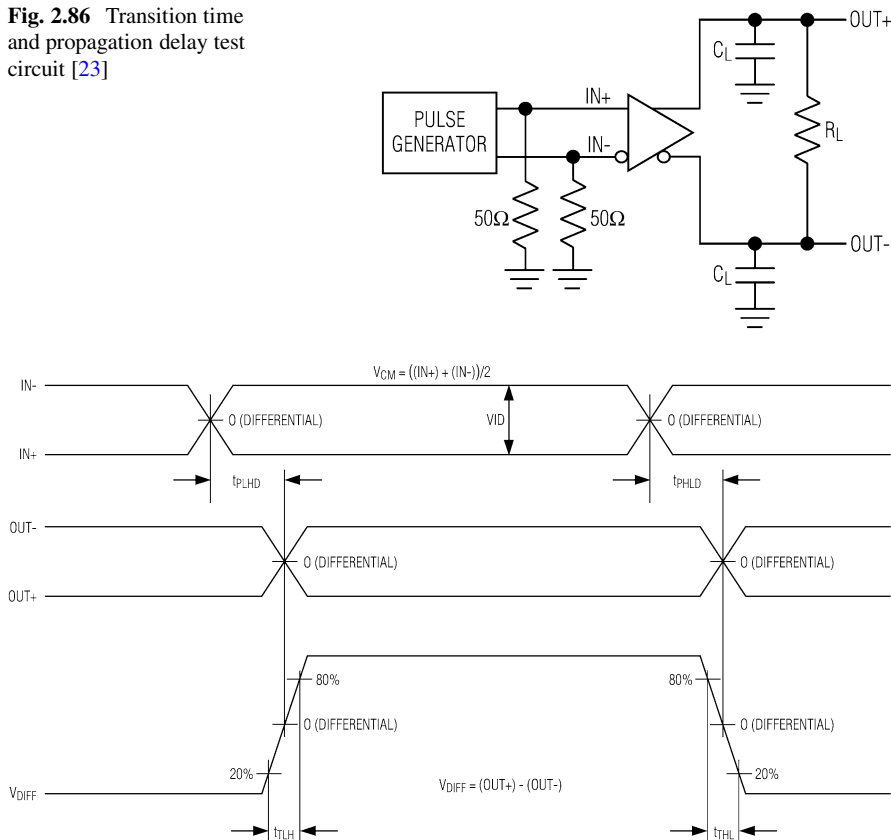


Fig. 2.87 Transition time and propagation delay timing diagram [23]

applications such as audio processing. The Chebyshev gives a much steeper roll-off, but pass-band ripple makes it unsuitable for audio systems. It is superior for applications in which the pass-band includes only one frequency of interest (e.g., the derivation of a sine wave from a square wave, by filtering out the harmonics). The Bessel filter gives a constant propagation delay across the input frequency spectrum. Therefore, applying a square wave (consisting of a fundamental and many harmonics) to the input of a Bessel filter yields an output square wave with no overshoot (all the frequencies are delayed by the same amount). Other filters delay the harmonics by different amounts, resulting in an overshoot on the output waveform. One other popular filter, the elliptical type, is a much more complicated filter that will not be discussed in this text. Similar to the Chebyshev response, it has ripple in the pass-band and severe roll-off at the expense of ripple in the stop-band [24].

In the Fig. 2.90 some examples of low-pass, high-pass, and generic filter design. Digital filters are algorithms used for digital computers. It is a linear operation

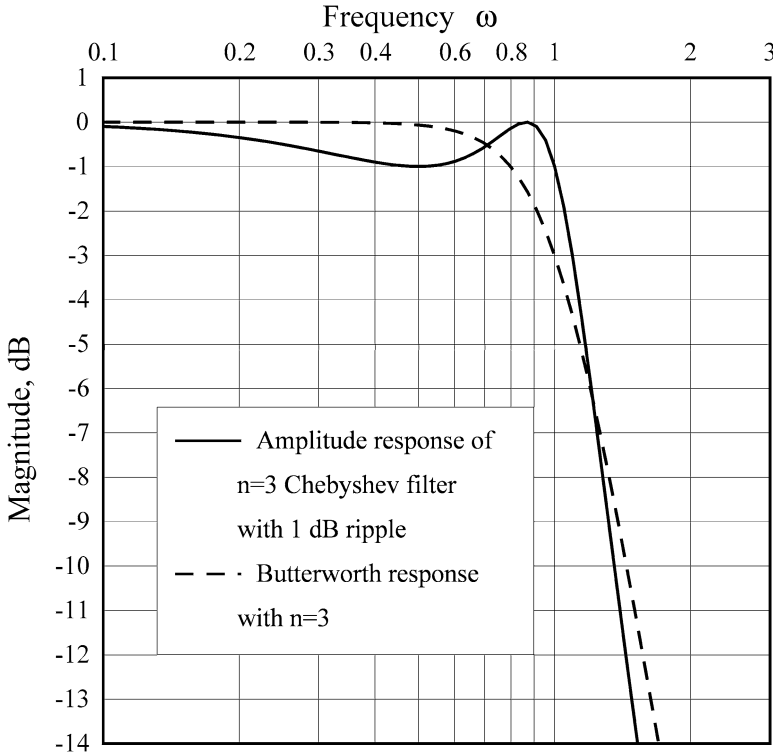


Fig. 2.88 Amplitude responses of third order filters ($n = 3$). Chebyshev filter in *boundary line*, Butterworth filter in *dashed line*

completed on sampled data. The main operations that includes are the following: smoothing (averaging), integrating, separating signals (filtering), and predicting.

Digital filters can be compared to analog filters. For example, low-pass have their digital equivalent but they have additionally some important features which make them well suited for digital communication system. Digital filters can be programmed and there are no impedance-matching problems and can have memories if required

2.12.1 Digitally Programmed, Dual Second-Order Continuous Low-Pass Filter, MAX270/271

The MAX270/MAX271 (Figs. 2.91 and 2.92) are digitally programmed, dual second-order continuous-time low-pass filters. Their typical dynamic range of 96 dB surpasses most switched capacitor filters which require additional filtering to remove clock noise. The MAX270/MAX271 are ideal for anti-aliasing and DAC

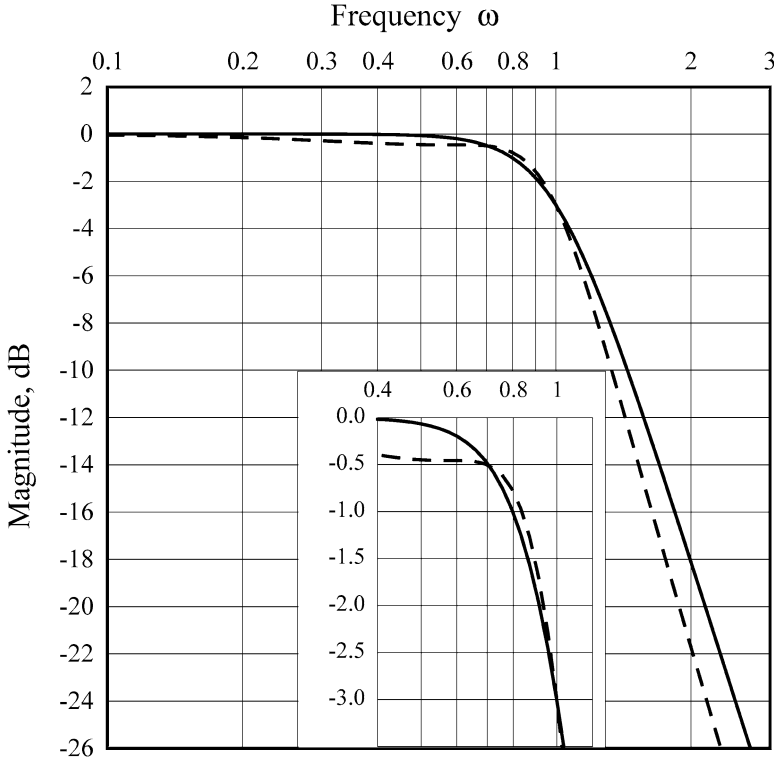


Fig. 2.89 Amplitude responses of Butterworth filter of order 3 (*solid line*) and optimum filter of order 3 (*dashed line*)

smoothing applications and can be cascaded for higher-order responses. Cutoff frequencies in the 1–25 kHz range can be selected [25].

Cut-Off Frequency: Cut-off frequency f_c is the frequency of 3 dB attenuation in the filter response. According to the data value in pin D0–D6, cut-off frequency is programmed from 1 to 25 kHz. The equations for calculating of f_c from the programmed code are as follows:

$$f_c = \frac{87.5}{87.5 - \text{CODE}} * 1 \text{ kHz} \quad (2.6)$$

with CODE: 0–63, and

$$f_c = \frac{262.5}{137.5 - \text{CODE}} * 1 \text{ kHz} \quad (2.7)$$

with CODE: 64–127. where CODE is the data on pins D0–D6 (0–127). D6 is the most significant bit (MSB) [25].

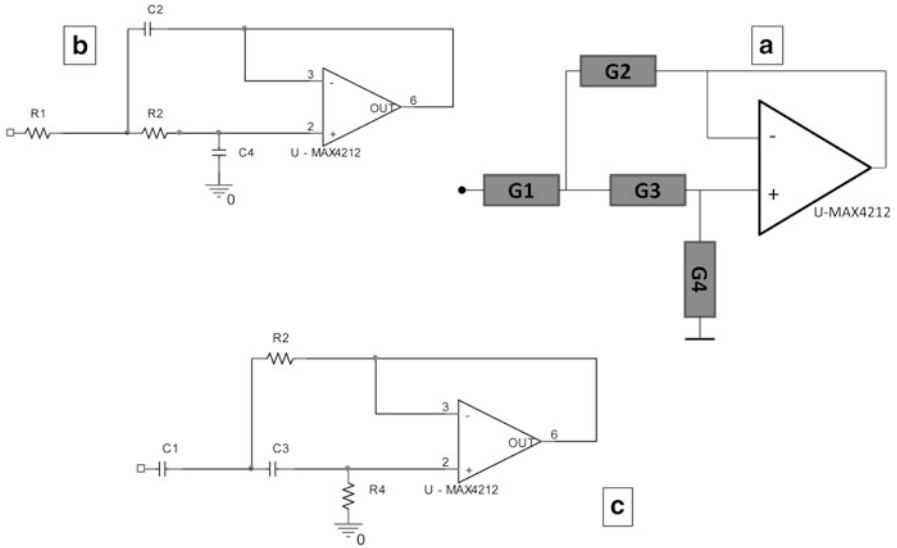
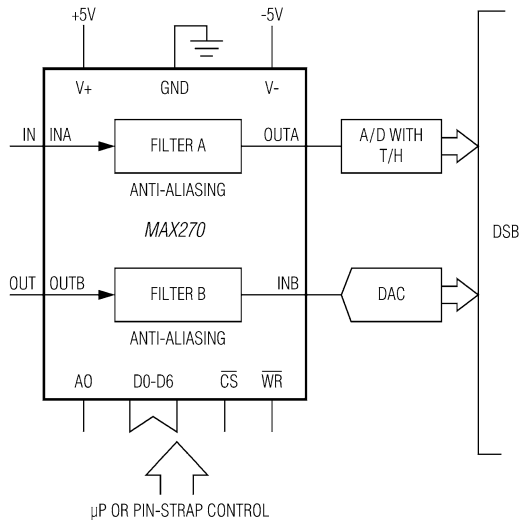


Fig. 2.90 Generic filter block (a), a low-pass filter (b), and a high-pass filter (c) [24]

Fig. 2.91 Typical circuit application [25]



2.13 Memory Board

Modern microprocessors can manage a huge amount of data in short time; for that they need that data are processed to the same speed.

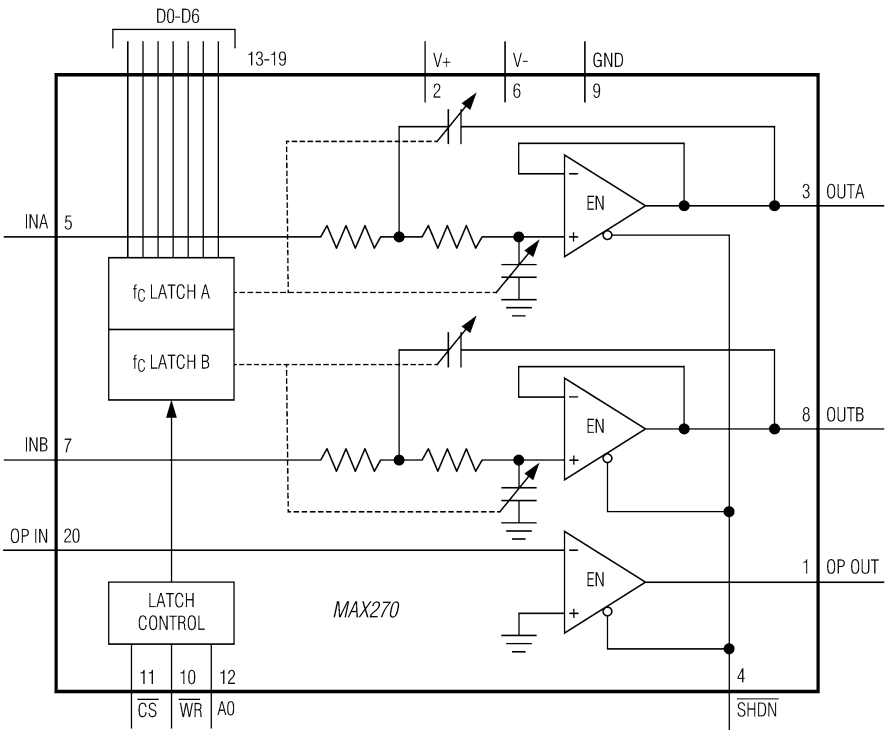


Fig. 2.92 MAX270 block diagram [25]

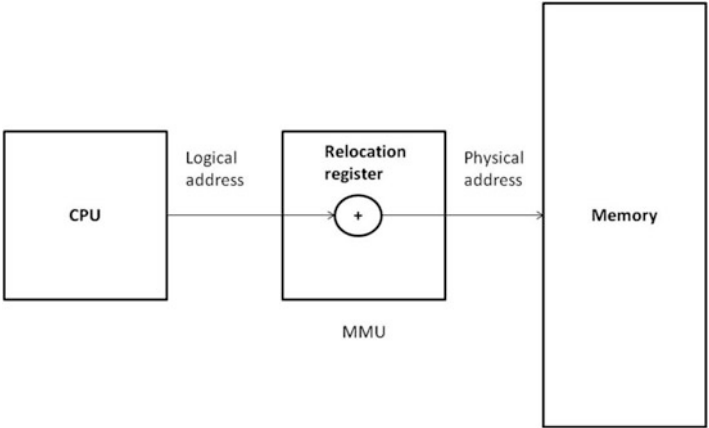
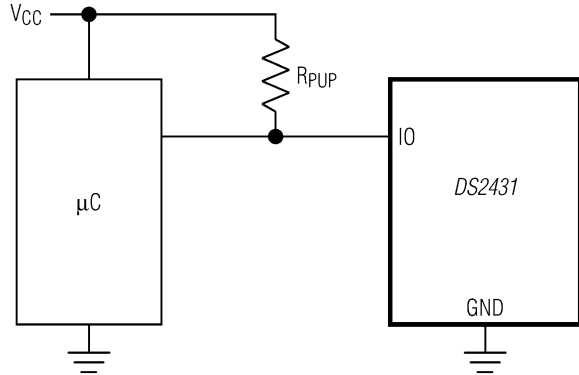


Fig. 2.93 Memory management

Memory is a large array of bytes, each with its own address. CPU fetches instructions that may cause loading from and storing to specific memory address. A instruction-execution cycle can be composed of:

Fig. 2.94 DS2431, typical application [26]



- Fetches an instruction from memory
- Decodes an instruction
- Fetches operands from memory
- Executes the instruction on the operands
- Stores results back in memory

Basic operation cycle of a computer is defined as instruction cycle, sometimes called fetch-and-execute cycle. This cycle is repeated continuously by the CPU, from bootup to when the computer is shut down. Memory management (Fig. 2.93) is the process of computer memory. The main requirement of memory management is to provide ways to dynamically allocate area of memory to programs at their request, and freeing it when is request. This operation is critical to the computer system. Several methods have been devised that increase the effectiveness of memory management. Virtual memory is a method of decoupling the memory from physical hardware. It permits the separation of processes increasing the efficiency of the memory. Its goal is translate the virtual address to a physical address.

In this way addition of virtual memory enables control over memory systems and methods of access:

Protection: It is used to disable a read and write process to memory that is not allocated to it.

Sharing: It is used for inter-process communication [6].

2.13.1 1024-Bit, 1-Wire EEPROM of Maxim Integrated

The DS2431 (Figs. 2.94 and 2.95) is a 1024-bit, 1-Wire EEPROM chip organized as four memory pages of 256 bits each. Data are written in an 8-byte scratchpad, verified, and then copied to the EEPROM memory. As a special feature, the four memory pages can individually be right-protected or put in EPROM-emulation mode, where bits can only be changed from a 1 to a 0 state. The DS2431

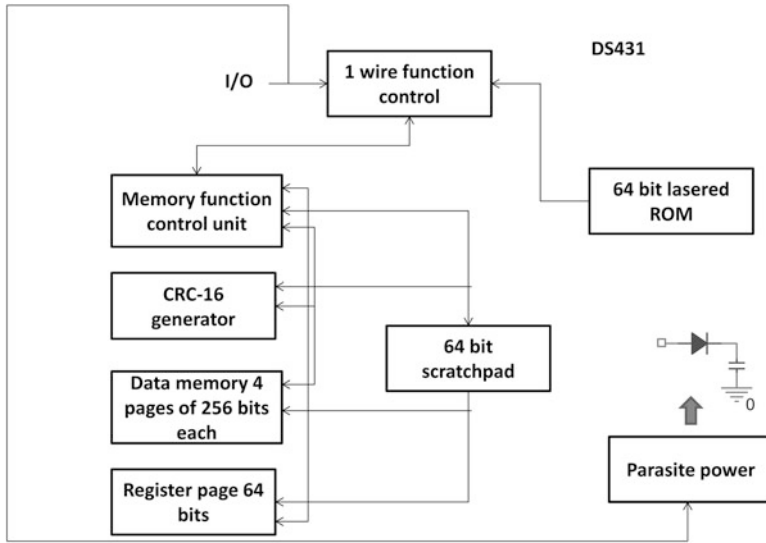


Fig. 2.95 DS2431, block diagram [26]

communicates over the single-conductor 1-Wire bus. The communication follows the standard 1-Wire protocol. Each device has its own unalterable and unique 64-bit ROM registration number that is factory laser-red into the chip. The registration number is used to address the device in a multidrop, 1-Wire net environment [26].

2.14 Bus Interface

A system bus is a device that connects several components of a electronic system. This technique was developed to reduce costs and improve modularity. The goal is based on management of data bus and address bus to determine what and where data must be sent; moreover, a control bus determine its operation.

According to the Figs. 2.96 and 2.97, data are moved from several electronic devices by means of buses.

Buses are designed in one of the following three ways:

- Point to point connection: a particular bus is designed for every transfer.
- Common bus: a common bus is used for all transfers.
- Multiple bus: it is a combination of the previous two methods.

The goal of the bus is to connect CPU and memory; it represents the main characteristics of the system.

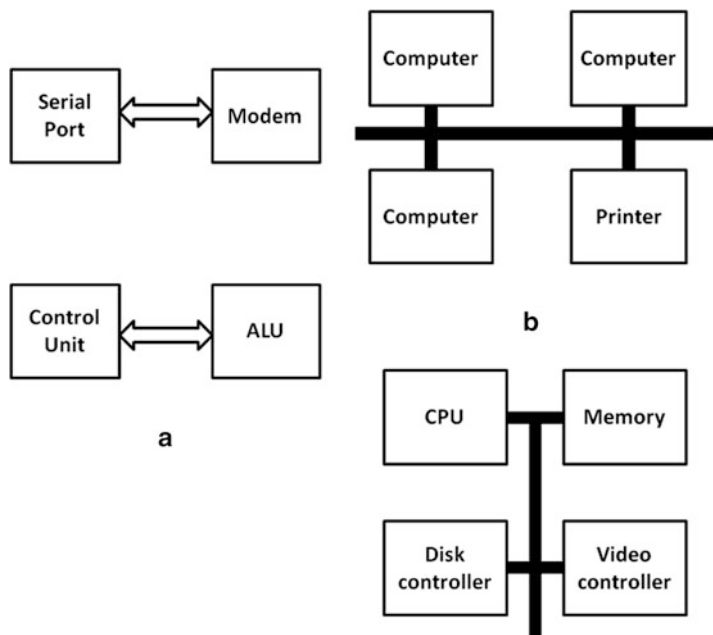


Fig. 2.96 Example of point-to-point buses (a) and multi-point buses (b)

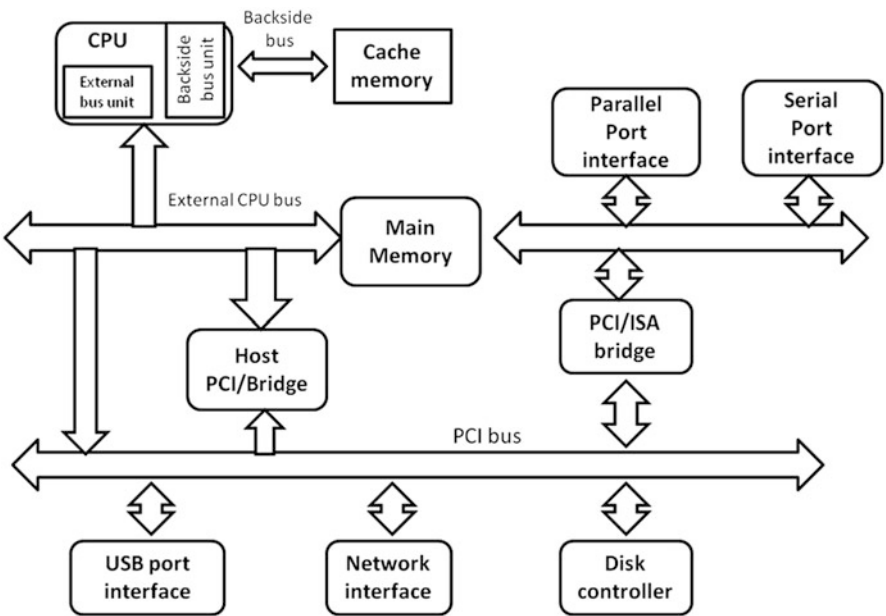


Fig. 2.97 Bus interface

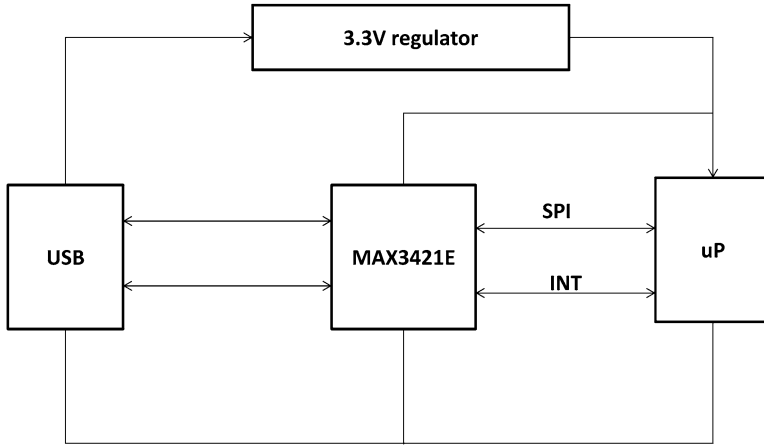


Fig. 2.98 MAX3421E, typical application [27]

Many CPUs use a set of pins for communicating with memory, but are able to operate at different speeds with different protocols. Others use smart controllers to send the data directly in memory, and this is known as direct memory access. Moreover, most modern systems combine both solutions.

In modern systems high speed memory is built directly into the CPU, known as cache, using high-performance buses that operate at speed much greater than memory.

Such systems are architecturally more similar to multicomputers [6].

2.14.1 MAX3421E, USB Peripheral/Host Controller with SPI Interface

The MAX3421E (Fig. 2.98) USB peripheral/host controller contains the digital logic and analog circuitry necessary to implement a full-speed USB peripheral or a full-/low-speed host compliant to USB specification rev 2.0. An internal serial interface engine (SIE) handles low-level USB protocol details such as error checking and bus retries.

The MAX3421E makes the vast collection of USB peripherals available to any microprocessor, ASIC, or DSP when it operates as a USB host. For point-to-point solutions, for example, a USB keyboard or mouse interfaced to an embedded system, the firmware that operates the MAX3421E can be simple since only a targeted device is supported [27].

References

1. Park J, Mackay S (2003) Practical data acquisition for instrumentation and system control. Elsevier, Oxford
2. Lacanette K (1997) Temperature Sensor Handbook - Application Note National Semiconductor Corporation
3. National Instruments (2002) Data Acquisition Fundamentals, Application Note 007, National Instruments Corporation
4. National Instruments (1997) Signal conditioning fundamentals for PC-based data acquisition systems, Application Note 048, National Instruments Corporation
5. Taylor J (1986) Computer-Based Data Acquisition System - Instrument Society of America
6. Wikipedia - http://en.wikipedia.org/wiki/Analog-to-digital_converter - Wikimedia Foundation, Inc.
7. Vandoren A (1982) Data Acquisition System - Reston, Va. Reston Pub. Co.
8. Maxim Integrated (2012) Data sheet of DS1843 - Maxim Integrated. Copyright Maxim Integrated Products (<http://www.maxim-ic.com>). Used by permission
9. Maxim Integrated (2010) Understanding flash ADC - Maxim Integrated. Copyright Maxim Integrated Products (<http://www.maxim-ic.com>). Used by permission
10. Maxim Integrated (1996) Data sheet of MAX1150 - Maxim Integrated. Copyright Maxim Integrated Products (<http://www.maxim-ic.com>). Used by permission
11. Maxim Integrated (2001) Deglitching techniques for high-voltage R-2R DACs - Maxim Integrated. Copyright Maxim Integrated Products (<http://www.maxim-ic.com>). Used by permission
12. Maxim Integrated (2005) Data sheet of MAX5109 - Maxim Integrated. Copyright Maxim Integrated Products (<http://www.maxim-ic.com>). Used by permission
13. Maxim Integrated (2008) Data sheet of MAX5893 - Maxim Integrated. Copyright Maxim Integrated Products (<http://www.maxim-ic.com>). Used by permission
14. Maxim Integrated (2011) Data sheet of MAXQ612/MAXQ622 - Maxim Integrated. Copyright Maxim Integrated Products (<http://www.maxim-ic.com>). Used by permission
15. Linear Tech. Corp. (1992) Data sheet of LT1128 - Linear Tech. Corp. Used by permission
16. Maxim Integrated (2011) Data sheet of MAX9632 - Maxim Integrated. Copyright Maxim Integrated Products (<http://www.maxim-ic.com>). Used by permission
17. Maxim Integrated (2012) Data sheet of MAX4638/4639 - Maxim Integrated. Copyright Maxim Integrated Products (<http://www.maxim-ic.com>). Used by permission
18. Maxim Integrated (2001) Using power management with high-speed microcontrollers - Maxim Integrated. Copyright Maxim Integrated Products (<http://www.maxim-ic.com>). Used by permission
19. Maxim Integrated (2011) Energy management for small portable systems - Maxim Integrated. Copyright Maxim Integrated Products (<http://www.maxim-ic.com>). Used by permission
20. Maxim Integrated (2011) Data sheet of MAX16920 - Maxim Integrated. Copyright Maxim Integrated Products (<http://www.maxim-ic.com>). Used by permission
21. Maxim Integrated (2010) Data sheet of MAX8662/MAX8663 - Maxim Integrated. Copyright Maxim Integrated Products (<http://www.maxim-ic.com>). Used by permission
22. Rabaye JM, Chandrakasan A, Nikolic B (2003) Digital Integrated Circuits 2nd - Prentice Hall
23. Maxim Integrated (2001) Data sheet of MAX9155 - Maxim Integrated. Copyright Maxim Integrated Products (<http://www.maxim-ic.com>). Used by permission
24. Maxim Integrated (2003) Tutorial, analog filter design demystified - Maxim Integrated. Copyright Maxim Integrated Products (<http://www.maxim-ic.com>). Used by permission

25. Maxim Integrated (2012) Data sheet of MAX270/MAX271 - Maxim Integrated. Copyright Maxim Integrated Products (<http://www.maxim-ic.com>). Used by permission
26. Maxim Integrated (2012) Data sheet of DS2431 - Maxim Integrated. Copyright Maxim Integrated Products (<http://www.maxim-ic.com>). Used by permission
27. Maxim Integrated (2007) MAX3421E, USB peripheral/host controller with SPI interface - Maxim Integrated. Copyright Maxim Integrated Products (<http://www.maxim-ic.com>). Used by permission



<http://www.springer.com/978-1-4614-4213-4>

Data Acquisition Systems
From Fundamentals to Applied Design
Di Paolo Emilio, M.
2013, XVII, 135 p., Hardcover
ISBN: 978-1-4614-4213-4