

## Chapter 2

# Converter Topologies and Fundamentals

To build a solid understanding of the capacitive conversion technique, this chapter introduces the fundamental characteristics of capacitive DC–DC converters in Sect. 2.1. Section 2.2 discusses three different analysis techniques: Charge Flow Analysis, Charge Balance Analysis and Branch Analysis. These complementary techniques have their specific merit in the development of the state-of-the-art capacitive DC–DC converter modeling techniques (Chap. 3) and are used for analyzing capacitive DC–DC converters. Charge Flow Analysis demonstrates an intuitive method to determine the VCR of capacitive converters. Charge Balance Analysis builds a bridge between the conventional switched-capacitor analysis and the analysis of capacitive DC–DC converters. Branch Analysis presents a generalized technique to analyze and to qualify the topology performance. Next the converter taxonomy is discussed in Sect. 2.3 and finally the analysis techniques are demonstrated for a selection of capacitive DC–DC converter topologies in Sect. 2.4.

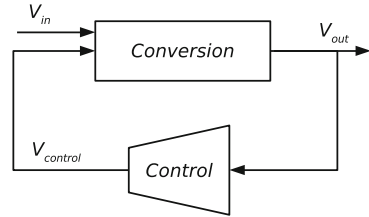
### 2.1 Characteristics

DC–DC conversion by means of capacitors differs fundamentally from an inductive DC–DC converter. The most notable difference is that lossless conversion can only be achieved at infinitely high switching frequencies or by a converter with an infinitely large amount of capacitance. In practice a properly designed capacitive DC–DC converter faces only a small efficiency penalty for violating these requirements. To make this more tangible, this section offers a first look into the principles and the operation of a primitive capacitive DC–DC converter.

#### 2.1.1 DC–DC Converter Structure

A capacitive DC–DC converter consists of the two parts in Fig. 2.1: the conversion block and the control block. The conversion block is the heart of the converter and

**Fig. 2.1** Graphical representation of the coarse converter system partitioning: the conversion block performs the DC–DC conversion and the control block controls the behavior of the conversion block



performs the actual conversion between the DC input voltage and the DC output voltage. The control block is a signal processing system that manipulates the behavior of the conversion block in order to keep it in line with the system requirements, it is discussed in Chap. 5.

There is a clear difference in nature between both blocks. The conversion block is the so-called power stage and embodies the low impedance part of the DC–DC converter. The control part is a high impedance feedback path of the conversion characteristics (output voltage, output current,...) to at least one of the control parameters of the conversion block (switching frequency, duty cycle of the switching frequency,...).

A DC–DC converter can operate without a closed control loop. This is done in case there is no power budget for the control loop circuitry or in case that the behavior of the DC–DC converter is non critical or has large design margins (Max1682, switched capacitor voltage doubler). This is rarely done, since the conversion characteristics are typically very sensitive to variations in operation circumstances (varying load, varying input voltage, temperature). The latter is demonstrated in Chap. 3.

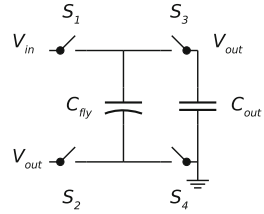
### 2.1.2 Principles

The capacitive DC–DC converter is identified as a Variable Structure System (VSS). The operation of such a VSS is characterized by the repetitive change in the circuit's structure. In contrast to inductive converters, capacitive converters use only switches and capacitors to transfer charge between the input and the output. In fact the capacitive converter consists of two distinct types of capacitors: the flying capacitors and the output buffer capacitor.

The flying capacitors are the charge-transferring capacitors. While the buffer capacitor does not participate in the charge transfer, it mainly influences the start-up behavior of the converter and the steady-state noise characteristics. In general the periodical reconfiguration of the switched-capacitor structure exists of two or more states.<sup>1</sup>

<sup>1</sup> In practice multi-state converters are a rarity (Ben-Yaakov and Kushnerov 2009). Two-state converters are used in most of the publications.

**Fig. 2.2** The conversion block of a fractional  $\frac{1}{2}$  converter: it consists of the flying capacitor  $C_{fly}$ , the output buffer capacitor  $C_{out}$  and four switches  $S_i$



One of the most important constraints faced during the design of a capacitive DC–DC converter is the following. Each converter topology has an ideal VCR (iVCR). This iVCR is the maximum ratio between the output voltage and the input voltage of the conversion block. In practice this iVCR is the upper bound for the actual VCR and the converter can only operate at a theoretical efficiency of 100 % when this VCR is met. For a converter with an input voltage  $V_{in}$ , an output voltage  $V_{out}$  and a common ground connection. The actual VCR is defined as:

$$VCR = \frac{V_{out}}{V_{in}} \quad (2.1)$$

A certain topology corresponds to a single iVCR, but a given iVCR can be obtained by multiple topologies. This gives the designer a range of possible implementations for achieving a certain conversion or conversion range and this is discussed in Sect. 2.3. In order to substantiate the previous description, the operation of capacitive DC–DC converters is demonstrated by means of the most straightforward capacitive DC–DC converter: the series-parallel  $\frac{1}{2}$  converter.

### 2.1.3 Example: The Series-Parallel $\frac{1}{2}$ Converter

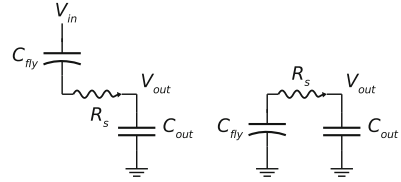
The series-parallel  $\frac{1}{2}$  converter consists of one flying capacitor  $C_{fly}$  and an output buffer capacitor  $C_{out}$ . The terminals of the flying capacitors undergo a significant change in potential due to the periodic change in converter structure. The output buffer capacitor does not participate in the charge transfer related to the conversion, it only reduces the switching noise that originates from the switched nature of the converter. One of the output capacitor's terminals is connected to ground or another DC voltage in the circuit. In Fig. 2.2 a series-parallel  $\frac{1}{2}$  converter topology is shown.

The two-state operation of a series-parallel  $\frac{1}{2}$  converter is formed by alternating between the following configurations:

$$\phi_1 : S_1 = S_2 = 1, S_3 = S_4 = 0 \quad (2.2)$$

$$\phi_2 : S_1 = S_2 = 0, S_3 = S_4 = 1 \quad (2.3)$$

**Fig. 2.3** Graphical representation of the two states of a fractional  $\frac{1}{2}$  converter: the *left pane*: state  $\phi_1$  and the *right pane*: state  $\phi_2$



Those two states are graphically represented in Fig. 2.3. The left-pane structure corresponds to state  $\phi_1$  and the right pane to state  $\phi_2$ . By alternating in a periodical way the steady state voltage at the output ideally corresponds to  $\frac{V_{in}}{2}$ .

In order to demonstrate the circuit's behavior, the system's set of time-dependent differential equations is formulated. For sake of generality an equivalent series resistance  $R_s$  is included. This resistance can be either invoked by the non-zero on-resistance of the switches, by the series resistance of the capacitors or a combination of both.

For state  $\phi_1$ :

$$V_{out} = V_{in} - V_{C_{fly}} - R_s C_{fly} \frac{dV_{C_{fly}}}{dt} \quad (2.4)$$

$$C_{fly} \frac{dV_{C_{fly}}}{dt} - C_{out} \frac{dV_{out}}{dt} = 0 \quad (2.5)$$

For state  $\phi_2$ :

$$V_{out} = V_{C_{fly}} + R_s C_{fly} \frac{dV_{C_{fly}}}{dt} \quad (2.6)$$

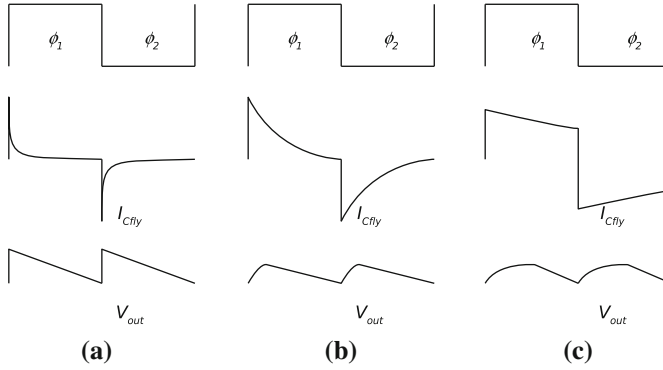
$$C_{fly} \frac{dV_{C_{fly}}}{dt} + C_{out} \frac{dV_{out}}{dt} = 0 \quad (2.7)$$

By solving this system of differential equations of state  $\phi_2$  for the boundary conditions  $V_{C_{fly},0} = V_{C_{fly},-}$  and  $V_{C_{out},0} = V_{C_{out},-}$  the output voltage can be obtained as a function of time (t):

$$V_{out} = \frac{C_{fly} V_{C_{fly},-} + C_{out} V_{out,-}}{C_{fly} + C_{out}} - C_{fly} \frac{V_{C_{fly},-} - V_{out,-}}{C_{fly} + C_{out}} e^{-\frac{C_{out} + C_{fly}}{R_s C_{fly} C_{out}} t} \quad (2.8)$$

$$I(C_{out}) = C_{out} \frac{dV_{out}}{dt} = \frac{V_{C_{fly},-} - V_{out,-}}{R_s} e^{-\frac{C_{out} + C_{fly}}{R_s C_{fly} C_{out}} t} \quad (2.9)$$

The peak current is observed at  $t = 0$ :



**Fig. 2.4** **a** Full Charging Mode (FCM), **b** Boundary Charging Mode (BCM), **c** Partial Charging Mode (PCM)

$$I_{C_{fly},+,peak} = \frac{V_{C_{fly},-} - V_{out,-}}{R_s} \quad (2.10)$$

The current pattern in Eq. 2.9 is dominated by an exponential decay, the rate is determined by the parasitic resistance  $R_s$  and the capacitor sizes. While the peak current during changing state of this Fractional Converter is only proportional to the voltage difference before changing state and inversely proportional to the parasitic resistance in the circuit  $R_s$ . Notice that if no resistance is present the charge transfer finds place by means of a current pulse ( $I_{C_{fly},+,peak} = \infty$ ) and the decay time turns to zero.

Based on the time constants of the charge transfer, early literature (Zhu and Ioinovici 1996) describes three operation modes: The Full Charging Mode where the parasitic resistance is relatively small and the flying capacitor current decays to zero during each state or switching interval. The Boundary Charging Mode for which the current decay corresponds to half of the switching period and the Partial Charging Mode where the current pattern resembles a linear slope and the flying capacitor current does not turn to zero during commutation. This effect of the parasitic resistances can be observed in Fig. 2.4. Negligible parasitic resistance is observed when the charge transfer resembles a current pulse in Fig. 2.4a, large parasitic resistance in Fig. 2.4c is identified by the quasi-constant current pattern.

## 2.2 Analysis Techniques

In this section three analysis techniques are selected: Charge Flow Analysis, Charge Balance Analysis and Branch Analysis. The selected techniques demonstrate a comprehensive introduction to the most prominent modeling approach for capacitive DC–DC converters: The Output Impedance Model.

### 2.2.1 Charge Flow Analysis

Charge Flow Analysis is the primary tool for identifying the role of the different components in the conversion block. Based on this analysis, the charge flow vectors  $a_c^i$  are extracted. These vectors play an important role in the modeling and design techniques presented in this work. They qualify the capacitive converter performance and enable an objective comparison of the converter topologies.

A conversion block consists of a number of linear networks switched periodically to achieve the charge transfer (Wu and Bass 2000). A first step in the analysis of such an array is to identify the component configurations for the separate states of the conversion and to formally describe the converter topology. Therefore a set vectors is defined (Seeman and Sanders 2008) describing the topology based on the charge flow through the components.  $q_i^{(j)}$  represents the amount of charge that is transferred during state  $j$  by capacitor  $i$ .  $q_{out}$  is the total amount of charge transferred to the load during a switching period  $T$ .

The charge flow through the capacitors is described by:

$$a_c^{(1)} = [q_{out}^{(1)} \ q_1^{(1)} \ \dots \ q_n^{(1)} \ q_{in}^{(1)}] / q_{out} \quad (2.11)$$

$$a_c^{(2)} = [q_{out}^{(2)} \ q_1^{(2)} \ \dots \ q_n^{(2)} \ q_{in}^{(2)}] / q_{out} \quad (2.12)$$

These charge vector elements can be determined by inspection for every state of the conversion period based on the following principles:

- Kirchhoff's current law in each node: The sum of charge flow elements equals zero in each circuit node.
- In steady state, for every component the sum of both state's charge flow elements equals zero.
- The output capacitor  $C_{out}$  is much larger than the flying capacitors and behaves as a voltage source with respect to the remainder of the circuit. This assumes no voltage ripple at the output node.

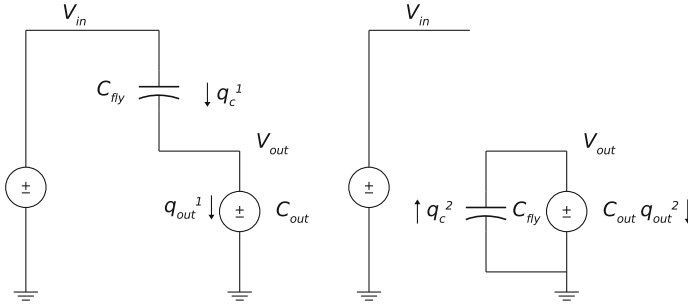
This is demonstrated by an analysis of a  $\frac{1}{2}$  series-parallel converter in Fig. 2.5. For this converter:

$$a_c^{(1)} = [q_{out}^{(1)} q_{C_{fly}}^{(1)} q_{out}^{(1)}]$$

$$a_c^{(1)} = [\frac{1}{2} \ \frac{1}{2} \ \frac{1}{2}] \quad (2.13)$$

$$a_c^{(2)} = [\frac{1}{2} \ \frac{-1}{2} \ \frac{0}{2}] \quad (2.14)$$

The following observations are made. The charge vector elements of both states of the flying capacitors have opposite signs. The charge vector elements of the output sum to 1. The ratio of the total input and output charge vector elements equals the iVCR ( $N$ ) of the topology:



**Fig. 2.5** Charge Balance Analysis of a fractional  $\frac{1}{2}$  converter: the *left pane*: state  $\phi_1$  and the *right pane*: state  $\phi_2$

$$N = \frac{q_{in}}{q_{out}} \quad (2.15)$$

This demonstrates that this intuitive method can be used for determining the converter's iVCR.

### 2.2.2 Charge Balance Analysis

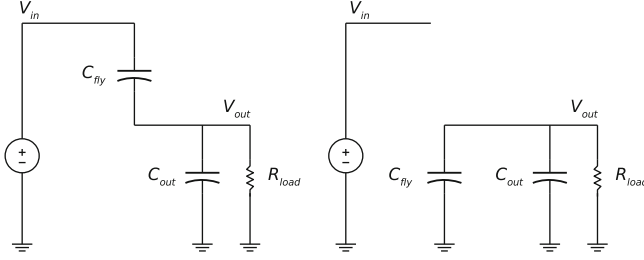
Charge Balance Analysis is used in the analysis of switched-capacitor circuits and is based on the law of charge conservation (Tsividis 1983). Charge Balance Analysis deals with the absolute amount of charge in the circuit, this in contrast with the Charge Flow Analysis that concerns the change in charge on the components. Therefore the charge flow analysis which is depicted in Fig. 2.6 uses the quantity  $q_x$  and the charge balance method uses the quantity  $Q_x$ . These quantities have the same dimension, Coulomb, but  $q_x$  denotes a change in  $Q_x$  for a change in time  $\Delta t = t_1 - t_0$ :

$$q_x = Q_{x,t=t_1} - Q_{x,t=t_0} \quad (2.16)$$

In steady state the charge is conserved along both states of the switching period and the output voltage is constant:

$$\Sigma Q_{c,i}^{(1)} = Q_{out}^{(2)} + \Sigma Q_{c,i}^{(2)} \quad (2.17)$$

The charge stored on the capacitors (including on the output capacitor) is calculated based on the voltage-capacitance-charge relationship. The charge dissipated in the load has been determined by Ohm's law.



**Fig. 2.6** Discrete Time Analysis of a fractional  $\frac{1}{2}$  converter: the *left pane*: state  $\phi_1$  and the *right pane*: state  $\phi_2$

$$Q_{out}^{(2)} = \frac{V_{out}[n-1]}{2R_{load}f_{sw}} \quad (2.18)$$

This results in the following charge conservation equation:

$$\begin{aligned} C_{fly}(V_i[n-1] - V_{out}[n-1]) + C_{out}V_{out}[n-1] \\ = \frac{V_{out}[n]}{2R_{load}f_{sw}} + C_{fly}V_{out}[n] + C_{out}V_{out}[n] \end{aligned} \quad (2.19)$$

This Discrete Time equation can be transformed into the circuit's transfer function (TF) by means of the Z-transform (Dorf 1995):

$$\frac{V_{out}}{V_{in}} = \frac{C_{fly}z^{-1}}{(C_{fly} + C_{out} + \frac{1}{2R_{load}f_{sw}}) - (-C_{fly} + C_{out})z^{-1}} \quad (2.20)$$

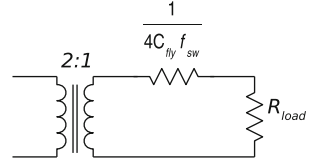
This transfer function demonstrates the input-output voltage relationships in function of the switching frequency  $f_{sw}$  the capacitor sizes  $C_{out}$ ,  $C_{fly}$  and the load  $R_{load}$ .

First the transfer function 2.20 is analyzed for the unloaded case ( $R_{load} = \infty$ ) and in case no AC variation ( $z = 1$ ):

$$\frac{V_{out}}{V_{in}} = \frac{C_{fly}}{(C_{fly} + C_{out}) - (C_{out} - C_{fly})} = \frac{1}{2} \quad (2.21)$$

For the loaded converter: transfer function 2.20 is evaluated in  $z = 1$  and this gives:

**Fig. 2.7** Schematic representation of the equivalent circuit found by applying the Charge Balance Method to a series-parallel  $\frac{1}{2}$  capacitive converter



$$\frac{V_{out}}{V_{in}} = \frac{C_{fly}}{\left(C_{fly} + C_{out} + \frac{1}{2R_{load}f_{sw}}\right) - (-C_{fly} + C_{out})} \quad (2.22)$$

$$= \frac{1}{\left(2 + \frac{1}{2C_{fly}R_{load}f_{sw}}\right)} \quad (2.23)$$

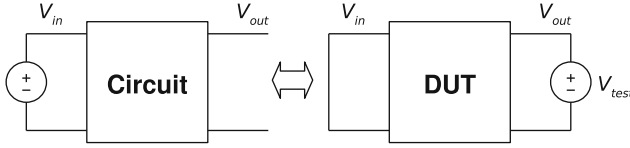
Equation 2.23 can be simplified:

$$V_{out} = \frac{1}{2} V_{in} \frac{R_{load}}{\left(R_{load} + \frac{1}{4C_{fly}f_{sw}}\right)}. \quad (2.24)$$

This input–output relationship consists of two factors: the constant gain factor  $\frac{1}{2}$  and the load dependent gain factor  $\frac{R_{load}}{\left(R_{load} + \frac{1}{4C_{fly}f_{sw}}\right)}$ . Actually considering a constant  $C_{fly}$  and  $f_{sw}$ , this gain equals the gain of a resistive divider. The same transfer function can be achieved by cascading an ideal DC–DC transformer with a fixed gain  $\frac{1}{2}$  and a resistive divider. This is demonstrated in Fig. 2.7. This means that a capacitive converter is determined by a conversion ratio  $N$  and an output impedance. Analysis of other topologies by means of this Charge Balance Method results in similar solutions.

### 2.2.3 Branch Analysis

The Charge Balance Analysis is a technique to analyze a capacitive conversion block but for complex converter topologies it turns to be an exhaustive method. Therefore the following analysis has been developed to determine the output impedance, based on Tellegen’s theorem: Branch Analysis. The Branch Analysis involves two approximations of the output impedance. The first includes nothing but the effect of the switched-capacitor nature of the converter. It is described by the Slow Switching Approximation. The second approximation only includes the resistive nature of the converter and is described by the Fast Switching Approximation. First Tellegen’s theorem is revisited:



**Fig. 2.8** **a** Regular set-up of the converter. **b** The converter as a Device Under Test in a set-up to determine the output impedance

**Tellegen 1** Consider an arbitrary lumped network whose graph  $G$  has  $b$  branches and  $n_t$  nodes. Suppose that to each branch of the graph we assign arbitrarily a branch potential difference  $W_k$  and a branch current  $F_k$  for  $k = 1, 2, \dots, b$ , and suppose that they are measured with respect to arbitrarily picked associated reference directions. If the branch potential differences  $W_1, W_2, \dots, W_b$  satisfy all the constraints imposed by KVL and if the branch currents  $F_1, F_2, \dots, F_b$  satisfy all the constraints imposed by KCL, then

$$\sum_1^b W_k F_k = 0 \quad (2.25)$$

### The Slow Switching Approximation

The Charge Balance analysis suggests that a capacitive converter can be modeled as a voltage-dependent voltage source (or a DC-transformer) with a non-zero output impedance. The most straightforward technique to determine the output impedance of a circuit is to apply a test source at the output terminals of the circuit and to short circuit the input of the circuit. This is demonstrated in Fig. 2.8

Tellegen's theorem can be interpreted as follows: for each state the charge balance vectors are orthogonal with the voltages across the components. Superposition of both states leads to the following equality:

$$v_{out}(a_{out}^{(1)} + a_{out}^{(2)}) + \sum_{i=1}^n (a_{c,i}^{(1)} v_{c,i}^{(1)} + a_{c,i}^{(2)} v_{c,i}^{(2)}) = 0 \quad (2.26)$$

The previous equation can be simplified by taking into account that  $a_{out}^{(1)} + a_{out}^{(2)} = 1$ . Moreover the absolute value of the charge balance vector elements and the voltage difference over the capacitors is introduced:  $a_{c,i} = a_{c,i}^{(1)} = -a_{c,i}^{(2)}$  and  $q_i = a_{c,i} q_{out}$ . These simplifications reduce Eq. 2.26 into:

$$v_{out} q_{out} + \sum_{i=1}^n (q_i \Delta v_i) = 0 \quad (2.27)$$

If it is assumed that the capacitors are linear or demonstrate a linear behavior in the operation point they are used. Then  $\Delta v_i = \frac{q_i}{C_i}$ . By dividing Eq. 2.27 by  $q_{out}^2$  the following equality is obtained:

$$\frac{v_{out}}{q_{out}} - \sum_{i=1}^n \left( \frac{q_i}{q_{out}} \right)^2 \frac{1}{C_i} = 0 \quad (2.28)$$

If both terms are divided by the switching frequency  $f_{sw}$  the following formulation is obtained:

$$\frac{v_{out}}{q_{out} f_{sw}} = \frac{v_{out}}{i_{out}} = \sum_{i=1}^n \left( \frac{q_i}{q_{out}} \right)^2 \frac{1}{f_{sw} C_i} \quad (2.29)$$

By definition  $a_{c,i} = \frac{q_i}{q_{out}}$ , then it is readily derived that the output impedance corresponds to the ratio of the test voltage and the resulting current. Moreover the output impedance is only a function of the amount of flying capacitance, the switching frequency and the sizing of the flying capacitors:

$$R_{SSL} = \sum_{i=1}^n \frac{a_{c,i}^2}{f_{sw} C_i} \quad (2.30)$$

For this derivation the influence of the parasitic resistors in the circuit are ignored and therefore this output impedance is only valid considering no influence of the resistance in the circuit.

### The Fast Switching Approximation

If the parasitic resistance can not be ignored and the power loss due to these resistances is dominant, another approach is followed. A set of switch charge flow vectors is determined. This can be done based on the same methodology proposed in the Charge Flow Analysis. There are two switch charge vectors each corresponding to each one of the converter's states. Each element  $a_{r,i}$  of the vector corresponds to the charge flow through one of the switches  $S_r$ .

The average current through the switches equals the amount of charge divided by the commutation period  $DT = \frac{D}{f_{sw}}$ :

$$i_{r,i} = \frac{q_{r,i} f_{sw}}{D} \quad (2.31)$$

Considering that  $q_{r,i} = a_{r,i} q_{out}$  and  $q_{out} = \frac{i_{out}}{f_{sw}}$  and the charge flow of a two-state capacitive converter is optimum for dutycycle  $D = 0.5$ :

$$i_{r,i} = 2a_{r,i} i_{out} \quad (2.32)$$

The power loss in the switches can now be formulated as:

$$P_{loss,switches} = \Sigma \left( \frac{1}{2} R_i (2a_{r,i} i_{out})^2 \right) \quad (2.33)$$

Since the power loss is proportional to the square of the output current, the output impedance is:

$$\frac{P_{loss,switches}}{i_{out}^2} = \Sigma \left( \frac{1}{2} R_i 2a_{r,i}^2 \right) \quad (2.34)$$

$$R_{FSL} = 2 \Sigma_i R_i a_{r,i}^2 \quad (2.35)$$

So the  $R_{FSL}$  is the output impedance, if the losses in the switches are dominating the total losses in the capacitive DC–DC converter. This approach inevitably leads to a dual interpretation of a capacitive DC–DC converter's output impedance. Each of these interpretations has nothing in common with the other one: For the capacitive nature the resistance in the circuit is ignored, for the resistive nature, the switched capacitor nature is ignored. Both approaches can be unified by considering both natures as complementary. In Seeman and Sanders (2008), it is demonstrated that the total output impedance is accurately approximated as follows:

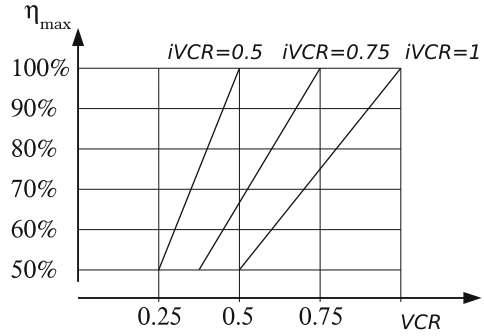
$$R_{out} = \sqrt{R_{SSL}^2 + R_{FSL}^2} \quad (2.36)$$

## 2.3 Topologies: Taxonomy

The topology represents the spatial properties of the capacitive DC–DC converter. More specifically: the structure and interconnection of the converter's components are described. This can be done either by a literal description, for example the netlist of a circuit or by a graphical means, for example a schematic drawing of the circuit components. Since capacitive converters are variable-structure systems with different states, it is preferred to represent each state by a separate schematic. This method has been used in previous sections.

The previous sections dealing with the analysis techniques indicate that each capacitive converter topology has a distinct iVCR. This fundamental property of capacitive DC–DC converters has large repercussions on the use of these converters. First, a single topology has an upper bound for which conversion can be performed:

**Fig. 2.9** In the graph the maximum efficiency with respect to the VCR is demonstrated for three different topologies



the  $iVCR$ . Secondly the efficiency has an upper bound that corresponds to the ratio of the actual  $VCR$  and the  $iVCR$ :

$$VCR \leq iVCR \quad (2.37)$$

$$\eta_{max} = \frac{VCR}{iVCR} \quad (2.38)$$

This relationship is represented in Fig. 2.9. This demonstrates that the maximum attainable efficiency heavily decreases for deviations from the  $iVCR$ . This effect puts constraints on the input-output voltage range of a capacitive converter topology if high efficiency is of the designer's concern. Therefore the  $VCR$  is one of the primary aspects of a capacitive DC–DC converter and classification of the capacitive converter topologies is required.

### 2.3.1 Topology Occurrence Theorem

There exists a vast range of converter topologies. The occurrence of capacitive converter topologies is subject to an important theorem (Makowski and Maksimovic 1995), which predicts the achievable  $iVCR$  given a certain number of capacitors:

The theoretical occurrence of capacitive type DC–DC converter topologies is defined as follows: For a two-state capacitive type of DC–DC converter with  $n$  flying capacitors, the flying capacitors can be configured such that an ideal  $VCR$   $N$  is achieved.

$$N(n) = \frac{V(n_{out})}{V(n_{in})} = \frac{P[n]}{Q[n]} \quad (2.39)$$

The VCR  $N_i$  not only corresponds to the ideal ratio of the output voltage and the input voltage but also corresponds to the ratio between two integer numbers  $P[n]$  and  $Q[n]$ . These characteristic numbers satisfy the following inequalities:

$$Max[Abs[P[n]], Abs[Q[n]]] \leq F_n Min[Abs[P[n]], Abs[Q[n]]] \geq 1 \quad (2.40)$$

In these equations  $N$  is the ideal VCR,  $n$  the number of flying capacitors and  $F_n$  the  $n$ -th Fibonacci number. If the number of flying capacitors is limited to three, the following conversion ratios can be achieved:

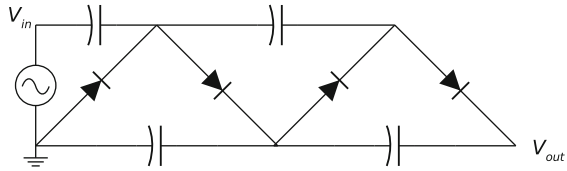
n flying capacitors	$N_i$
1	$\frac{1}{2}, 1, 2$
2	$\frac{1}{3}, \frac{1}{2}, \frac{2}{3}, \frac{2}{2}, 1, 2, 3$
3	$\frac{1}{5}, \frac{1}{4}, \frac{1}{3}, \frac{2}{5}, \frac{1}{2}, \frac{3}{5}, \frac{2}{3}, \frac{3}{4}, \frac{4}{5}, 1, \frac{5}{4}, \frac{4}{3}, \frac{3}{2}, \frac{5}{3}, \frac{2}{2}, \frac{5}{2}, 3, 4, 5$

### 2.3.2 Up Converters

Historically seen, the use of capacitive DC–DC converters focused on up converters. Up-converters have a VCR larger than one. In the early 1900s these converters were used to generate high voltages (in the range of kV) in particle physics experiments. But the break-through of the solid-state transistor renewed the attention for voltage multipliers. By the 1970s capacitive DC–DC converters (charge pumps) found their way as integrated voltage generators in the memory business.<sup>2</sup> It appears that the research interest in up converters has been tempered over the past years, especially due to the emerging potential of down converters and the maturity of the modified Dickson Charge Pumps (Mensi et al. 2005).

<sup>2</sup> Embedded memories require voltage of 5–10 V which is typically higher than the supply voltage of the accompanying chips.

**Fig. 2.10** Greinacher topology



### The Greinacher Multiplier

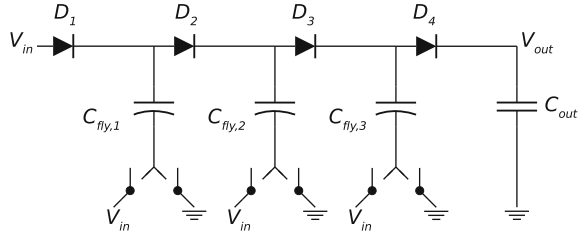
The Greinacher multiplier was invented in 1914 by Heinrich Greinacher, a Swiss physicist (Evannat and Lorrain 1953). It is actually an AC-DC converter but since it served as inspiration for one of the most used DC-DC converters (Dickson 1976) it deserves some attention. In Fig. 2.10 a two-stage Greinacher converter is shown. The physicists John D. Cockroft and Ernest T.S. Walton used this converter to generate extremely high voltages ( $>100\text{ kV}$ ) for their particle physics experiments and this converter became also known as the Cockroft-Walton Voltage Multiplier. The strength of this converter lays within its simplicity: it requires nothing but a number of diodes and capacitors, and no active timing circuitry nor switches.

It operates as follows: during the negative half wave the upper branch capacitors are charged to the peak input voltage. During the positive half wave, the lower branch capacitors are charged to two times the peak input voltage. After a start-up period, the output voltage reaches steady state and an output voltage that becomes ideally equal to  $2nV_{peak}(n_{in})$ ,  $n$  being the number of stages. Moreover the components are only facing a voltage corresponding to two times the peak voltage of the AC-input, while the converter is able to generate voltages that are  $2n$  times higher than the peak input voltage. This concept is used to deal with high voltages while the individual components of the system are facing a small fraction of the high voltage is nowadays known as voltage domain stacking.

This voltage domain stacking is actually a concept used in some of the most state-of-the-art DC-DC converters in Deep Sub Micron CMOS: if the individual components have limited voltage capability, a topology is used that exposes the components to only a fraction of the total voltage (Van Breusseger and Steyaert 2011; Somasekhar et al. 2010; Le et al. 2010; Ng et al. 2009).

### The Dickson Charge Pump

The Dickson Converter or Charge Pump finds its origin in the need for on-chip high-voltage generation (high with respect to the conventional on-chip voltages:  $>10\text{ V}$ ). These high voltages are required for erasing and writing the non-volatile solid-state memories. This invoked a renewed interest in voltage multipliers and for the first time a need for on-chip voltage multipliers. The main bottleneck of the Greinacher

**Fig. 2.11** Dickson topology

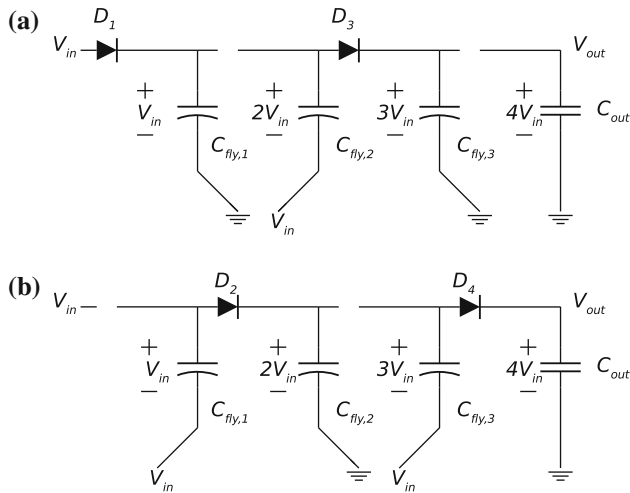
Multiplier laid within the series connection of the capacitors. Practical capacitors and especially on-chip capacitors exhibit a large parasitic capacitance to the chip's substrate (stray capacitance) and the Greinacher Voltage Multiplier proves to be very sensitive to these parasitic elements. Especially due to the series connection of the capacitors. Therefore a new topology (Dickson 1976) was introduced in 1976, that demonstrates a structure based on parallel connection of the capacitors instead of series connection. This topology demonstrates a much lower output impedance and a much higher resilience to stray capacitance. In Fig. 2.11 a three-stage Dickson is represented. An ideal unloaded Dickson converter with  $n$  stages,  $n$  equally sized flying capacitors with a total flying capacitance  $C_{fly}$ , a stray capacitance  $\alpha$ , switching at a frequency  $f_{sw}$  and loaded with a current  $I_{load}$ , has the output voltage

$$V_{out} = V_{in} + \frac{n}{1 + \alpha} \left( V_{in} - \frac{I_{load}}{f_{sw} C_{fly}} \right) \quad (2.41)$$

The Dickson charge pump operates as shown in Fig. 2.12: In a first state the odd numbered diodes in the diode string conduct and transfer charges in the direction of the load through the diode string. In the second state, the even-numbered diodes conduct and the odd-numbered diodes block. This sequence is invoked by alternating the potential of the flying capacitors bottom plate by means of the switches. In more advanced implementations (Mensi et al. 2005) the diodes are replaced by active devices and feed-forward biasing<sup>3</sup> techniques are adopted to decrease the threshold voltage and thus the drop-out voltage over the switches in the previously called 'diode string'.

This charge pump has the same advantages as the Greinacher Multiplier concerning the diodes and switches: these are exposed to a fraction of the output voltage. But the capacitors are dealing with much larger voltages, but a lot of capacitor types have a large breakdown voltage by nature and this is exploited in the following design: Van Breussegem and Steyaert (2011). In this converter,

<sup>3</sup> Feed-forward biasing denotes the biasing of diode-connected MOS devices by means of a next stage voltage node in the diode string, operating at a higher voltage. By doing this the threshold voltage can be reduced and power loss in the diode is cut.



**Fig. 2.12** The operation of a Dickson Charge Pump: **a** State 1, **b** State 2

only the capacitors in the level shifter are dealing with larger voltages. The capacitors used herein can cope with voltages up to 10 V.

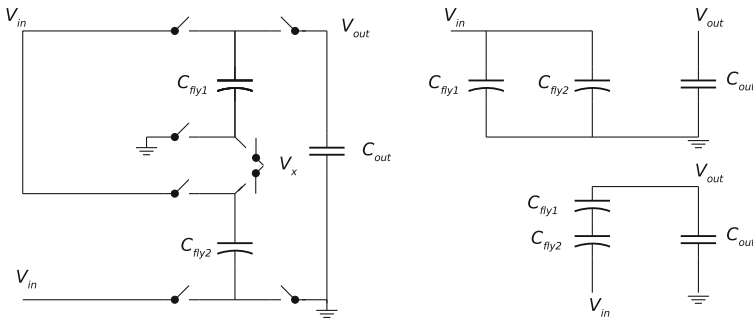
### Parallel-Series Converter

The most straightforward capacitive DC–DC converter is the Parallel-Series Converter. In a first state the flying capacitors are parallel charged by the input source, in the second state the capacitors are series discharged between input and output node. An integer  $(n + 1)$  Parallel Series converter has  $n$  flying capacitors and an ideal voltage multiplication of  $(n + 1)$ .

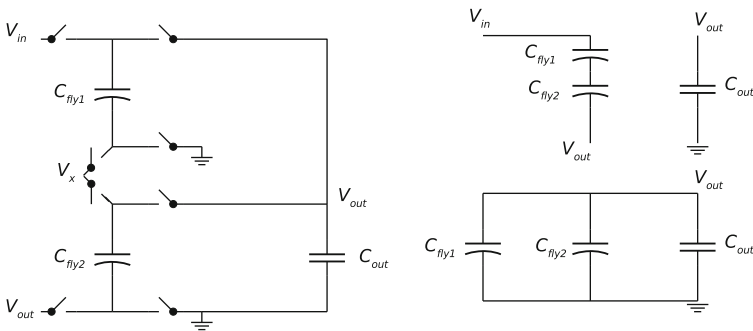
The integer  $\frac{3}{1}$  Parallel-Series Converter, that is represented in Fig. 2.13, operates in a two-state cycle. During the first state both flying capacitors are charged up to the input voltage. During this state of the commutation the output capacitor is decoupled from the charge-transferring structure. Next the flying capacitors are series-connected between input and output node and in steady state the output voltage equals three times the input voltage, in case no load is applied.

### 2.3.3 Down Converters

The interest in capacitive DC–DC down converters has grown recently. Especially the so-called *Voltage Gap* discussed in Chap. 1 has pushed capacitive down-converters



**Fig. 2.13** Parallel series converter topology with schematic representation of both configuration states



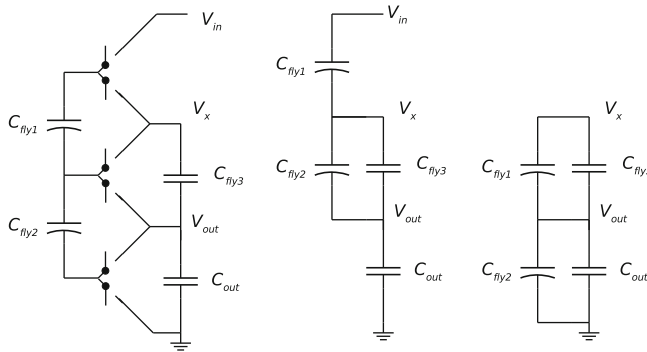
**Fig. 2.14** Series-parallel converter topology with schematic representation of both configuration states

into the main stream of power-management solutions. This section describes a number of the dominant down-conversion topologies, found in literature.

### Series-Parallel Converter

The Series-Parallel converter is the antagonist of the Parallel-Series Converter. In a first state the flying capacitors are connected in series between input node and output node while in the second state the capacitors are discharged in parallel with the output. A  $(n + 1)^{-1}$  Parallel-Series converter has  $n$  flying capacitors and an ideal voltage multiplication of  $(n + 1)^{-1}$ . It is actually the mirrored version of the up converter but with transposed input and output nodes.

The  $\frac{1}{3}$  capacitive converter is shown in Fig. 2.14, the left pane shows the entire topology while the right pane highlights the configurations during both states of the topology.



**Fig. 2.15** Ladder topology

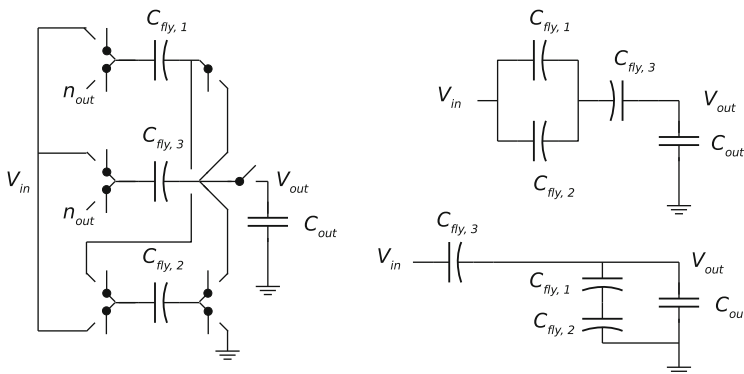
### Ladder Converter

The ladder converter consists of two series-capacitor-strings that slide along each other while charging from the supply and discharging towards the load. Figure 2.15 shows the two states of a ladder converter. A converter with  $n$  flying capacitors performs a primary conversion with a ratio  $\frac{2}{n+3}$ , with  $n$  the number of flying capacitors. For a ladder converter each capacitor will charge until a voltage equal to  $\frac{(n+3)V_{in}}{2}$  is observed across each capacitor in case no load is applied of course.

The converter has the advantage that a DC voltage can be tapped from multiple nodes ( $n_{out}$   $n_x$  for the example). It is thus a multiple-output converter by nature. But loading of multiple nodes will increase the output impedance and thus negatively influence the converter efficiency if the other specifications remain the same. Moreover a type of voltage-domain stacking can be implemented because of the multiple DC nodes in the circuit and this makes this kind of converter very appealing to use in high-input-voltage applications. On the other hand, this type of converter requires a relatively large number of switches and this turns the converter in a switch-intensive solution.

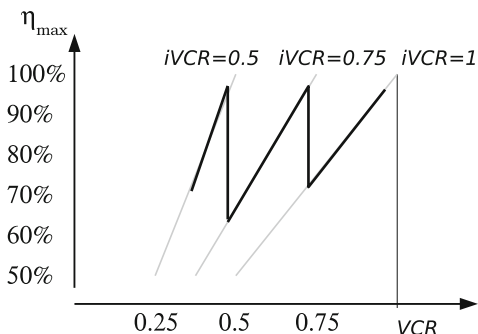
### Fractional Converter

The Fractional Converters is a family of converters that cannot be classified under the previous types (Makowski and Maksimovic 1995). In most cases the iVCR of this type is hard to be determined by visual inspection. Formal determination of the iVCR is performed by means of the analysis techniques presented in the previous section. The existence of this kind of converter is predicted by the theorems in Makowski and Maksimovic (1995), but their synthesis is non-methodological. In Fig. 2.16 a  $\frac{4}{5}$  fractional converter topology is shown. At the right the component configuration is demonstrated for both conversion states.



**Fig. 2.16** A fractional 4/5 topology and converter states

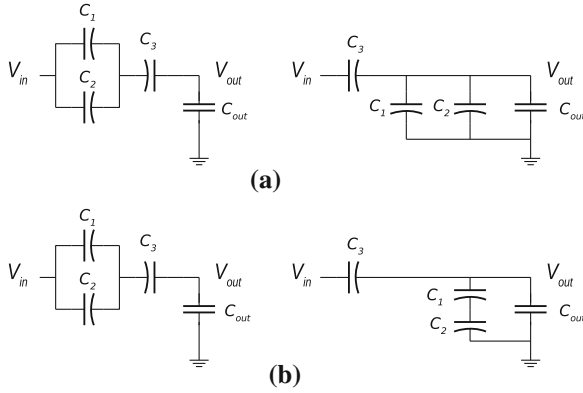
**Fig. 2.17** Graphical representation of the potential efficiency improvement by using the multi-topology approach



### 2.3.4 Multi-Topology Converters

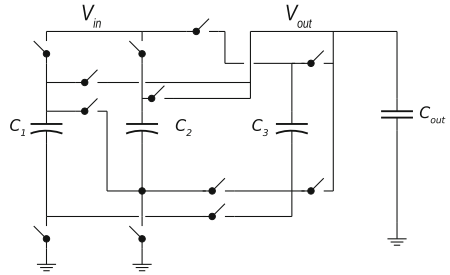
The relationship between topology and iVCR puts constraints on the input-output voltage range of the converter and the associated converter's performance within this range. To improve the efficiency/performance over a broad range and thus to increase the flexibility of the converter (the ability to deal with a broad range of conversion scenario's), there is a clear need for multi-topology capacitive converters.

These converters comprise a capacitor-switch array that can not only switch between both states of the base topology but can also switch between different topologies. Each one of these topologies addresses a separate part of the input-output range. The latter technique is demonstrated in Fig. 2.17. The ideal efficiency ratings of three topologies, based on Eq. 2.38, are drawn in gray. Using either one of them in a separate configuration will either constraint the input output range: the topologies have a maximum VCR corresponding to the iVCR. Or each topology demonstrates a poor performance (low maximum efficiency  $\eta_{max}$ ) if the VCR deviates significantly from iVCR but by combining multiple topologies in a single structure and to switch



**Fig. 2.18** Multi topology converter: **a** the 2/3-topology, **b** the 4/5-topology

**Fig. 2.19** Implementation of a multi topology converter with both a 4/5 and a 2/3 topology

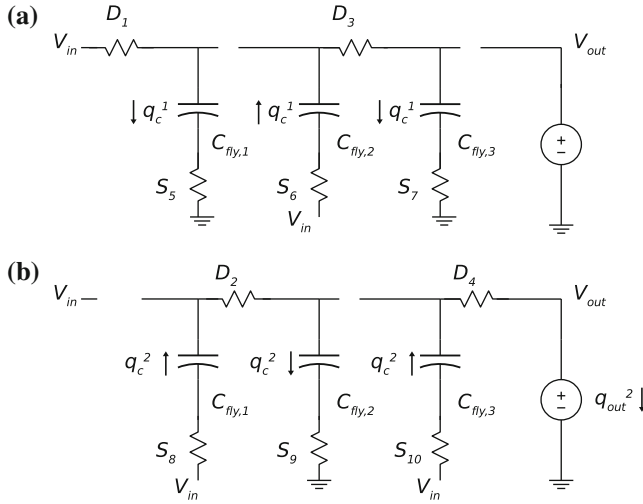


structure according to the required VCR. In Fig. 2.17 the potential maximum efficiency of a multi-topology converter comprising of three topologies ( $iVCR = \frac{1}{1} \frac{3}{4} \frac{1}{2}$ ) is demonstrated by means of the thick dark line. This shows that the input-output range is extended and that in the low VCR range the efficiency is boosted with respect to the single topology approach if only  $iVCR \frac{3}{4}$  is used. In Fig. 2.18 the converter's states are shown. In the upper pane (a) the  $\frac{2}{3}$ -topology, in the lower pane (b) the  $\frac{4}{5}$ -topology.

In Fig. 2.19 an implementation example is demonstrated of a multi-topology converter comprising of a dual  $\frac{4}{5}$  and a  $\frac{2}{3}$  capacitive converter.

## 2.4 Topologies: Analysis

The previous section introduced a selection of topologies occurring in the state-of-the-art capacitive converters. In this section the analysis technique presented before are applied to these topologies. This analysis provides a first look at the topology performance and the opportunities laying herein. For each converter topology, both states are graphically represented including the parasitic switch resistance. Other



**Fig. 2.20** Charge Flow Analysis of the Dickson Converter

parasitic components, for example the parasitic series resistance of the switches or the parasitic resistance related to the metal interconnect between the components, can be included in a similar fashion. But for sake of clarity this is omitted in this first analysis.

### 2.4.1 Dickson Converter

The Dickson converter is a two state converter (Dickson 1976; Zhang and Llaser 2004). Figure 2.20 represents both states of the converter. In the state-of-the-art implementations of the Dickson Converter (Mensi et al. 2005), the diodes in the diode string are replaced by active switches. During state  $\phi_1$  switches  $D_1$   $D_3$   $S_5$   $S_6$   $S_7$  are conducting while the other switches are off. During state  $\phi_2$  switches  $D_2$   $D_4$   $S_8$   $S_9$   $S_{10}$  are conducting, while the other switches are off.

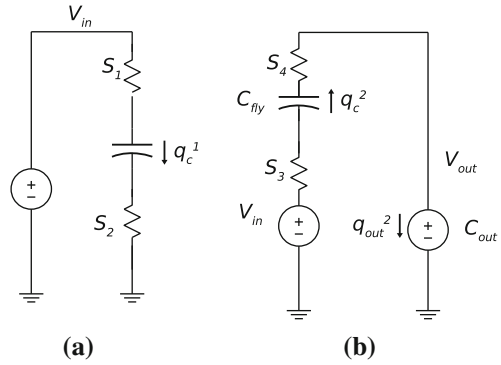
Based on the charge Flow Analysis the following capacitor charge vectors are derived:

$$\vec{a}_c^{(1)} = [0(-1)(+1)(-1)(2)]$$

$$\vec{a}_c^{(2)} = [1(+1)(-1)(+1)(2)]$$

Similarly the switch charge vectors can be calculated:

**Fig. 2.21** Charge Flow Analysis of the Voltage Doubler



$$\begin{aligned} \vec{a}_r^{(1)} &= [010101010102] \\ \vec{a}_r^{(2)} &= [101010101012] \end{aligned} \quad (2.42)$$

For this Dickson converter:

$$N = \frac{q_{in}}{q_{out}} = \frac{2+2}{1} = 4 \quad (2.43)$$

In case that the output impedance is maximized by matching the component sizing with the charge vector elements the following output impedance factors are obtained:

$$R_{SSL} = \frac{(1+1+1)^2}{C_{fly} f_{sw}} \quad (2.44)$$

$$R_{FSL} = 2 \frac{(1+1+1+1+1+1+1+1+1+1+1)^2}{G_{tot}} \quad (2.45)$$

### 2.4.2 Voltage Doubler

The voltage doubler is a broadly used parallel-series capacitive DC–DC converter (Lee et al. 2006; Gregoire 2006; Lau et al. 2007; Van Breussegeem and Steyaert 2009). It is often used to supply a higher voltage at a small part of a chip to improve its performance. In other configurations, multiple voltage doublers are cascaded to achieve a voltage multiplication  $2^k$  with  $k$  the number of conversion stages (Starzyk et al. 2001). This results in a larger voltage multiplication than a Dickson converter where the gain increases linearly instead of exponentially. In Fig. 2.21 both states of a single stage voltage doubler topology are shown. The voltage doubler consists of a single flying capacitor  $C_{fly}$ , a single output buffer capacitor  $C_{out}$  and four switches  $S_{1-4}$ .

The following charge flow vectors are derived for a single stage voltage doubler:

$$\begin{aligned} a_r^{(1)} &= [011001] \\ a_r^{(2)} &= [100111] \\ a_c^{(1)} &= [0(-1)(1)] \\ a_c^{(2)} &= [1(+1)(1)] \end{aligned}$$

For this voltage doubler DC–DC converter:

$$N = \frac{q_{in}}{q_{out}} = \frac{2}{1} = 2 \quad (2.46)$$

In case that the output impedance is maximized by matching the component sizing with the charge vector elements the following output impedance factors are obtained:

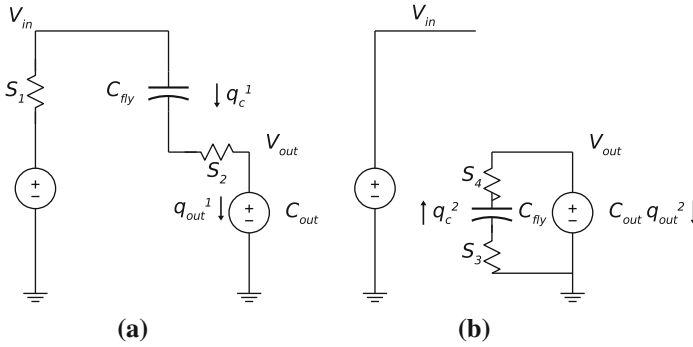
$$R_{SSL} = \frac{1}{C_{fly} f_{sw}} \quad (2.47)$$

$$R_{FSL} = 2 \frac{(1 + 1 + 1 + 1)^2}{G_{tot}} \quad (2.48)$$

### 2.4.3 Voltage Divider

The voltage divider is the antagonist of the voltage doubler, it is a series-parallel converter. From an output impedance point of view this is the most advantageous converter to implement. Therefore it is often used as a demonstrator circuit to show case the impact of technology improvements on capacitive converter design (Chang et al. 2010; Le et al. 2010). The voltage divider, shown in Fig. 2.22, also consists of a single flying capacitor  $C_{fly}$ , a single output buffer capacitor  $C_{out}$  and four switches  $S_{1-4}$ . The charge flow vectors are:

$$\begin{aligned} a_r^{(1)} &= \left[ \frac{1}{2}, \frac{1}{2}, \frac{1}{2}, 0, 0, \frac{1}{2} \right] \\ a_r^{(2)} &= \left[ \frac{1}{2}, 0, 0, \frac{1}{2}, \frac{1}{2}, 0 \right] \\ a_c^{(1)} &= \left[ \frac{1}{2}, \frac{-1}{2}, \frac{1}{2} \right] \\ a_c^{(2)} &= \left[ \frac{1}{2}, \frac{1}{2}, \frac{0}{2} \right] \end{aligned}$$



**Fig. 2.22** Charge Flow Analysis of the Voltage Divider

For this voltage divider DC–DC converter:

$$N = \frac{q_{in}}{q_{out}} = \frac{1}{2} = 0.5 \quad (2.49)$$

In case that the output impedance is maximized by matching the component sizing with the charge vector elements the following output impedance factors are obtained:

$$R_{SSL} = \frac{1}{4C_{fly}f_{sw}} \quad (2.50)$$

$$R_{FSL} = 2 \frac{(4 \times \frac{1}{2})^2}{G_{tot}} \quad (2.51)$$

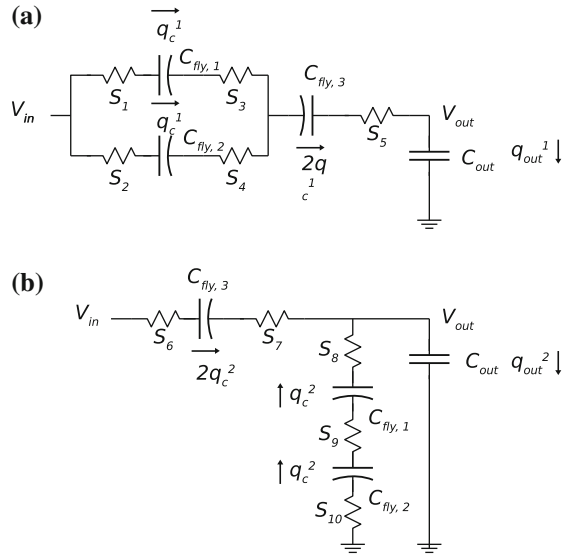
#### 2.4.4 Fractional Converter

Fractional Converters exist for a whole range of conversion ratio's. In practice the number of capacitors is kept below four since the output impedance increases fast in function of the number of capacitors. In Fig. 2.23 both states of a fractional  $\frac{4}{5}$  capacitive converter are demonstrated. The topology requires ten switches.

The Charge Flow vectors are:

$$\begin{aligned} a_r^{(1)} &= \left[ \frac{1}{5}, \frac{1}{5}, \frac{1}{5}, \frac{1}{5}, \frac{1}{5}, \frac{2}{5}, 0, 0, 0, 0, 0, \frac{2}{5} \right] \\ a_r^{(2)} &= \left[ \frac{4}{5}, 0, 0, 0, 0, 0, \frac{2}{5}, \frac{2}{5}, \frac{1}{5}, \frac{1}{5}, \frac{1}{5}, \frac{2}{5} \right] \\ a_c^{(1)} &= \left[ \frac{1}{5}, \frac{1}{5}, \frac{1}{5}, \frac{-2}{5}, \frac{2}{5} \right] \end{aligned}$$

**Fig. 2.23** Charge Flow Analysis of the  $\frac{4}{5}$  Fractional Converter



$$\vec{a}_c^{(2)} = \left[ \frac{4}{5}, \frac{-1}{5}, \frac{-1}{5}, \frac{2}{5}, \frac{2}{5} \right]$$

## 2.5 Conclusion

This chapter has presented a first look at an alternative DC–DC conversion technique: capacitive DC–DC conversion. This technique distinguishes itself from the conventional techniques by omitting the use of an inductor for achieving the DC–DC conversion. A number of techniques has been elaborated to analyze the operation of the converters and to conduct a first comparison between the different capacitive converter topologies. The predominant capacitive converter topologies are presented and some of their appealing characteristics are mentioned. Both the Dickson Converter and the Greinacher Multiplier use a voltage-domain stacking technique to overcome the technology restrictions of the their components. Moreover the Dickson converter shows that capacitors can be used to bridge the voltage gap between multiple voltage domains.

Now that the operation of the capacitive converter is made clear and a first primitive model (the output impedance model) is suggested, it is time to elaborate this model and to construct a design method for capacitive DC–DC converters.

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