Chapter 2
VFC Fundamentals

Voltage-to-frequency converters (VFCs) are, by definition, first-order oscillators whose input is an analog voltage V_{in} and whose output is a frequency signal f_0 linearly proportional to its input voltage, that is, $f_0 = kV_{in}$. They often are denominated as quasi-digital converters because of their analog frequency-coded output. This signal can be directly interfaced to a microcontroller using a single digital input-output port, where, to obtain a digital word, a frequency-to-code conversion must be completed using its internal counters [HUI08]. VFCs are usually mistaken with voltage-controlled oscillators (VCOs), but note that VFCs have different and more stringent performance specifications: typical requirements are high-scale factor accuracy and stability with temperature and supply voltage, wide dynamic range (four decades or more) and low linearity error (less than 0.1 % deviation from zero to full scale) [FRA02, PAL01a].

Although conventional analog-to-digital converters (ADCs) have attracted lots of interest and inversion by huge companies during the past few decades, achieving high levels in terms of development and optimization, currently the widespread use of microcontroller-based measurement systems has made VFCs an attractive alternative to the standard ADC because of their inherent advantages [KIR02a, YUR04]. As mentioned in Chap. 1, frequency modulation exhibits high noise immunity; therefore, frequency signals, compared with analog signals, can be transmitted through communication lines over longer distances [PEA80, SIL00]. Besides, a frequency signal is equivalent to a serial digital signal without the need of synchronization, which makes the interfacing with the microcontroller easier, thus allowing digital conversion with high effective resolution by means of specific conversion algorithms. Note that the frequency-to-code conversion is not a trivial timing window task. Conventional methods have a speed-accuracy trade-off, whereas advanced method needs a license payment [KIR02b, YUR04], which makes the conversion expensive. In addition, it needs a careful analysis that includes the contribution of the algorithmic errors [REV03].

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To provide a deep insight into the theory and design of VFC circuits, this chapter reviews the most important parameters that characterize a VFC. Next, the main VFCs types are explained. To close, a brief introduction to standard frequency-to-code conversion methods is provided.

2.1 VFC Characteristic Parameters

This section defines the key parameters that are used to characterize voltage-to-frequency converters [ALL12, ANA12, FRA10, KEN05, PAL01b]. The majority of them are graphically shown in Fig. 2.1, which represents the normalized output frequency f_0 vs. the normalized input voltage V_{in}. Ideal response is shown in black and an actual transfer response is shown in red.

Input range. Set of values between the lower limit $V_{\text{in,min}}$ and upper limit $V_{\text{in,max}}$, $[V_{\text{in,min}}, V_{\text{in,max}}]$, for which the output frequency f_0 varies linearly with the input.

Output range. Set of values between the lower limit $f_{0,\text{min}}$ and upper limit $f_{0,\text{max}}$, $[f_{0,\text{min}}, f_{0,\text{max}}]$ that vary linearly with the given input range.

Frequency span (***FS***). Positive difference between the output frequencies that correspond to the limits of the input range, where one is the minimum output frequency $f_{0,\text{min}}$, and the other is the upper limit of the range $f_{0,\text{max}}$. Therefore, $FS = f_{0,\text{max}} - f_{0,\text{min}}$.

Sensitivity (***S***) ***or gain***. Variation in the output frequency for a corresponding variation in the input voltage under static conditions. As such, it may be expressed

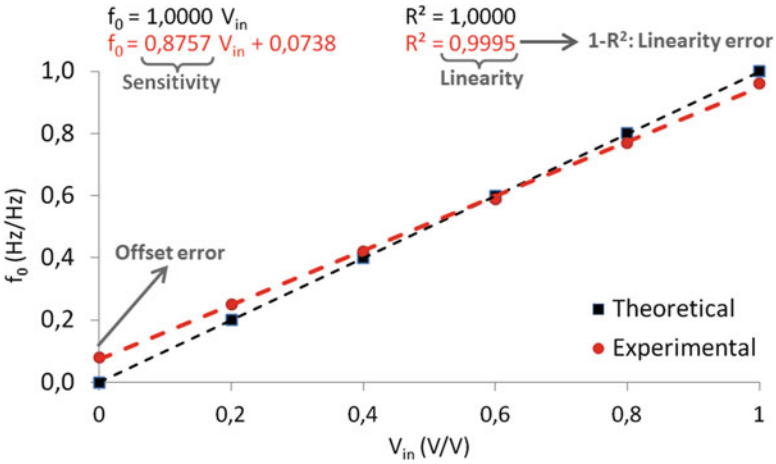

Fig. 2.1 Example of normalized response of an ideal and an actual VFC

as the derivative of the transfer function with respect to the input signal, df_0/dV_{in}. Therefore, as the VFCs considered here are linear, the sensitivity is the slope of the straight line that fits the output frequency f_0 to the input voltage, $f_0 = S\,V_{in}$, given in Hz/V.

Sensitivity or gain error. Deviation of the experimental sensitivity referred to the ideal one, computed as $(S_{exp} - S_{teo})/S_{teo}$ and expressed in percentage.

Sensitivity or gain error drift. Variation of the sensitivity error over the specified temperature range while the remaining parameters are kept constant. It is expressed in ppm/°C.

Relative error. Deviation of the experimental output frequency in each point referred to its ideal value, computed as $(f_{0,exp} - f_{0,teo})/f_{0,teo}$ and expressed in percentage.

Linearity error. Maximum deviation from a straight line passing through the experimental VFC points. There are several measures of this error, the most common one is computed as $(1\text{-}R^2)$, R^2 being the linear regression coefficient. It is expressed in percentage or in bits.

Linearity error drift. Variation of the linearity error over the specified temperature range, while the remaining parameters are kept constant. It is expressed in %/°C.

Offset error. Constant frequency added to the output frequency for all the output ranges. It is usually computed as the absolute deviation of the minimum output frequency $(f_{0,exp}\,(V_{in,min}) - f_{0,teo}\,(V_{in,min}))$, expressed in Hz or in percentage.

Offset error drift. Variation of the offset error over the specified temperature range while the remaining parameters are kept constant. It is expressed in Hz/°C.

Power supply rejection ratio (***PSRR***). It is a measure of the VFC dependence with power supply variations, computed as $S^{-1}\Delta f_0/\Delta V_{DD}$ for a constant input voltage, and expressed in dB.

As with most precision circuitry, through adequate calibration processes gain and offset errors can be trimmed by the user in the microcontroller. However, this does not happen with the linearity error, which is inherent to each VFC topology and will determine, with other factors, the accuracy in the final digitalization. In a VFC response where the sensitivity and the offset errors have been trimmed, linearity error remains the same as it was before trimming; therefore, with an ideal sensitivity and an ideal offset, the linearity error shows how well the experimental data fit the theoretical linear response and, therefore, the accuracy of the converter. Thus, it can be considered that for trimmed VFCs, the linearity error is the fundamental parameter, and the smaller the linearity error, the better the VFC, whereas for non-trimmed systems, other errors become important [BRY97, PAL01a].

2.2 VFC Configurations

There are many different approaches for VFCs in the literature, most of them based on the same operation principle, which consists of an alternate integration of the input voltage and the generation of pulses when the integrator output voltage equals a reference voltage [KIR02a]. Focusing on the most recent VCFs, there are two common architectures: the multivibrator VFC and the charge-balance VFC. Their differences can be seen as a different role of the control circuit: in the multivibrator approach the control circuit imposes the threshold voltages, setting the voltage swing in the capacitor, whereas in the charge-balance approach, the control circuit fixes the duration of the charging (or discharging) phase [VID05].

The multivibrator VFC is usually a current-to-frequency converter (IFC), preceded by a voltage-to-current (V-I) converter. It is simple and demands low power; however, it is less accurate than the charge-balance VFC [STO05].

The charge-balance VFC can be either synchronous or asynchronous. It is more accurate than the multivibrator VFC but needs more power. Its output is not a square signal but a pulse train [BRY97].

Next, these three structures—their ways of operation and their advantages and disadvantages—are described. To verify their operation, functional simulations have been carried out. From these simulations the VFC output signal can be observed, as well as the other main signals that characterize the VFC behavior. More detailed descriptions and other VFC implementations can be found at [KIR02a].

2.2.1 Multivibrator VFC

The block diagram of a typical multivibrator VFC is shown in Fig. 2.2a, and its typical implementation is shown in Fig. 2.2b. A multivibrator VFC consists of an input voltage-to-current converter, followed by a bidirectional current integrator driven by a control circuit. The principle of operation is as follows. First of all, the input voltage V_{in} is linearly converted into a current I_{in}. This current alternatively charges and discharges an integrating capacitor C_{int} between two stable voltage limits, V_{H} and V_{L}, determined by a control circuit, which is usually a voltage window comparator (VWC) or a Schmitt trigger. The waveform at the integrator output is a linear triangular wave and the output of the control circuit is a square signal (Fig. 2.2c), which is the output frequency f_0 of the VFC and also the signal that controls the direction of the integrating current.

Thus, a fully symmetrical repeated loop is built, obtaining at the output a square signal with a frequency given by

$$f_0 = \frac{1}{2} I_{in} \frac{1}{C_{int} \Delta V} \tag{2.1}$$

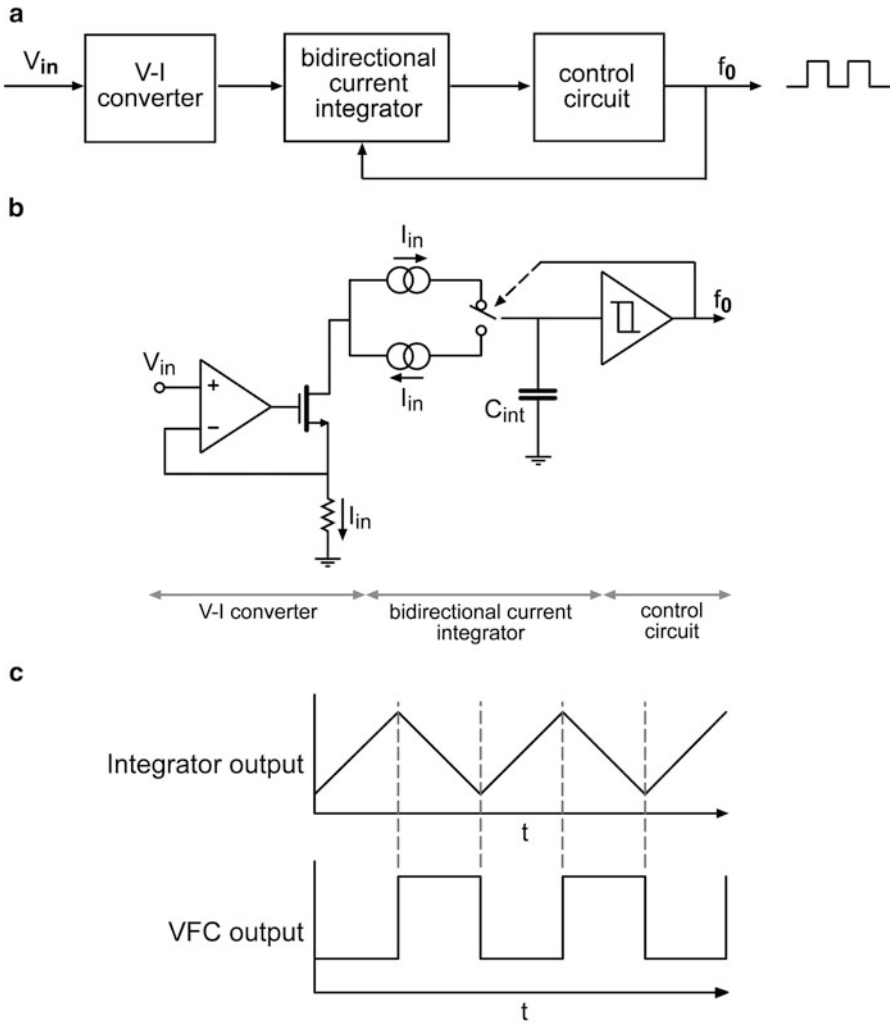

Fig. 2.2 Multivibrator VFC: (**a**) block diagram, (**b**) typical implementation and (**c**) main voltage signals

where I_{in} is the generated current, which is proportional to the input voltage, C_{int} is the integrating capacitor, and $\Delta V = V_{\text{H}} - V_{\text{L}}$.

Practical multivibrator VFCs can achieve around 14 bits of linearity and comparable stability (variation of the actual frequency over time with respect to the ideal frequency), although they may be used in ADCs with higher resolutions without missing codes [ZUM08]. According to (2.1), the performance limits are mainly set by the V_{in}−I_{in} linearity conversion, the comparator threshold noise, and the capacitor temperature coefficient. At high output frequencies, for period widths comparable to VWC delay time, non-negligible errors are introduced in the response of the VFC [KES09].

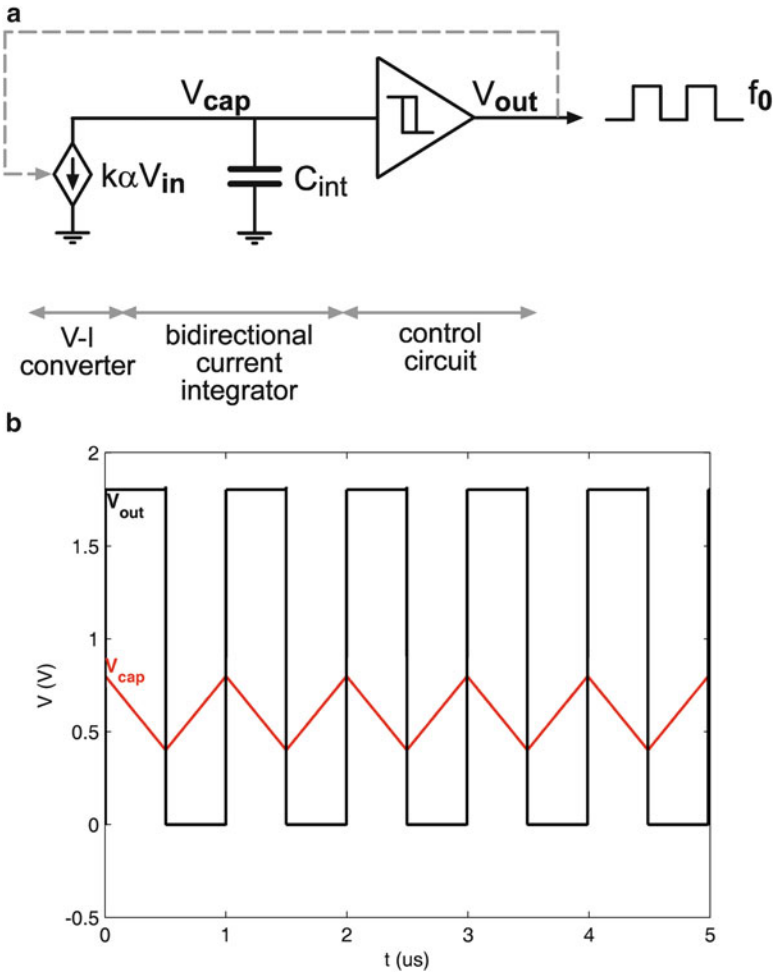

Fig. 2.3 Functional simulation of the multivibrator VFC: (**a**) Schematics and (**b**) capacitor and output waveforms

The scheme shown in Fig. 2.3a was implemented to model the multivibrator VFC in Fig. 2.2a. The input voltage V_{in} is converted into a current $I_{\text{in}} = k\alpha V_{\text{in}}$ with an ideal voltage-controlled current source. This current is integrated in a grounded capacitor C_{int} between the limits V_{L} and V_{H} of a VWC, made up of two ideal comparators and an output $\overline{\text{RS}}$ flip-flop to generate stable signals. The output signal of the VWC, that is, the output signal of the VFC, also controls the sign of the current in the bidirectional current integrator. When the output of the VFC is high, $\alpha = +1$, starting the capacitor discharge phase until V_{cap} reaches V_{L}. At that time, the output of the VFC goes down, $\alpha = -1$, starting the capacitor charge until V_{cap} reaches V_{H}, and so on.

Figure 2.3b shows the waveforms in the time domain at the capacitor (V_{cap}) and at the output of the VFC (V_{out}), for $k = 4$ µS, $V_{\text{in}} = 1$ V, $C_{\text{int}} = 5$ pF, $V_{\text{H}} = 0.8$ V,

and $V_L = 0.4$ V, with a single supply of $V_{DD} = 1.8$ V. The output frequency is, according to (2.1), 1 MHz.

Note than when this VFC is supplied with symmetrical voltages, only the positive half of the voltage range can be converted into a frequency because this VFC cannot integrate negative input voltages. However, when it is single supplied, its input can swing from 0 to V_{DD}. Thus, in both cases, the theoretical input range is $[0, V_{DD}]$.

2.2.2 Asynchronous Charge-Balance VFC

Figure 2.4a shows the general scheme of a charge-balance VFC, and a typical implementation is shown in Fig. 2.4b. It consists of a voltage-to-current converter, a current integrator, a control circuit—usually made up of a comparator and a monostable (one-shot)—and a reference current source responsible for the charge balance.

As shown in Fig. 2.4c, the waveform at the output of the integrator is a two-part linear ramp: the first part lasts for time T_1, which depends on the input voltage, and the second one lasts a fixed time T_2, which corresponds to the pulse given by the monostable. The input voltage V_{in} is converted into a current I_{in}, then this current is integrated, charging the capacitor C_{int}. When the output of the integrator reaches the threshold voltage V_u of a single comparator, the comparator changes its state, triggering the monostable. At that moment, the precision monostable provides a pulse during a fixed time T_2. During this time, a reference current I_{ref}, $|I_{ref}| > |I_{in}|$, is subtracted from the circuit, subtracting a fixed charge from the capacitor, whereas the input current is continuously flowing during the discharge, so no input charge is lost. Once the pulse from the monostable ends, the cycle starts again, resulting in an output pulse rate that is accurately proportional to the rate at which the integrator charges from the input.

The iteration of this cycle gives a sawtooth wave at the integrator output, whose frequency is f_0. This output frequency is proportional to the sum of the charge time T_2 and the discharge time T_1, according to (2.2). That is, the output frequency depends on T_2, which is the pulse width given by the precision monostable; on I_{in}, the applied current proportional to the input voltage V_{in}; and on I_{ref}, the reference current, which is responsible for the charge balance.

$$f_0 = \frac{1}{T_1 + T_2} = \frac{I_{in}}{I_{ref}} \frac{1}{T_2} \tag{2.2}$$

This kind of VFC is more complex and demands more power than the multivibrator one and is able to achieve around 16 – 18 bits of linearity. Critical parameters are the pulse width of the monostable and the value of the reference current, which must be very stable [PAL01a]. At low frequencies, the stability of the voltage sources (V_{ref} and V_u) and the stability of the monostable (which mainly

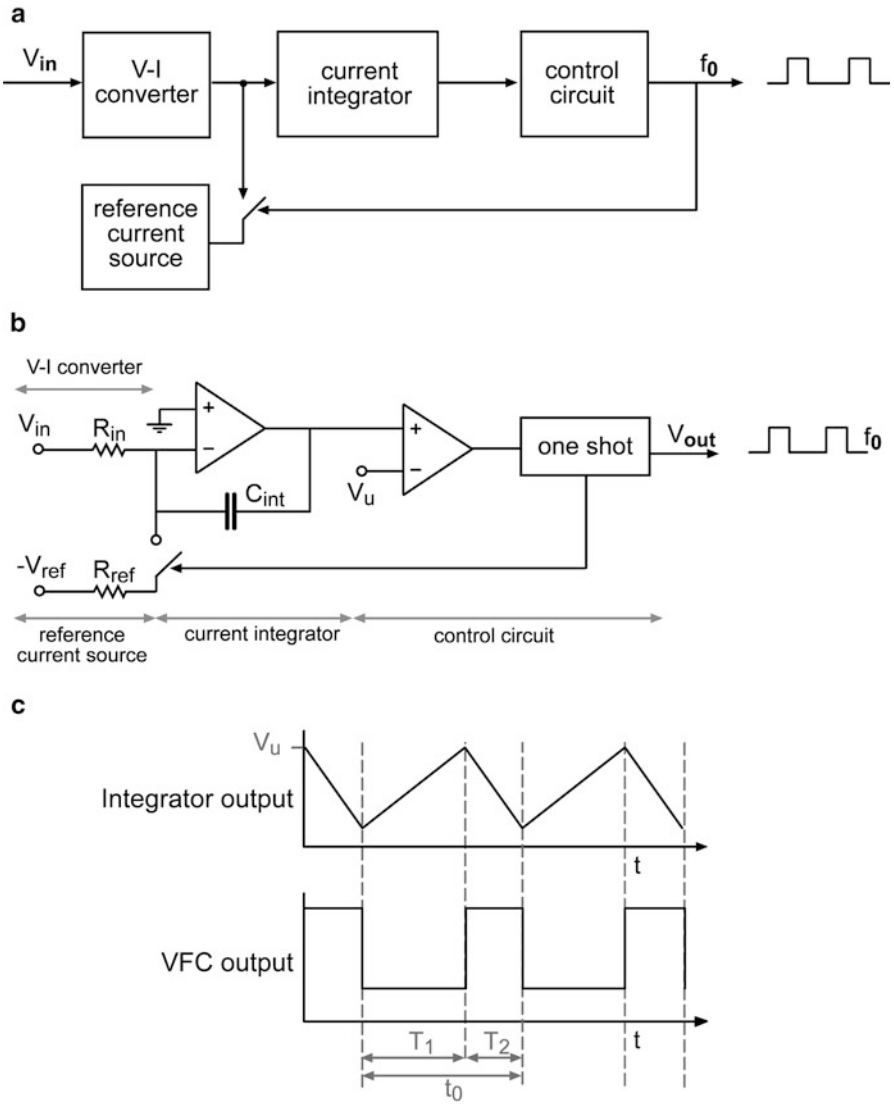

Fig. 2.4 Asynchronous charge-balance VFC: (**a**) block diagram, (**b**) typical implementation and (**c**) main voltage signals

depends on the capacitor stability) compromise the proper operation of the VFC. Temperature stability of the capacitor does not strongly affect the accuracy, but it does affect its dielectric absorption and leakages. At high frequencies second-order effects, such as switching transients in the integrator and in the monostable when being triggered shortly after the end of a pulse, affect the accuracy and the linearity [KES05].

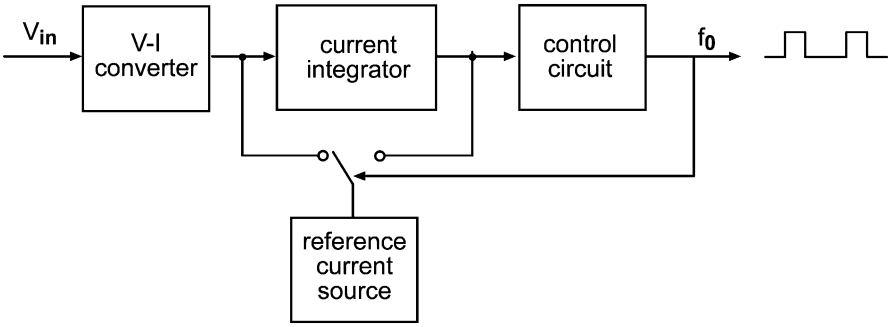

Fig. 2.5 Improved proposal of the asynchronous charge-balance VFC

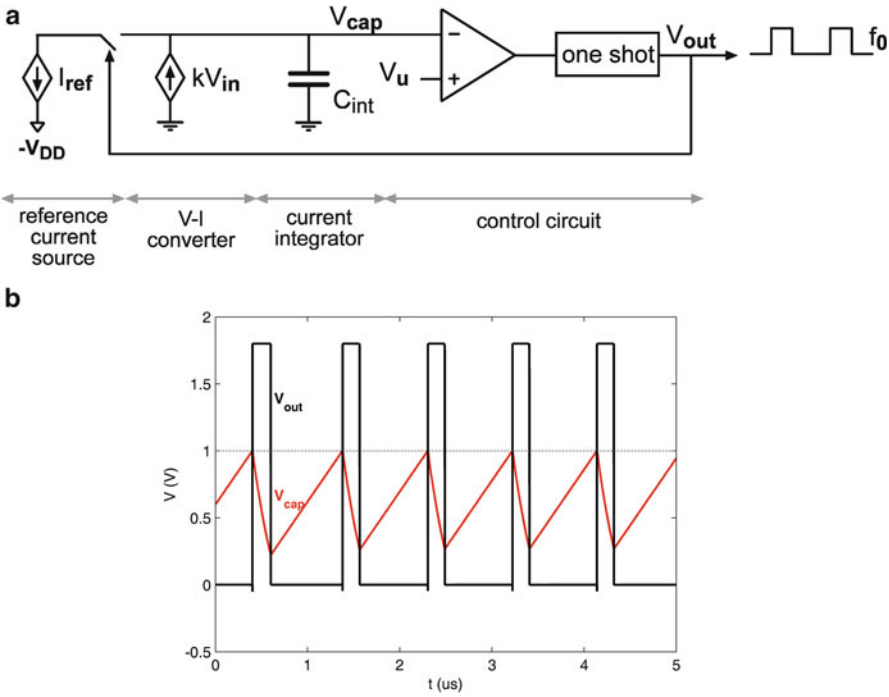

Fig. 2.6 Functional simulation of the asynchronous charge-balance VFC: (**a**) Schematics and (**b**) capacitor and output waveforms

To address the integrator transient problem, more recent charge-balance techniques introduce a changeover switch in the reference current source [ZUM08]: instead of having on/off transients, this current source is connected alternately to both sides of the integrator (see Fig. 2.5). With this change, the output stage of the integrator sees a constant load; most of the time the current from the source flows directly in the output stage. During the charge balance, it still flows in the output stage but through the integration capacitor.

The scheme shown in Fig. 2.6a was implemented to model the asynchronous charge-balance VFC in Fig. 2.4a. The input voltage V_{in} is converted into a current $I_{in} = kV_{in}$ with an ideal voltage-controlled current source. This current is integrated in a grounded capacitor C_{int}. The voltage across this capacitor is compared with a threshold voltage V_u in an ideal comparator. When the voltage across capacitor C_{int} reaches V_u, the output of the comparator changes and shoots the monostable. During T_2, the time that the monostable is active, a reference current I_{ref} is connected to the circuit, subtracting a fixed charge from the capacitor. When T_2 ends, the reference current is disconnected, starting the charging phase again. The output of the VFC is the output of the monostable.

Figure 2.6b shows the waveforms in the time domain at the integrating capacitor (V_{cap}) and at the output of the VFC (V_{out}), for $k = 10$ µS, $V_{in} = 1$ V, $C_{int} = 20$ pF, $I_{ref} = 50$ µA, $V_u = 1$ V, and $T_2 = 200$ ns with a symmetrical supply voltage of $V_{DD} = \pm 1.8$ V. The output frequency is 1 MHz according to (2.2).

Note that the required condition $|I_{ref}| > |I_{in}|$ to ensure the charge balance makes this type of VFCs to be typically biased with dual $\pm V_{DD}$ supply voltage, so that the input voltage swings from 0 to V_{DD}, whereas the reference current can be adequately generated using as a negative reference voltage $-V_{ref}$ and making the conversion into a current by means of a resistor R_{ref}, ($I_{ref} = -V_{ref}/R_{ref}$), as shown in Fig. 2.4b, which depicts the most widely used electronic implementation based on V-I converter with floating capacitor. For a single supply implementation, the input range would be reduced to $[\Delta V, V_{DD}]$, ΔV being the current source biasing voltage headroom.

2.2.3 Synchronous Charge-Balance VFC

The stability and the transient response of the monostable imply linearity problems in the charge-balance VFC. An alternative to the charge-balance VFC that solves this issue is the synchronous charge-balance VFC (SVFC), whose general diagram is shown in Fig. 2.7a: instead of a monostable, a bistable driven by an external clock is used. Thus, the linearity is increased, achieving around 18 bits and a high temperature stability, which makes them especially demanded for applications that require a high-resolution VFC [KES09]. A typical implementation of this kind of VFC is shown in Fig. 2.7b.

In this type of converters, as shown in Fig. 2.7c, the discharging phase does not start when the integrator output reaches the threshold voltage but with the next clock cycle. The output frequency expression is given by:

$$f_0 = \frac{I_{in}}{I_{ref}} f_{clk} \tag{2.3}$$

Hence, the SVFC output is synchronized with the clock, so it is easier to process it with external or internal microcontroller counters. However, as the output pulses are aligned with clock pulses, the output pulses are not equally spaced, which

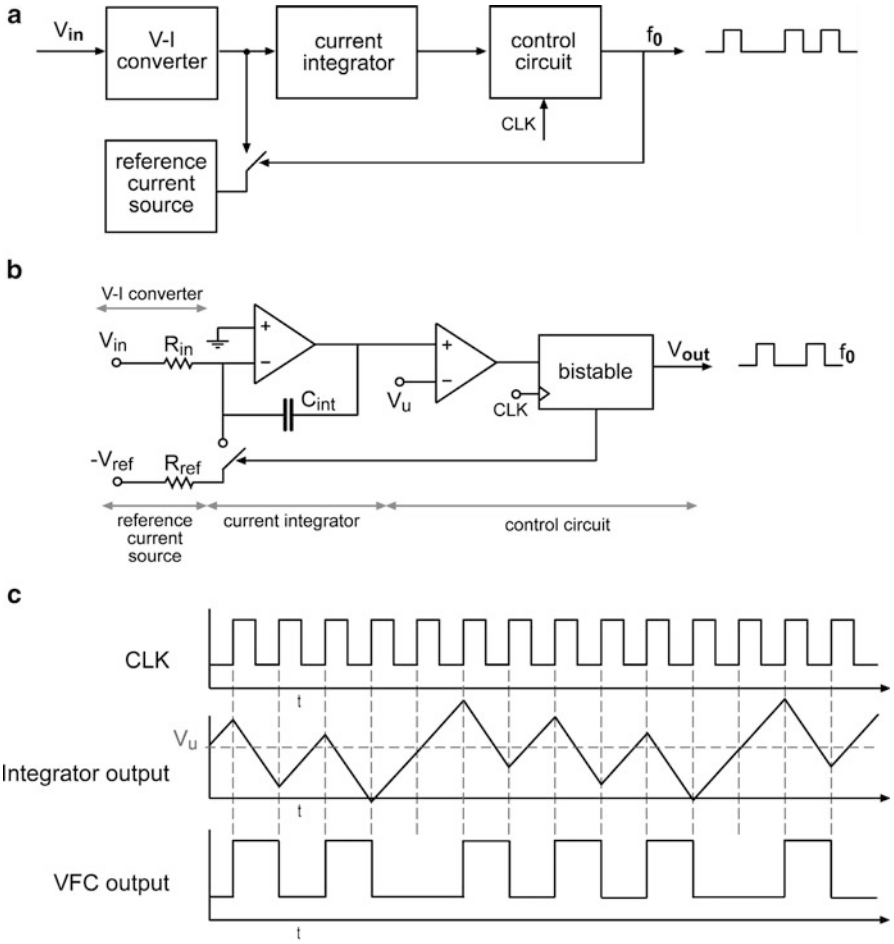

Fig. 2.7 Synchronous charge-balance VFC: (**a**) block diagram, (**b**) typical implementation and (**c**) main voltage signals

means that the output of a SVFC is not a pure tone like a conventional VFC, but contains components harmonically related to the clock frequency. This is a common cause of confusion when displaying the SVFC output on an oscilloscope because, in an asynchronous VFC, an increase in the input voltage is translated into an increase in the output frequency, whereas a change in a SVFC produces a change in the probability density of output pulses N and $N + 1$ clock cycles after the previous output pulse, which often is misinterpreted as severe jitter and a sign of a faulty device [KES05]. This might not affect the use of the SVFC as a part of an ADC, but it does when used as a precision oscillator. Another disadvantage appears close to subharmonic clock frequencies. This is due to the capacitive coupling of the clock into the comparator, which causes injection-lock effects, causing a small dead zone in its response [KES09].

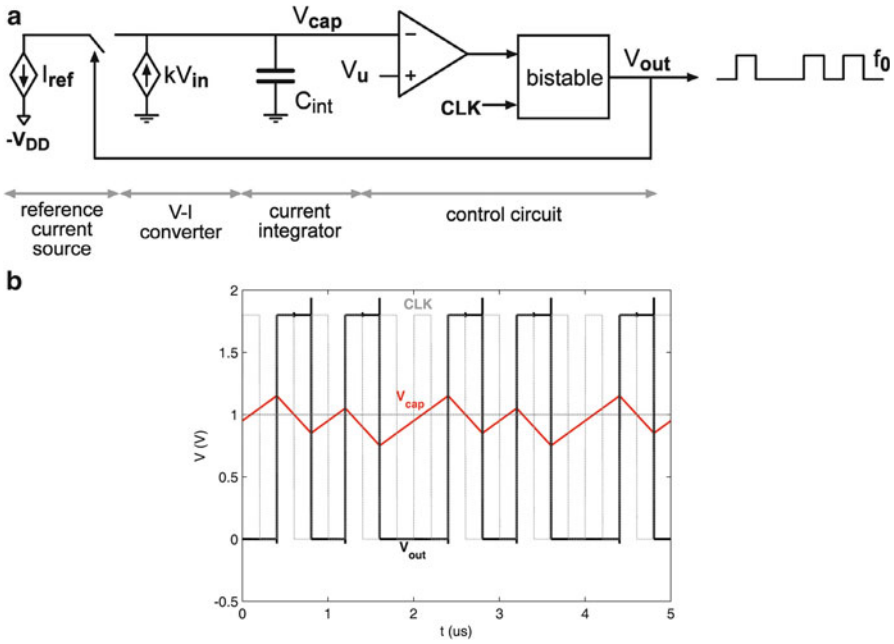

Fig. 2.8 Functional simulation of the synchronous charge-balance VFC: (**a**) Schematics and (**b**) capacitor, output and clock waveforms

Despite these disadvantages, the SVFC has better performances compared with the asynchronous approach, which makes it suitable for high resolution VFC applications and in multichannel systems because it removes problems of interference that can appear when having multiple asynchronous frequency signals [ZUM08].

The scheme shown in Fig. 2.8a was implemented to model the synchronous charge-balance VFC in Fig. 2.7a. As in the asynchronous VFC, the input voltage V_{in} is converted into a current $I_{in} = kV_{in}$ with an ideal voltage-controlled current source. This current is integrated in a grounded capacitor C_{int}. The voltage across the capacitor is compared with a threshold voltage V_u in an ideal single comparator. When the voltage across capacitor reaches V_u, the output of the comparator changes but, in contrast to what happens in the asynchronous approach, this time the current reference I_{ref} is not connected to the circuit until the next clock pulse comes, and therefore, the charge phase continues until the next clock pulse. Once the reference current is connected, a fixed charge is subtracted from the capacitor during a period of clock.

The waveforms at the capacitor and the output of the VFC are shown in the time domain in Fig. 2.8b, for $k = 10$ µS, $V_{in} = 1$ V, $C_{int} = 20$ pF, $I_{ref} = 25$ µA, $V_u = 1$ V and $f_{clk} = 2.5$ MHz with a symmetrical supply voltage of $V_{DD} = \pm 1.8$ V. The output frequency is 1 MHz according to (2.3). Note that, as in the asynchronous charge-balance VFC, to ensure the condition $|I_{ref}| > |I_{in}|$, the VFC is usually biased with symmetrical $\pm V_{DD}$ supply voltage being the input voltage [0, V_{DD}] and

the reference current $I_{ref} = -V_{ref}/R_{ref}$. So, again the input range would be reduced to $[\Delta V, V_{DD}]$ for a single supply implementation, ΔV being the current source biasing voltage headroom.

2.3 Frequency-to-Code Conversion Methods

When used as a building block in an ADC system, a VFC exhibits excellent accuracy and linearity. Besides, although VFCs are not fast converters (they are slower than successive approximation devices [FRA10] but comparable to integrating ADCs), by using efficient frequency-to-code conversion methods, a good speed-accuracy trade-off can be obtained [BUR94].

There are many methods of frequency-to-code conversion, such as the standard counting method, the indirect method, the interpolation method, the method of recirculation, or the reciprocal counting method [KIR02b, YUR08]. However, when set against others, the simplicity, high performance, and universality of the standard direct counting method and the indirect counting method have contributed to their popularity. This is why they have become the preferred methods despite some restrictions and faults [KIR02b]. Therefore, these two methods are going to be studied in this section.

2.3.1 Standard Direct Counting Method (DCM)

This method is a frequency measurement technique, and it consists in counting a number of pulses N_x of unknown frequency f_x (with a period T_x) during a fixed gate time T_W.

$$N_x = \frac{T_W}{T_x} = T_W f_x \tag{2.4}$$

Therefore, the unknown frequency f_x is given by:

$$f_x = \frac{N_x}{T_W} \tag{2.5}$$

Figure 2.9 shows the DCM time diagram. When applying this method there are two main errors, the quantization error δN_x, and the reference frequency error δf_W.

The quantization error is due to the lack of synchronization of the beginning and the end of the gate time (T_W) with pulses f_x. The practical time where pulse counting is performed is T'_W, determined by values Δt_1 and Δt_2:

$$T'_W = N_x T_x = T_W + \Delta t_1 - \Delta t_2 \tag{2.6}$$

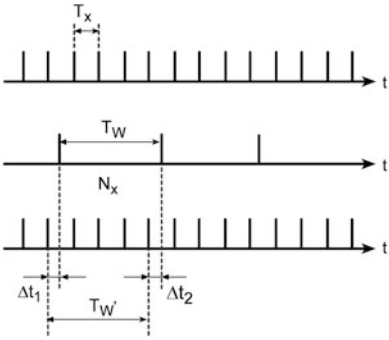

Fig. 2.9 Standard direct counting method time diagram [KIR02b]

So that T_W can be rewritten as

$$T_W = N_x T_x - \Delta t_1 + \Delta t_2 = N_x T_x \pm \Delta t \tag{2.7}$$

Time intervals Δt_1 and Δt_2 can change independently of each other, varying Δt from 0 to T_x. Then, the maximum relative quantization error caused by the absence of synchronization is $\delta N_x = \pm 1$ [KIR02b].

Concerning the reference frequency f_W, two different errors should be considered: (1) $\delta f_{W,ref}$ is a systematic error caused by inaccuracy of the initial tuning and the long-term instability of the generator frequency and is a fixed error, and (2) $\delta f_{W,T}$ is the deviation of the real frequency from the nominal value because of temperature variations in a non-temperature-compensated crystal oscillator. Therefore, the error δf_W can be expressed as

$$\delta f_W = \delta f_{W,ref} + \delta f_{W,T} \tag{2.8}$$

Now, since (2.5) is an indirect measure, the frequency error can be calculated by applying the error propagation method, which results in the following expression:

$$\delta f_x = \left[f_W^2 (\delta N_x)^2 + N_x^2 (\delta f_W)^2 \right]^{1/2} \tag{2.9}$$

If N_x is written in terms of f_W, and considering that δf_W can be computed as $\delta f_W = f_W \Delta.f_W$, where $\Delta.f_W$ is the f_W error per unit, the frequency error (2.9) related to f_x is given by

$$\frac{\delta f_x}{f_x} = \left[\frac{f_W^2}{f_x^2} (\delta N_x)^2 + (\Delta.f_W)^2 \right]^{1/2} \tag{2.10}$$

Analyzing (2.10), the reference error term is fixed and it is independent on the reference frequency, whereas the term related to the quantization error increases as

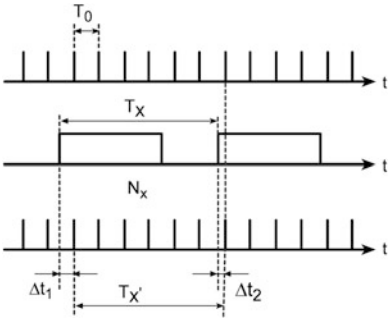

Fig. 2.10 Indirect counting method time diagram [KIR02b]

the unknown frequency decreases. In addition, focusing on δN_x, it can be negligible for high frequencies and significant for very low frequencies. Thus, this method is a right option to measure high frequencies. Effective methods for reducing the quantization error are: (a) opening a longer gate, kT_W, and (b) using weight functions; however, both choices result in an increase of the conversion time. One of the disadvantages of this classical method is the redundant conversion time in all frequency ranges, except for the nominal frequency [KIR02b].

One last thing that has to be taken into account is that, if the counter that is going to sum the number of pulses has a number of bits that is denoted by N, the gate time T_W required to have the maximum resolution depends on both the maximum and minimum frequencies to be measured, and is given by (2.11) [KLO12, PAL01a].

$$T_W = \frac{2^N}{f_{x,max} - f_{x,min}} \tag{2.11}$$

2.3.2 *Indirect Counting Method (ICM)*

This method is a period measurement technique, and it is commonly used for low or extra low frequencies. In this case, a number of pulses N_x of a reference frequency f_W (with period T_W) are counted during m periods of the unknown frequency f_x (with period T_x), as given in (2.12).

$$N_X = m\frac{T_x}{T_W} \tag{2.12}$$

Therefore, the unknown frequency f_x is given by

$$f_x = \frac{m}{N_x} f_W \tag{2.13}$$

Figure 2.10 shows the ICM time diagram. There are two main errors associated, the quantization error δN_x and the reference frequency error δf_W.

The quantization error is due to the lack of synchronization of the beginning and the end of the gate time, T_x, with pulses f_W. The practical time where pulse counting is done is T_x' whose absolute value is determined by values Δt_1 and Δt_2.

$$mT_x^{'} = N_x T_W = mT_X + \Delta t_1 - \Delta t_2 \tag{2.14}$$

Hence,

$$mT_X = N_x T_W - \Delta t_1 + \Delta t_2 = N_x T_W \pm \Delta t \tag{2.15}$$

Time intervals Δt_1 and Δt_2 can change independently of each other, varying Δt from 0 to T_W. Then, as in the DCM, the maximum relative quantization error caused by the absence of synchronization is $\delta N_x = \pm 1$ [KIR02b].

As has been explained in the previous method, for the reference frequency f_W two different errors have to be considered: (1) $\delta f_{W,ref}$ and (2) $\delta f_{W,T}$, so that the known frequency error δf_W is given by

$$\delta f_W = \delta f_{W,ref} + \delta f_{W,T} \tag{2.16}$$

and the final frequency error results in the following expression:

$$\delta f_x = \left[\left(\frac{f_x}{N_x} \right)^2 (\delta N_x)^2 + \left(\frac{m}{N_x} \right)^2 (\delta f_W)^2 \right]^{1/2} \tag{2.17}$$

If N_x is written in terms of f_W, and considering that δf_W can be computed as $\delta f_W = f_W \Delta.f_W$, where $\Delta.f_W$ is f_W error per unit, the frequency error (2.17), related to the working frequency, is given by

$$\frac{\delta f_x}{f_x} = \left[\left(\frac{f_x}{m f_W} \right)^2 (\delta N_x)^2 + (\Delta.f_W)^2 \right]^{1/2} \tag{2.18}$$

Analyzing (2.18), the reference error term is independent of the unknown error, and it is easy to see that the error grows as the unknown frequency f_x grows, and the error can be negligible for low frequencies. Thus, this method is the right option to measure low frequencies. Short time intervals cause a large quantization error. This can be reduced by: (a) increasing the reference frequency f_W and converting a greater number of intervals n or (b) with the interpolation method, which instead of an integer number of reference frequency periods filling out the converted time interval, fractional parts of this period reference pulse also are taken into account. The second method has a non-redundant conversion time, but it has a high quantization error in the medium and high frequency range [KIR02b].

In this case, if the counter that is going to sum the number of pulses has a number of bits denoted by N, the number of periods m of the unknown frequency f_x that the counter has to be active depends on the maximum frequency that is going to be measured, $f_{x,max}$, and is given by (2.19) [PAL01a].

$$m = \frac{f_{x,max}}{f_W} \, 2^N \tag{2.19}$$

2.4 Conclusions

In this chapter, the basic fundamentals of voltage-to-frequency converters have been introduced. First, to properly evaluate the performances of the different proposed VFCs, definition of key parameters has been performed. Next, the most common types of VFC, the multivibrator and the charge-balance VFC, have been reviewed, and finally, standard code-to-frequency conversion methods have been briefly explained.

This work is focused on the study of VFCs acting as a part of an analog-to-digital converter in sensor signal interface circuits within embedded microcontroller systems. In these systems, a quasi-digital converter can be used to digitize the sensor output signal, taking advantage of the microcontroller, which makes the final digitalization thanks to its internal clocks.

Particularly, in this book the VFCs are thought to be used in wireless sensor network nodes for environmental applications. For these networks, low-cost sensors that have usually around 8 – 10 bits accuracy are used. Therefore, the designed VFCs need only to have moderate accuracy. In addition, these networks are supplied with standard single supply batteries, typically 3 V. Thus, single-supply operation must be regarded, whereas low power is a must to extend battery life and, therefore, to maximize the operating life of the sensor node.

From the review of the most common VFC types in Sect. 2.2, and taking into account the requirements of moderate accuracy and single power supply, the proper starting point for the fully integrated VFC design seems to be a multivibrator VFC: it has a moderate 14-bit accuracy, which is good enough for our application, it is simpler than the charge-balance VFC, which means better low-voltage low-power compatibility, and its input range is not reduced with single voltage supply.

Reviewing the presented frequency-to-code conversion methods, the standard direct counting method is worse for low frequencies, whereas the indirect counting method does not work well for high frequencies. To use the proposed VFCs with an only frequency-to-code conversion method to simplify the microcontroller internal code, and considering that the VFC output frequencies have to be compatible with the microcontroller clock frequency, typically around 4 MHz, the standard direct counting method is the most suitable method. Therefore, to minimize the error in measuring low frequencies related to this method, an offset frequency will be added to the VFC to achieve an optimum output range $[f_{0,min}, f_{0,max}]$ for performing the digitalization.

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