

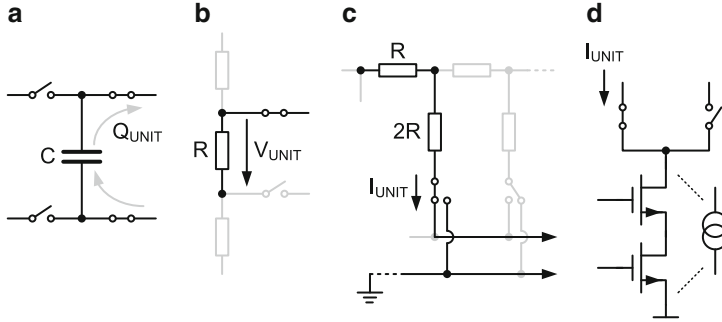
# Chapter 1

## Introduction

### 1.1 Integrated D/A-Converters

A digital-to-analog converter (DAC) is designed to perform an accurate summation of a given number of electrical unit quantities. This number is specified by the *digital* input code applied to the converter. The result of the summation appears as an *analog* electrical signal at the converter output. Thus, the output signal of the DAC represents, with more or less accuracy, the digital input code in the analog domain and can be further processed by subsequent analog circuitry, e.g., filters, amplifiers, mixers, or transducer interfaces. Fundamentally, it is the summing operation of appropriate electrical unit quantities that marks the actual transition from the digital into the analog domain. This data conversion process is also subject to a number of error sources that introduce distortion, as well as additional noise, into the analog output signal. Since these nonideal effects tend to limit the performance of practical converters, they should be adequately considered already during the design phase. The modeling of conversion inaccuracies is believed to be of central importance for close-to-optimum, system-specific DAC design. Indeed, a large part of this work is dedicated to providing theoretical insight into fundamental nonidealities of integrated D/A-converters with a focus on the current-steering architecture and, wherever appropriate, linking it to the system-level perspective.

The DAC unit cell comprises one or more primary circuit elements that generate the summable electrical unit quantity in the first place, as well as a couple of analog switches that allow to connect the unit cell to common circuit nodes within the converter. Primary circuit elements in integrated converters are capacitors, resistors, or transistors. Important types of DAC unit cells used in integrated converters are shown in Fig. 1.1. The complete D/A-converter is eventually constructed using a suitable number of such unit cells, together with a couple of auxiliary circuits required for proper operation of the DAC. Auxiliary circuits include, e.g., biasing and clocking circuits, an output stage interfacing the converter to subsequent analog processing blocks, decoders and control circuitry, as well as digital interfaces.

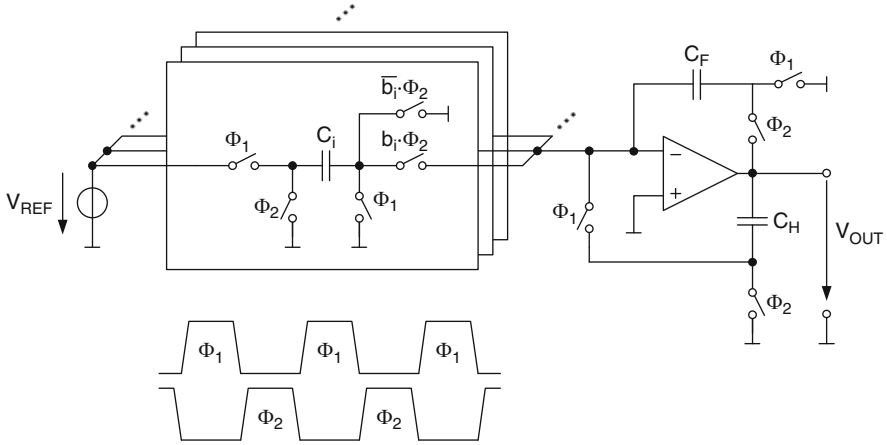


**Fig. 1.1** DAC unit cell types: (a) charge, (b) voltage, (c) current, and (d) current

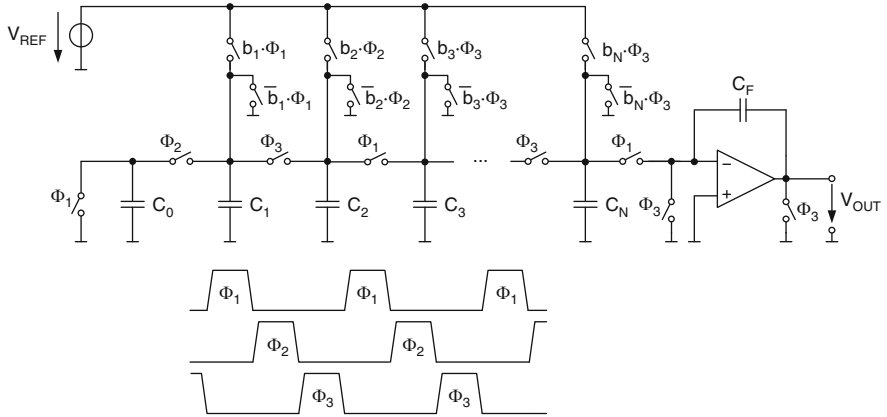
In general, a D/A-converter can have a voltage or a current output, depending on the type of input the circuitry connected to the converter provides. In high dynamic range AFEs the preferred method for analog signal interfacing is usually voltage mode, which in turn requires the D/A-converter to perform an accurate conversion from the previously summed up primary electrical quantity into the corresponding output voltage. In other circumstances, the electrical unit quantity is already available as a voltage, but a direct connection to the load would destroy the accuracy. In such cases, the data converter must include a sufficiently low-noise and linear voltage buffer.

Charge-based D/A-conversion is performed by storing electrical unit charges  $Q_{UNIT}$  on an array of integrated capacitors (Fig. 1.1a) and appropriately redistributing them onto a summation capacitor. Such converters are called Switched-Capacitor DACs and are especially popular as subsystems in more complex integrated MOS A/D-converters [1]. The main reason is that MOS technologies offer high-quality and easy-to-drive switches. Equally important, many integrated capacitor types are very linear<sup>1</sup> and can be laid out to exhibit good matching behavior [2]. Switched-capacitor DACs are also found as stand-alone building blocks, especially for high-resolution, low-frequency applications, e.g., in audio front ends [3, 4]. Figure 1.2 shows the principle of a multibit Switched-Capacitor DAC [5]. The charge stored on the unit capacitors  $C_i$  in phase  $\Phi_1$  is transferred to capacitor  $C_F$  during phase  $\Phi_2$ , provided that the corresponding input bits are set, i.e.,  $b_i = 1$ . The charges of those capacitors  $C_i$ , for which  $b_i = 0$ , are instead dumped to ground in phase  $\Phi_2$  and do not contribute to the output signal. The low-impedance node required for complete charge transfer from  $C_i$  to  $C_F$  is provided by the virtual ground node of the operational amplifier. The output voltage at the end of phase  $\Phi_2$  is additionally stored on the holding capacitor  $C_H$ , which is then put in the feedback of the operational amplifier during the subsequent phase  $\Phi_1$ .

<sup>1</sup>An exception are diffusion- and MOS-based capacitors, which display a relatively strong voltage dependency. High-precision converters therefore tend to use poly-poly, poly-metal and metal-metal structures to form integrated capacitors.



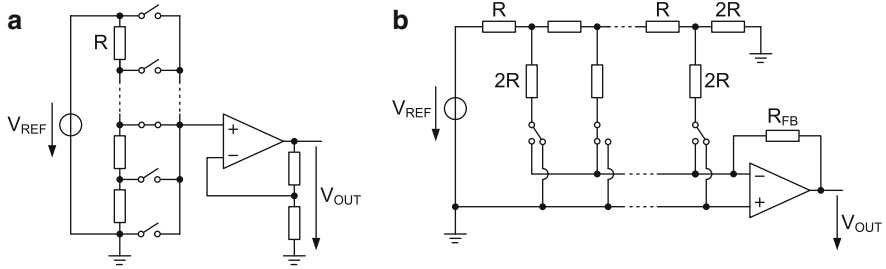
**Fig. 1.2** Multibit parallel switched-capacitor DAC



**Fig. 1.3** Multibit pipelined switched-capacitor DAC

This clock phase is also used to precharge the unit capacitors  $C_i$  to  $V_{REF}$  and discharge the summing capacitor  $C_F$ , in effect preparing the converter for the next conversion cycle, while the actual output voltage is held on  $C_H$ .

Another approach is the pipelined switched-capacitor DAC [6] shown in Fig. 1.3. Using only  $N + 1$  identical capacitors  $C_0 - C_N$ , an  $N$ -bit converter can be constructed, which is very area efficient. The operating principle is in some sense similar to a charge-coupled device (CCD), but with additional input-code-dependent precharging of the single capacitors. Using three clock phases and appropriately delayed input bits, the binary-weighted output charge corresponding to the digital input word is building up by successive charge redistribution along the capacitor pipeline. The reconstructed “analog” charge on the last capacitor  $C_N$  can finally be transferred to the output via a SC-amplifier. Drawbacks of this DAC architecture



**Fig. 1.4** Basic resistor-DAC types: (a) R-string and (b) R-2R multiplying DAC

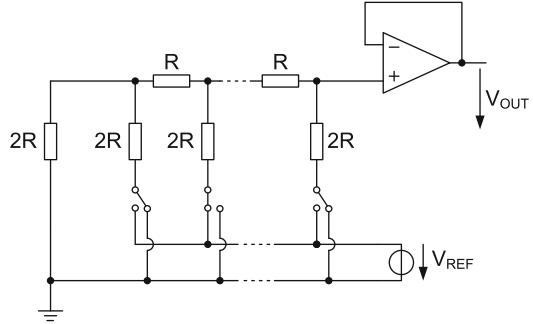
are the latency of  $N + 2$  clock cycles and, possibly, a certain limit on the achievable resolution due to error progression along the capacitor pipeline. Nevertheless, due to the pipelining of the conversion process, it allows operation at respectably high sampling rates, as demonstrated for example in [7].

Integrated matched resistors can be arranged either as a programmable voltage divider (Fig. 1.1b), also called resistor string, or as a programmable current divider in the form of an R-2R ladder (Fig. 1.1c). In the voltage divider case, the output node must display a sufficiently high impedance compared to the total resistance of the string. Since the output impedance of a tapped resistor string depends on the actual position of the tap, the voltage distribution within the resistor stack is (code-dependently) disturbed, in case a significant current is flowing into the output. In the current divider case, on the other hand, the output node must be of very low impedance, otherwise the current distribution within the R-2R ladder will depend on the actual setting of the switches, i.e. on the digital input code. In practical implementations, both types of resistor-based D/A-converters require not only a precise voltage reference driving the resistor array but also a high-quality operational amplifier as output stage.<sup>2</sup> This amplifier either serves as a high-impedance voltage amplifier/buffer in the string-type converter, or it provides the low-impedance current-summing node for the current divider, along with the implicit current to voltage conversion using resistive feedback.

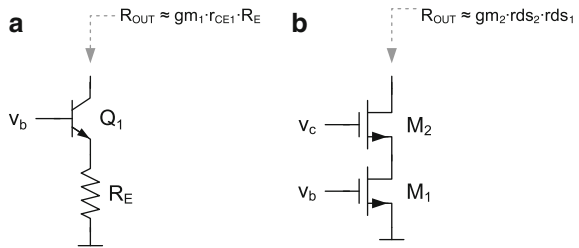
Figure 1.4 shows the two basic resistor-type DACs in greater circuit-level detail. Figure 1.4a shows the resistor string DAC or string-DAC [8]. The converter in Fig. 1.4b with accessible reference voltage  $V_{REF}$  is called R-2R multiplying DAC [9], owing to the fact that the output voltage is the product of the reference voltage and the digital input code [10], both applied externally. With the amplifier configured as a voltage buffer, the R-2R ladder can also be tapped in voltage mode, as shown in Fig. 1.5. In this case, the ladder behaves like a programmable voltage divider. Such an arrangement is called voltage-mode R-2R ladder DAC [10], sometimes also R-2R back-DAC [11].

<sup>2</sup>This is certainly true for general purpose instrumentation applications. However, for on-chip control applications with known suitable loading a dedicated op-amp is often not necessary.

**Fig. 1.5** Voltage-mode R-2R DAC (R-2R back-DAC)



**Fig. 1.6** Transistor-based current sources: (a) BJT and (b) MOS

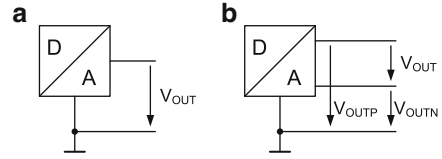


As stand-alone converters, resistor-based DACs are heavily used not only in instrumentation and control applications but also in high-end digital audio products [12–14]. In conjunction with resistor (and reference) trimming, these converters can achieve exceptional accuracy, linearity, and long-term stability at very low power dissipation [15, 16]. The signal bandwidth covered by resistor-based D/A-converters is normally quite small, nevertheless sufficient for the usual target applications. A notable exception that covers video bandwidths, albeit displaying also considerably less resolution, can be found in [17].

Integrated current sources based on active elements require at least one transistor operated in the active region (Fig. 1.1d). In most cases, either resistive degeneration or cascoding is employed to further boost the output resistance to sufficiently high values. Traditionally, bipolar designs tend to use resistive emitter degeneration, while MOS current sources are normally in favor of cascoding. Both techniques are shown in Fig. 1.6. Extensive treatments of integrated current sources can be found in reference texts on integrated analog circuit design; see, e.g., [5, 18–20]. D/A-converters built with active current sources are called current-steering DACs because the unit cell currents must not be turned on and off. Instead, they have to be *steered*, rather cautiously, to the appropriate summing node(s) in order not to disturb the potentially delicate biasing required for these circuits. Current-steering DACs implemented in CMOS-technologies are the main subject of this book and described in more detail starting from Sect. 1.4.

In general, every unit cell contains at least one high-accuracy switch. This switch connects the unit cell, when triggered by the digital input code, to an appropriate common node within the converter circuitry, where, e.g., the summation of the electrical unit quantities occurs. Differential architectures (see below) have two

**Fig. 1.7** Single-ended (a) and differential output (b) DAC



output nodes, obviously requiring at least two high-accuracy switches within each unit cell. Additional switches may be needed to establish a proper behavior of the unit circuit element during subsequent conversion cycles. For example, in charge-based converters, as described above, the unit capacitors must be correctly precharged prior to each summation operation.

In a D/A-converter, the unit cells need not necessarily be all of the same type. Nevertheless, true hybrid D/A-converters are not very common, an example using voltage division plus charge redistribution is reported in [21]. On the other hand, resistor-based current division of transistor current sources appears to be quite popular in bipolar designs [22–24], because it allows the construction of a true binary-weighted current-cell array, while employing only equal-sized current source transistors. This architecture has already been used<sup>3</sup> in the feedback DAC of EPSCO’s 1954 11-bit 50 kS/s SAR-ADC (the “DATRAC”), an all-valve 500 W (!) A/D-converter system [10, 25].

On a more architectural level, we can distinguish between single-ended output and differential output D/A-converters; see Fig. 1.7. Single-ended output DACs are mostly found in low-frequency instrumentation and control applications, whenever the output node is single-ended by definition. Differential output DACs, on the other hand, are nowadays the primary choice for dynamic signal synthesis, whenever the spectral purity, i.e., the signal quality with respect to noise and distortion, is of primary importance. According to common understanding, this has to do with the doubled signal swing of differential architectures, leading to 3 dB better signal to noise performance. Additionally, defining the output signal as being the difference of two single-ended, opposite polarity signals<sup>4</sup> has the tendency to suppress even-order harmonic distortion, as well as providing a certain immunity against disturbance and noise present on common circuit nodes, e.g. the supply rails. Note, also, that any differential output DAC can be converted into a single-ended DAC by using only one of its two output nodes and discarding the other. Of course, by doing so, any previously present common-mode rejection is given up on as well.

On system level we can distinguish between Nyquist-rate and noiseshaped D/A-converters. Nyquist-rate converters exhibit a flat quantization noise spectrum (see Sect. 2.3.1), and, in principle, allow to exploit the full converter bandwidth for signal synthesis. Since virtually all communication systems require a certain

<sup>3</sup> According to [10] for the first time in data converter history.

<sup>4</sup> The two single-ended signals in a differential configuration are opposite in polarity relative to a fixed common-mode level above on-chip ground. Ideally, the differential output appears floating with respect to any fixed ground-referenced potential.

amount of oversampling, e.g., to facilitate the necessary analog filtering, in practical applications, only a certain fraction of the full Nyquist bandwidth, as defined by half the sampling rate, is actually used.

Noiseshaped D/A-converters, on the other hand, try to concentrate the major part of the quantization noise outside of the signal bandwidth of interest, thereby greatly improving the in-band resolution. As a consequence, they can only be used for signal synthesis within a relatively small fraction of the Nyquist bandwidth. Noiseshaped D/A-converters are also called  $\Sigma\Delta$ -DACs.

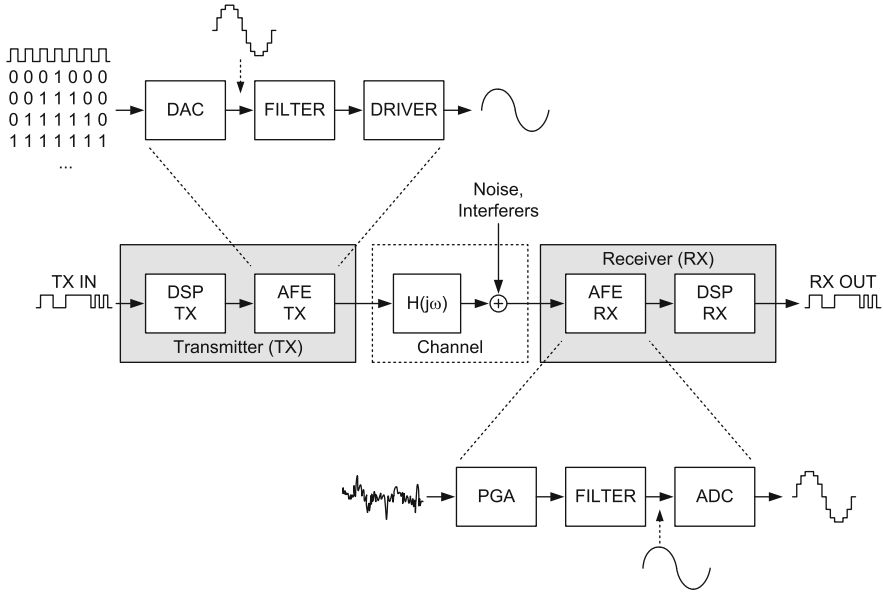
The MOS-transistor based, current-steering, and differential output converter topology (see Sect. 1.4) has become the most prominent DAC architecture for signal synthesis in communication systems, because it offers high-speed and high-accuracy capability at moderate power consumption. Whether oversampling, or even noiseshaping is employed, largely depends on the overall system specification, because these decisions usually have a rather big influence on the overall AFE architecture. In any case, current-steering D/A-converters can be realized quite straightforwardly, even in standard digital CMOS processes, and are easily combined with a fair amount of digital circuitry, e.g., to control DAC-element shuffling or calibration algorithms. This “digital assistance” is used extensively in the hardware examples in later chapters of this book, with the goal to improve the converter performance, while keeping the required silicon area small.

## 1.2 DACs for Highly Integrated Transceivers

Digital communication systems have become an integral part of the infrastructure in our modern information society. Although the bulk of the signal processing is already done in the digital domain, still the transmission medium, or channel, across which the connection of the so-called data link is finally established, is analog by nature [26]. Therefore, the digital data must be converted into an appropriate analog signal by the transmitter and back into digital data samples by the receiver.

Figure 1.8 shows a generic (unidirectional) digital communication link. In the transmitter (TX) a digital signal processor (DSP) performs the necessary coding and modulation of the input bit stream. In the AFE the encoded digital data is then converted into an analog signal by a DAC. After suitable filtering and power amplification, the analog transmit signal is finally applied to the channel.

The input signal of the receiver (RX) consists of the attenuated and spectrally distorted wanted signal together with noise and interferers. This composite signal is first amplified by a programmable gain amplifier (PGA), then filtered, and subsequently converted back into a digital signal by an analog-to-digital converter (ADC). Only then can the DSP in the receiver recover the original bit stream sent by the transmitter down through the channel. For bidirectional (duplex) operation a complete receiver and transmitter module must be implemented at both data terminals. This combination of *transmitter* and *receiver* is often called *transceiver*. If transmitter and receiver are active at the same time, i.e.,



**Fig. 1.8** Digital communication link

a bidirectional data link is established simultaneously, we speak of full-duplex operation, whereas in so-called half-duplex systems transmitter and receiver are active and transmitting/receiving only alternately. A typical example for full-duplex systems is the current xDSL-families using DMT modulation, while today's WLAN-standards and most PLC-systems operate in half-duplex.

In wireless systems we additionally find an analog mixer in the transmitter for spectral upconversion of the signal to the desired center frequency. In the corresponding receiver there is at least one analog mixer for downconversion of the antenna signal, either directly to the baseband frequency, or first to some intermediate frequency for further amplification and filtering, before the signal is downconverted to the baseband and digitized by the ADC [27]. In case the A/D-converter is able to sample the signal at an intermediate frequency (IF), the final downconversion can also be performed in the digital domain [28].

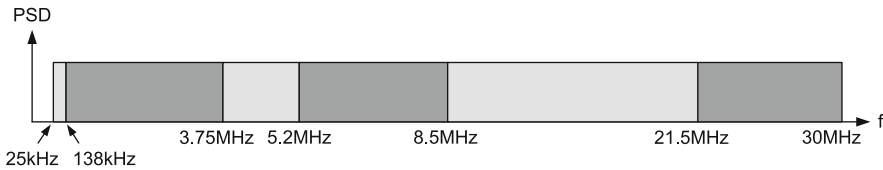
In any case, the two inverse data conversion operations in the analog front-end (AFE), D/A in the transmitter and A/D in the receiver, constitute very central signal processing functions that can be found in every digital communication system. The fidelity with which the data conversion can be accomplished on either side of the analog channel has an immediate impact on the quality of the data link. Therefore, considerable effort is spent in optimizing the performance of the data converters in the context of a limited power budget and silicon area constraints. These boundary conditions tend to become especially stringent in multi-channel integration, where multiple transmit and receive channels must be integrated together on the same silicon die.



ADSL:



VDSL2 (30a profile):



**Fig. 1.9** DSL frequency-band plan examples

Special difficulties also arise when a single AFE-design must cover multiple transmission standards with considerably different bandwidth and linearity specifications. This feature is sometimes called multi-mode capability. As an example, Fig. 1.9 shows exemplary frequency band plans for two popular digital subscriber line (DSL) standards. The asymmetric digital subscriber line (ADSL) standard employs a single upstream and downstream<sup>5</sup> band from 25 kHz up to 138 kHz and from 138 kHz up to 1.1 MHz, respectively. On the other hand, the very high-speed digital subscriber line (VDSL) revision 2 system (30a profile in this example) uses a spectrum that is split into several interleaved upstream and downstream bands in the frequency range between 25 kHz and 30 MHz [29]. In practice, a myriad of different, even country-specific DSL-standards and substandards exist, all with different frequency band plans and sometimes even different transmit power masks.

The resolution and linearity requirements for the ADSL and VDSL system are also strongly differing. While ADSL requires around 14-bit performance, 11–12 bits are generally sufficient for VDSL, depending on the amount of out-of-band filtering and echo attenuation achieved for a given loop. Including enough flexibility into the analog building blocks to cover strongly differing operating modes, while still maintaining close-to-optimum silicon area and power consumption, considerably complicates the design of a multimode AFE.

<sup>5</sup>In wireline systems “upstream” is the data transfer from customer premises equipment (CPE) to central office (CO). “Downstream” is the reverse direction.

**Table 1.1** D/A-converter requirements for digital communication systems

System	Signal bandwidth	Resolution	Sampling rate
WLAN 802.11a/g	10 MHz	8 bit	80 MS/s
WLAN 802.11n	20 MHz	9 bit	160 MS/s
Bluetooth 2	2 MHz	10 bit	13 MS/s
Cable modem	8 MHz	10 bit	160 MS/s
1000Base-T	62.5 MHz	5 levels	125 MS/s
ADSL	1.1 MHz	14 bit	100 MS/s
ADSL2	2.2 MHz	14 bit	100 MS/s
VDSL2	30 MHz	11–12 bit	200 MS/s
PLC	30–100 MHz	11 bit	400 MS/s

In many situations the accuracy of the analog signal synthesis in the transmitter limits the maximum bitrate for a given loop length of the data link. In full-duplex systems with frequency division multiplexing (FDM) noise and distortion generated in the transmitter can eventually leak into the near-end receive path and limit the achievable signal-to-noise ratio (SNR) in the ADC, which is trying to digitize the signal from the far-end transmitter. This problem is especially encountered in systems with interlaced or even partly overlapping transmit and receive spectra, e.g., in DSL. Consequently, the D/A-converter in the transmitter of a digital transceiver is a very important building block with considerable impact on the overall system behavior.

In Table 1.1 coarse performance specifications for the TX-DAC of different digital communication systems are reported. Note, that the actual choice of the physical resolution and the sampling rate of the data converters may vary in different implementations. For example, it may be advantageous to run the D/A-converter at a higher clock rate, since this generally relaxes the order of the analog reconstruction filter that follows the DAC in the transmit chain. Although a higher sampling rate means a somewhat higher power consumption in the DAC, this is eventually overcompensated by a much simpler analog filter. On the other hand, the last stage of the digital interpolation filter preceding the DAC then also has to run at a higher clock rate. Likewise, it is in general more difficult to achieve a certain performance level, if the DAC is run at a higher sampling rate, because nonideal effects generated by the switching of DAC-elements will occupy a larger relative portion of the sampling interval. A careful optimization of the AFE-architecture is therefore mandatory to optimize the area and power consumption of the overall transceiver for a given performance target.

D/A-converters for modern digital transceivers are almost exclusively designed in advanced CMOS technologies. The main reason for this choice is that CMOS allows the data converters to be integrated together with analog and RF circuits, as well as a powerful DSP. This highest possible level of integration is often termed system-on-chip (SoC). To simplify the system integration, DAC-modules designed for the transmit path of digital transceivers must be fully embeddable macros and preferably run from a single supply with lowest possible power dissipation.

### 1.3 The Ideal D/A-Converter

As already stated previously, a DAC generates an analog output signal by summing together as many electrical unit quantities as represented by the actual digital input code. The electrical unit quantity can be a voltage, current, or an electrical charge, and it is usually derived from a reference circuit, e.g., a bandgap voltage. We can write a B-bit binary digital input code vector  $d$  as a weighted sum of the input bits  $b_i$  that constitute the digital word:

$$d = \sum_{i=0}^{B-1} 2^i \cdot b_i \quad b_i \in [0, 1]. \quad (1.1)$$

The bit with the smallest weight ( $b_0$ ) is called the least significant bit (LSB), while the bit with the largest weight ( $b_{B-1}$ ) is called the most significant bit (MSB). An ideal B-bit D/A-converter, fed with the digital input code of Eq. (1.1), produces an output signal  $u$  given by

$$u = \Delta \cdot \sum_{i=0}^{B-1} 2^i \cdot b_i. \quad (1.2)$$

$\Delta$  is the smallest output step that the D/A-converter can perform. It is commonly called the unit quantity or LSB-quantity. The maximum and minimum value that the output signal can assume is called positive and negative full-scale (FS) value, respectively. The difference between these two values is called the full-scale range (FSR) of the converter:

$$\text{FSR} = \Delta \cdot (2^B - 1). \quad (1.3)$$

According to Eq. (1.2) the output of the D/A-converter can only take on integer multiples of the unit-quantity  $\Delta$ . This discretization of the amplitude range is a fundamental property of digital signal processing and commonly called quantization. Likewise, the difference between a continuous-amplitude signal and its quantized counterpart is called the quantization error. For an ideal converter the quantization error is always in the range of  $-\frac{1}{2}\Delta$  and  $+\frac{1}{2}\Delta$  and is essentially a nonlinear error [30]. However, if the amplitude range of a quantized signal comprises many LSB-levels and the signal is not correlated with the quantization error, then we can treat it, to a good approximation, as noise [31]. This quantization “noise” obviously becomes smaller when the LSB-size is decreased relative to the full-scale range, meaning that the resolution of the converter is being increased. Note that the quantization error is not introduced by the ideal D/A-converter itself, still it is a fundamental limitation to the accuracy with which an analog signal can be reproduced. The relationship between the amplitude quantization and the achievable converter resolution is further explored in Sect. 2.3.1.

Digital signals are not only discrete in amplitude, but also discrete in time. As such, they are only defined at equidistant sampling instants, spaced  $T$  seconds apart.

$T$  is called the sampling clock period, sampling period, or clock period. In practice, a D/A-converter must hold the corresponding output value for a significant fraction of the sampling period, in order to deliver sufficient signal power to the load.

### 1.3.1 The Non Return-to-Zero DAC

We define the unit impulse response of an ideal non return-to-zero (NRZ) D/A-converter,  $p_{\text{NRZ}}(t)$ , to the (digital) Dirac sequence  $\delta_k$  as a perfectly rectangular pulse with the height of 1 LSB and a duration  $T = 1/f_{\text{CLK}}$ . In the following, we normalize the LSB-size  $\Delta$  to 1, such that

$$p_{\text{NRZ}}(t) = \text{rect}\left(\frac{t - \frac{T}{2}}{T}\right). \quad (1.4)$$

The standard  $\text{rect}()$ -function is defined to be equal to 1 if its argument is between  $-\frac{1}{2}$  and  $+\frac{1}{2}$ , and 0 otherwise. The DAC unit pulse in Eq. (1.4) is additionally shifted by half a clock period to the right on the time-axis in order to make the sampling instants fall on integer multiples of  $T$ . The ideal time-domain analog output  $u_{\text{NRZ}}(t)$  is given by multiplying the input data sequence  $d_k$  with the ideal unit impulse response  $p_{\text{NRZ}}(t)$  of the D/A-converter:

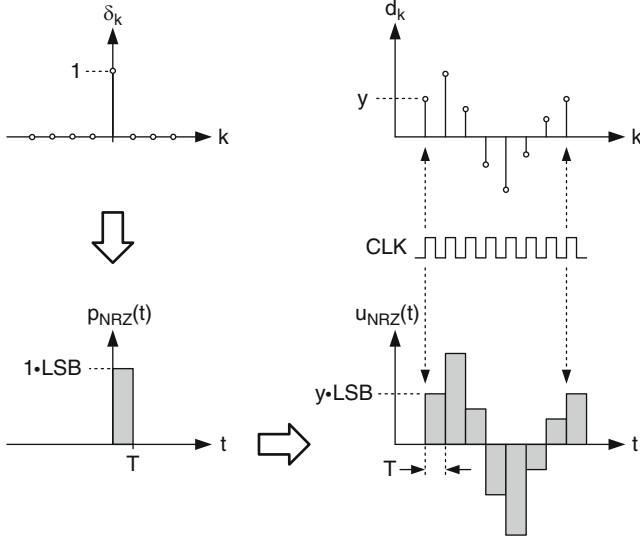
$$u_{\text{NRZ}}(t) = \sum_k d_k \cdot p_{\text{NRZ}}(t - k \cdot T) = \sum_k d_k \cdot \text{rect}\left(\frac{t - k \cdot T - \frac{T}{2}}{T}\right). \quad (1.5)$$

The digital input code sequence  $d_k$  can assume only integer values and is updated with the sampling clock of frequency  $f_{\text{CLK}} = 1/T$ . The output of the ideal NRZ D/A-converter is a staircase signal whose value stays constant within the whole sampling period  $T$ ; see Fig. 1.10.

Equation (1.5) can also be written as the convolution of the continuous-time signal  $d(t)$ , which has been “sampled” (multiplied) with the Dirac comb, and the unit impulse response  $p_{\text{NRZ}}(t)$  [26]:

$$u_{\text{NRZ}}(t) = \left[ d(t) \cdot \sum_k \delta(t - k \cdot T) \right] * p_{\text{NRZ}}(t). \quad (1.6)$$

At first,  $d(t)$  is a purely hypothetical continuous-time signal that corresponds exactly to the digital input code sequence  $d_k$  at the sampling instants  $t = kT$ , but could take on arbitrary values elsewhere. A more likely scenario, however, consists in  $d(t)$  being a real-valued continuous-time signal obeying the Nyquist criterion, which has been digitized by an ADC. In this case Eqs. (1.5) and (1.6) formalize the reconstruction process using an ideal NRZ-DAC.



**Fig. 1.10** Ideal DAC output signal

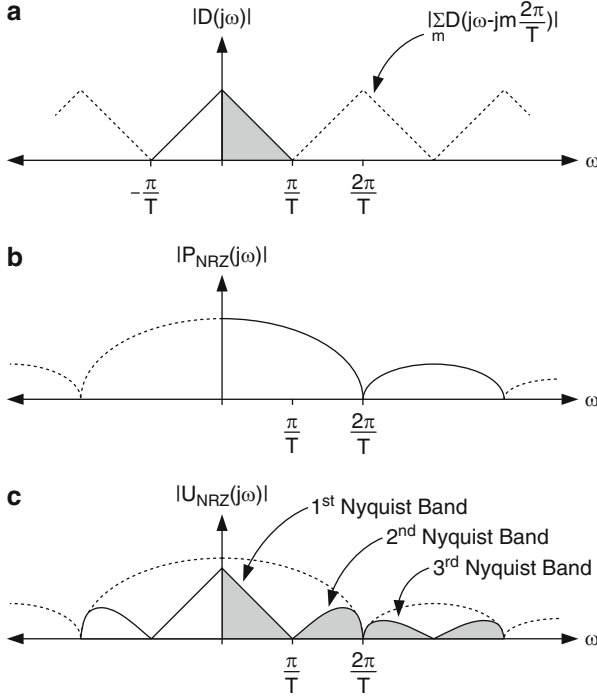
In the frequency domain, Eq. (1.6) is equivalent to the product of the repetitive spectrum of the input signal  $d(t)$ , as obtained by the ideal sampling process, and the Fourier transform of the ideal unit pulse  $P_{\text{NRZ}}(j\omega)$ .

$$U_{\text{NRZ}}(j\omega) = \frac{1}{T} \sum_m D \left( j \left( \omega - m \frac{2\pi}{T} \right) \right) \cdot P_{\text{NRZ}}(j\omega). \quad (1.7)$$

The Fourier transform of the ideal rectangular unit impulse response of Eq. (1.4) is given by

$$p_{\text{NRZ}}(t) = \text{rect} \left( \frac{t - \frac{T}{2}}{T} \right) \quad \longleftrightarrow \quad P_{\text{NRZ}}(j\omega) = T \cdot \frac{\sin \frac{\omega T}{2}}{\frac{\omega T}{2}} \cdot e^{-j\frac{\omega T}{2}}. \quad (1.8)$$

The ideal NRZ-DAC thus represents a zero-order hold (ZOH) [31]. Its transfer function is the well-known  $\sin(x)/x$  or  $\text{sinc}(x)$  function, with zeros at multiples of  $f_{\text{CLK}}$ . Figure 1.11a shows the spectrum of the original signal  $d(t)$ , before and after sampling. According to the Nyquist–Shannon theorem [26], only signals with a bandwidth smaller than  $\frac{1}{2}f_{\text{CLK}}$  can be reconstructed unambiguously after being sampled with  $f_{\text{CLK}}$ . Therefore,  $\frac{1}{2}f_{\text{CLK}}$  is also called the Nyquist frequency. Figure 1.11b displays schematically the ZOH transfer function  $P_{\text{NRZ}}(j\omega)$ , and Fig. 1.11c shows the spectrum of the reconstructed signal at the output of an ideal NRZ DAC,  $U_{\text{NRZ}}(j\omega)$ . At the Nyquist frequency  $\frac{1}{2}f_{\text{CLK}}$  the sinc function introduces an amplitude error of  $2/\pi$ , corresponding to  $-3.92$  dB.



**Fig. 1.11** Spectrum of ideal NRZ DAC: (a) (Repetitive) input spectrum, (b) NRZ DAC unit pulse spectrum, and (c) NRZ DAC output spectrum

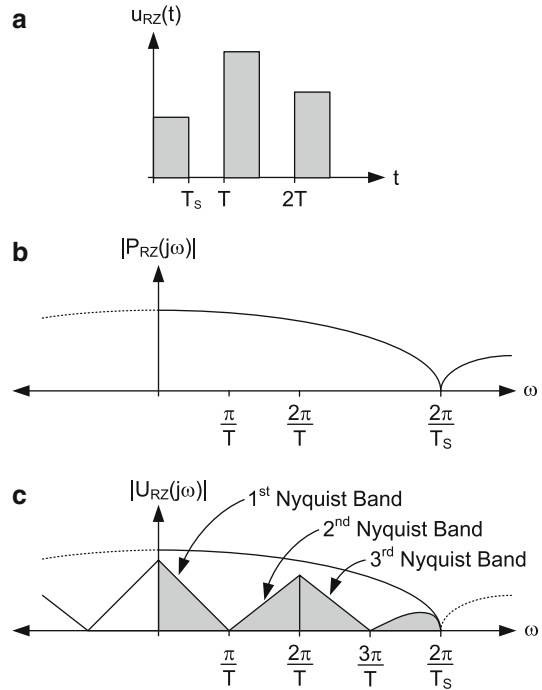
### 1.3.2 The Return-to-Zero DAC

If the unit impulse response is made shorter than the sampling period  $T$ , we speak of a return-to-zero (RZ) DAC. As shown in Fig. 1.12a, the output of the DAC is only active for  $T_S < T$  and reset to zero for the rest of the sampling period. We call the fraction  $D = T_S/T$  with  $D \in ]0..1[$  the duty-factor of the RZ-DAC. The unit impulse response and the corresponding Fourier transform (shown in Fig. 1.12b) are given by

$$p_{\text{RZ}}(t) = \text{rect}\left(\frac{t - \frac{T_S}{2}}{T_S}\right) \quad \longleftrightarrow \quad P_{\text{RZ}}(j\omega) = T_S \cdot \frac{\sin \frac{\omega T_S}{2}}{\frac{\omega T_S}{2}} \cdot e^{-j\frac{\omega T_S}{2}}. \quad (1.9)$$

The first zero in the frequency response is now shifted out to  $1/T_S = 1/D \cdot f_{\text{CLK}}$ , such that the relative amplitude error introduced by an RZ-DAC is smaller, as long as the reset period, or gap,  $(T - T_S)$  consumes a significant fraction of the clock period  $T$  (Fig. 1.12c).

**Fig. 1.12** Spectrum of ideal RZ-DAC: (a) ideal time-domain output waveform, (b) RZ DAC unit pulse spectrum, and (c) RZ DAC output spectrum



As discussed in Sect. 4.2.6, the primary motivation to use RZ is to improve the dynamic performance of D/A-converters. A major drawback is, however, that at the same time, the signal power residing in the baseband that can be delivered to the load is also reduced by the factor  $(T_s/T)^2 = D^2$ . In an oversampled converter employing an active transimpedance stage, the resulting high slew-rate at the output of an RZ-DAC may be problematic (see Sect. 1.4.3). In addition, the increased jitter sensitivity of the RZ-DAC, especially for low signal frequencies, requires in general a much higher-quality clock as compared to NRZ-implementations (see Sect. 2.3.3).

The frequency band from DC to  $\frac{1}{2}f_{CLK}$  is sometimes called the first Nyquist band. Here, we find the reconstructed signal  $d(t)$  that has been filtered with the unit impulse response of the DAC. Likewise, the frequency band from  $\frac{1}{2} \cdot f_{CLK}$  to  $f_{CLK}$  is called the second Nyquist band, from  $f_{CLK}$  to  $\frac{3}{2} \cdot f_{CLK}$  the third Nyquist band, and so forth. The majority of D/A-converter designs is intended for signal synthesis in the first Nyquist band, while the signal components residing in the higher Nyquist bands are eliminated by an analog filter.

An example of a D/A-converter intended for operation in higher Nyquist bands is described in [32]. The implemented half-clock RZ moves the first zero of the unit impulse response to  $2f_{CLK}$ , and the extraction of the second or even the third Nyquist band by an analog bandpass filter is proposed. Although this method potentially allows the translation of the baseband signal to very high frequencies without the use of an analog mixer, it requires a precise and sufficiently linear analog bandpass filter.

Moreover, with signal content near DC the filter order must be correspondingly high to suppress the adjacent image. Note, also, that the signal spectrum in the even Nyquist bands is mirrored with respect to the baseband spectrum. This must be taken into account when generating the digital input sequence for the DAC, in case an even-order Nyquist band is intended for signal transmission.<sup>6</sup>

## 1.4 The Current-Steering DAC

Current-mode D/A-converters represent the digital input code by summing together the corresponding number of unit currents. Because the major part of analog signal processing still takes place in the voltage domain, the output current of the DAC is in most cases converted into an output voltage. The output stage, i.e., the circuit that provides the I-V conversion, must be viewed as an integral part of the D/A-converter because its properties also do influence the behavior of the current sources. In the simplest case, the output stage is a pair of resistors connected to a supply rail.

### 1.4.1 General Description

At a very basic level, a current-steering DAC consists of an array of current sources. A pair of current switches is connected to each current source to steer the current to either the positive or negative output node. The current switches are controlled by the digital input code—depending on the array coding—via a suitable decoder (see Sect. 1.5.1).

In single-ended implementations (see Fig. 1.13a), one switch connects the current source to the output, while the second switch, when switched on, diverts the current to a low-impedance node (e.g. a supply rail), without putting it to further use.

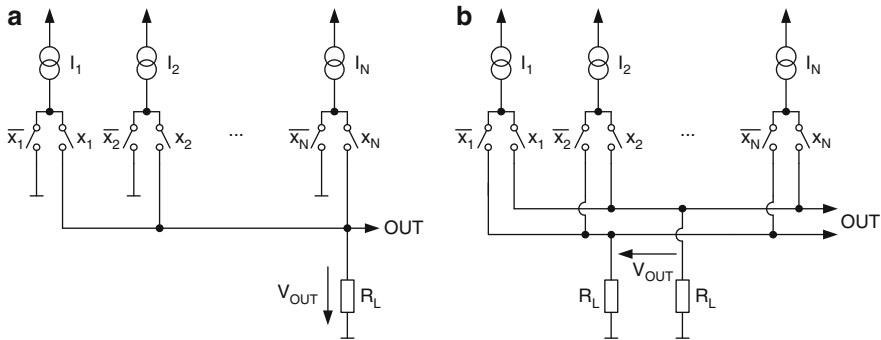
Most modern implementations, especially for transceiver applications, are differential designs that use both complementary output nodes (see Fig. 1.13b). One reason is, that the analog circuits, to which the D/A-converter in a digital transceiver must interface, are usually differential as well. A single-ended DAC-output would then require a single-ended to differential conversion, which is never trivial in high-performance applications. More importantly, differential implementations double the available signal swing, while at the same time the resulting structural symmetry improves other properties, like immunity to certain common-mode disturbances.

Current sources are built with active circuit elements, i.e., MOS or bipolar transistors operated in the active region. MOS-implementations are generally preferred in transceiver applications because they can be integrated in the most basic digital CMOS process together with a large DSP. However, modern digital

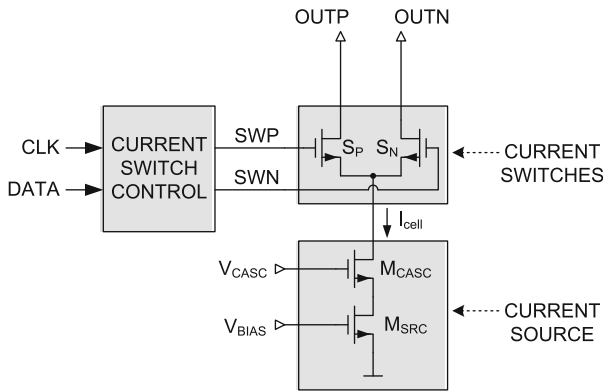
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<sup>6</sup>Alternatively, the flipped spectrum must be handled correctly in the receiver DSP.





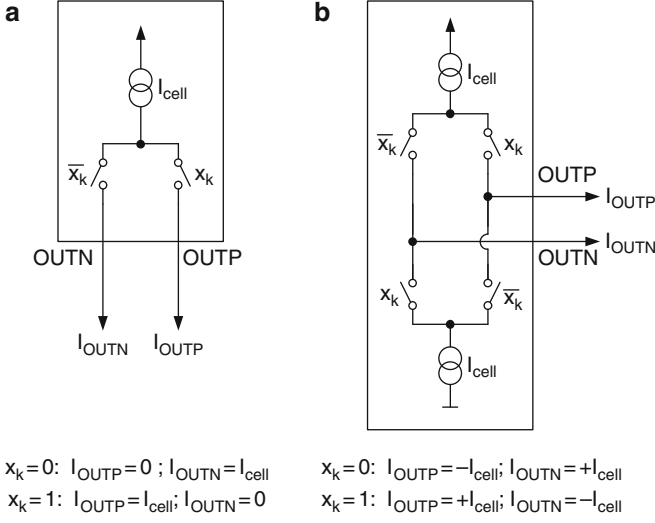
**Fig. 1.13** Single-ended (a) and differential current-steering (b) DAC



**Fig. 1.14** Principle of MOS-based current cell

transceivers are usually fabricated in “analog” CMOS technologies, featuring also high-quality passive circuit elements like linear resistors and capacitors. Such processes offer a much broader range of possibilities to integrate together digital signal processing, data converters and linear analog signal processing circuits.

Figure 1.14 shows the principle of a (single-polarity) current-cell in MOS technology. It consists basically of three parts. The current source ( $M_{SRC}$ ,  $M_{CASC}$ ) generates the cell current  $I_{cell}$ , which is then steered to either OUTP or OUTN with the current switches  $S_P$  and  $S_N$ , depending on the input data (DATA). Because a D/A-converter contains many current cells, the input data must be locally resynchronized with a high-quality clock (CLK), to ensure that all current cells switch at exactly the same time. Also, the switching signals SWP and SWN have to be properly aligned to minimize the dynamic voltage change at the drain node of the cascode transistor  $M_{CASC}$  during switching. These tasks are accomplished by the current switch control.



**Fig. 1.15** Single-polarity (a) and dual-polarity (b) current cell

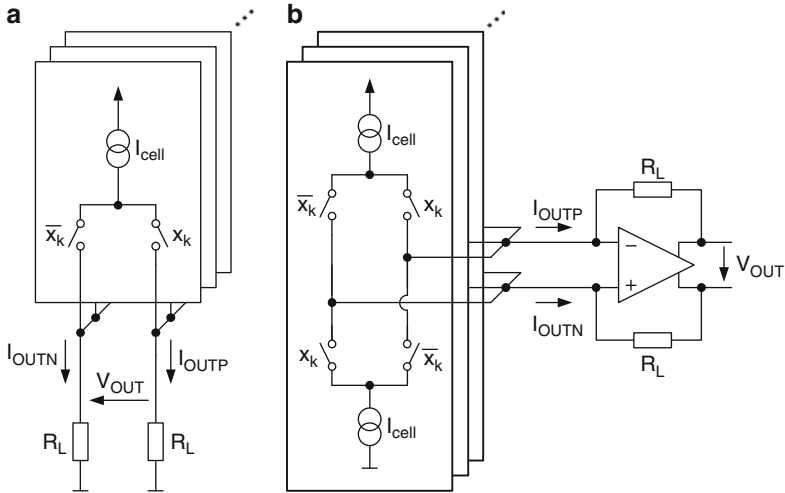
### 1.4.2 Single-Polarity and Dual-Polarity Current Cells

A single-polarity current cell contains a single current source  $I_{\text{cell}}$  and can therefore only source (or sink) its current at one of the two output branches, while the other output is left open-circuited. As shown in Fig. 1.15a, when the right switch is closed ( $x_k = \text{high}$ ) the current  $I_{\text{cell}}$  flows out of  $\text{OUTP}$ , while  $\text{OUTN}$  is disconnected. With  $x_k = \text{low}$ , the left switch connects the current source with  $\text{OUTN}$ . The impedance seen at the output branches thus depends on the value of the switching bit  $x_k$ . Because single-polarity current-steering DACs are usually working into a low impedance load, this fundamental asymmetry is not problematic.

A dual-polarity current cell (Fig. 1.15b) can source *and* sink current. The two complementary current sources in the upper and lower half nominally carry the same current  $I_{\text{cell}}$ . When  $x_k = \text{high}$ , the upper current source is connected to  $\text{OUTP}$  and the lower current source to  $\text{OUTN}$ , the differential output current  $I_{\text{OUTP}} - I_{\text{OUTN}}$  being  $2 \cdot I_{\text{cell}}$ . With  $x_k = \text{low}$  the connections are reversed and the currents in both output branches change polarity. The differential output current is now  $-2 \cdot I_{\text{cell}}$ . Provided that both current sources have identical properties, the impedance seen at both output branches is equal and independent of the switching bit  $x_k$ . This symmetry is important to guarantee code independent settling when an active output stage is used.

### 1.4.3 Passive and Active Output Stage

Single-polarity and dual-polarity current-cell arrays also require a different type of output stage that converts the signal current into a voltage. Assuming a differential



**Fig. 1.16** Current-mode DAC output stages

output, the simplest I-V conversion is provided by a pair of resistors connected to one of the supply rails; see Fig. 1.16a. This output stage is preferred in conjunction with a single-polarity current-cell array. If  $I_{FS}$  is the maximum output current, the so-called full-scale current, then the available voltage range at each of the single-ended outputs is  $[0; R_L I_{FS}]$ , while the differential output voltage range is  $[-R_L I_{FS}; +R_L I_{FS}]$ . The common-mode voltage of the differential output is at  $\frac{1}{2} \cdot R_L I_{FS}$ , which is quite close to one of the supply rails.

The maximum output voltage of a single-polarity current-steering DAC with resistive loading is limited by the compliance voltage range of the current cell that still allows it to achieve a high accuracy. As a rule of thumb, in a single-supply environment with core supply voltage  $V_{DD}$ , the maximum single-ended output voltage for high-linearity applications is typically limited to one quarter of  $V_{DD}$ . The maximum differential FSR is thus 50 % of the supply voltage. Op-amp-based analog circuits on the other hand typically use a differential voltage range of 100–120 % of  $V_{DD}$ , with a common-mode voltage about halfway between the supply rails. Therefore, if the D/A-converter of Fig. 1.16a interfaces to an active analog circuit, e.g., a reconstruction filter, then this block must provide a voltage gain of typically 6 dB. Unless a high input impedance buffer circuit is used, a common-mode current  $I_{CM}$  will flow into the load resistors  $R_L$ . This common-mode current offsets the single-ended output voltage by  $R_L I_{CM}$  and further decreases the linear differential voltage range by  $4 \cdot R_L I_{CM}$ . Additionally, the input impedance of the following stage also appears in parallel to the load resistors  $R_L$ . As an advantage, the single-polarity current-cell array together with a passive output stage is an open-loop structure, and therefore allows the highest conversion speed and signal bandwidth.

Dual-polarity current-steering D/A-converters usually employ an active output stage, as shown in Fig. 1.16b. The I-V conversion is performed in the feedback

branch of the operational amplifier by the resistors  $R_L$ . If  $I_{FS}$  is the maximum output current of each half of the current-cell array, then the full-scale differential output voltage range is  $[-2R_L I_{FS}; +2R_L I_{FS}]$ , with the common-mode voltage set by the operational amplifier. The output nodes of the current-cell array are also maintained at the same common-mode level and the voltage swing at these nodes is very small due to the large gain of the amplifier. The active output stage thus decouples the current-cells from the output nodes and the full-scale voltage can be optimized. Typically, the output voltage range of the DAC can be made equal to the voltage range of the other op-amp-based building blocks connected to the converter. Thus, no further amplification is required, and no loading effects occur, since the output voltage is buffered by the operational amplifier. However, the dual-polarity current-steering DAC with active output stage is a closed-loop system and therefore not suited for very-high-bandwidth applications.

In summary, the choice of the current cell structure and associated output stage for the transmit-DAC of a digital transceiver heavily depends on overall system considerations.

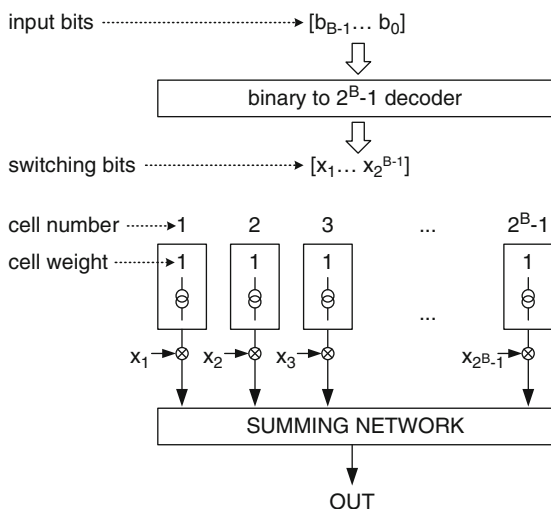
## 1.5 Array Coding

As already mentioned, a D/A-converter relies on the ability of accurately summing together an appropriate number of unit quantities and providing the result at its output port. In every sampling period the number of unit quantities to be summed is given by the digital input word. We call the way in which the possible digital input codes are represented internally by arrays of circuit elements and their respective weights relative to the full-scale value array coding. The following three array types are commonly encountered in D/A-conversion:

- Unary array
- Binary array
- Segmented array

### 1.5.1 Unary Array

A B-bit unary array consists of  $2^B - 1$  identical unit elements, each having LSB-size, as shown in Fig. 1.17. To represent a binary digital code, the unary array requires a digital decoder that maps the binary input data to an equivalent number of DAC-elements. Because the unit elements are not distinguishable, this mapping function is not unique. This means that a specific input code can be represented by more than one set of DAC-elements. Only the full-scale values, i.e., all zeros or ones, have a unique representation, all other codes do have at least  $2^B - 1$  different combinations of unit elements that generate nominally the same output value. Dynamic element matching (DEM) techniques (see Sect. 3.2) try to average out the unit element mismatch over time and make extensive use of this property of unary arrays.

**Fig. 1.17** Unary array

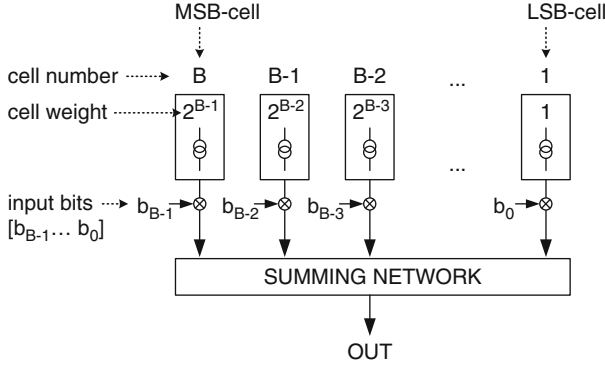
The drawback of unary arrays is that the complexity of the digital decoder is exponentially related to the resolution. In practical implementations the resolution of a unary array is therefore limited to typically 4–8 bits.

On the other hand, unary arrays offer the best possible performance. Because of their strictly incremental nature, monotonicity is always guaranteed. As shown in Sect. 2.1.2, the differential nonlinearity (DNL) of unary arrays is unequaled, because for every code transition it depends only on the accuracy of one single DAC-element of LSB-size. The same is true for a limited class of dynamic effects. When switching from one code to the next, certain transitional errors are linearly related to the code step. If the DAC-elements and the associated switching errors are additionally well matched, then, supposedly, only linear errors can occur in the output signal [33]. However, it will be shown in Sect. 4.1, that even perfectly matched unary current-steering arrays are subject to certain switching imperfections that cause nonlinear distortion.

Unary arrays are also the architecture of choice for multibit current-steering  $\Sigma\Delta$ -DACs. Two design examples using a 6-bit unary array consisting of 64 current sources are described in Chap. 5.

### 1.5.2 Binary Array

In a binary array the elements are binary weighted and thus directly correspond to the respective weight of the bits of a binary digital input code. The LSB-element has unit weight, while the MSB-element has a weight of  $2^{B-1}$ . Because of the direct correspondence between input bits and single DAC-elements, digital decoding is not necessary—the input bits can directly control the respective DAC-cells. For a binary array the mapping function is always unique: each input code is represented by exactly one combination of DAC-elements (Fig. 1.18).



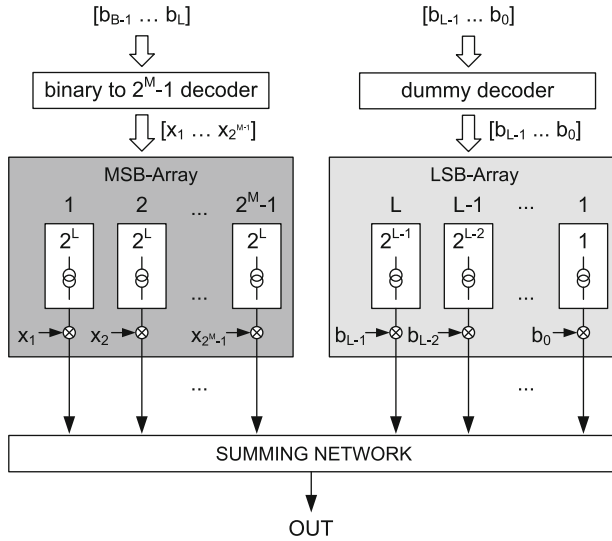
**Fig. 1.18** Binary array

Binary arrays have the simplest possible implementation and minimum overhead for digital logic. In terms of performance, however, they are inferior to unary arrays. Monotonicity is not guaranteed, and the DNL of binary arrays is generally worse, because major carry transitions rely on addition *and* subtraction. For the same reason, dynamic errors related to the switching of the DAC-elements, commonly called glitches, are also much more pronounced. For these reasons, binary arrays are believed to be limited to the lower resolution range. As a counter-example, a 250 MS/s 10-bit binary-coded current-steering DAC having a SFDR > 60 dB within the first Nyquist band is described in [34].

### 1.5.3 Segmented Array

Segmented arrays consist of different sub-arrays, or segments, each with a potentially different array coding. Figure 1.19 shows an example of a segmented converter with two sub-arrays. The MSB-segment is a unary array with  $2^M - 1$  elements and represents the upper  $M$  bits. The LSB-segment realizes the lower  $L$  bits in a binary array. The overall resolution of the converter is  $B = M + L$ . The MSB-elements all have an equal weight of  $2^L$  and are controlled by a binary to  $2^M - 1$  decoder. The LSB-elements on the other hand can be directly controlled by the lower  $L$  bits of the digital input code. In order to equalize the delay of the MSB-decoder, usually a dummy decoder is inserted to align the timing for the LSB-segment [35].

Segmented arrays offer an attractive compromise between the superior static and dynamic performance, but increased complexity of unary arrays and the simplicity, but inferior performance of binary arrays. Therefore, in a segmented architecture the MSB-segment is virtually always a unary array, while the LSB-segment is typically a binary array. The higher the amount of segmentation, i.e., the resolution of the unary MSB-array relative to the overall converter resolution, the better the dynamic

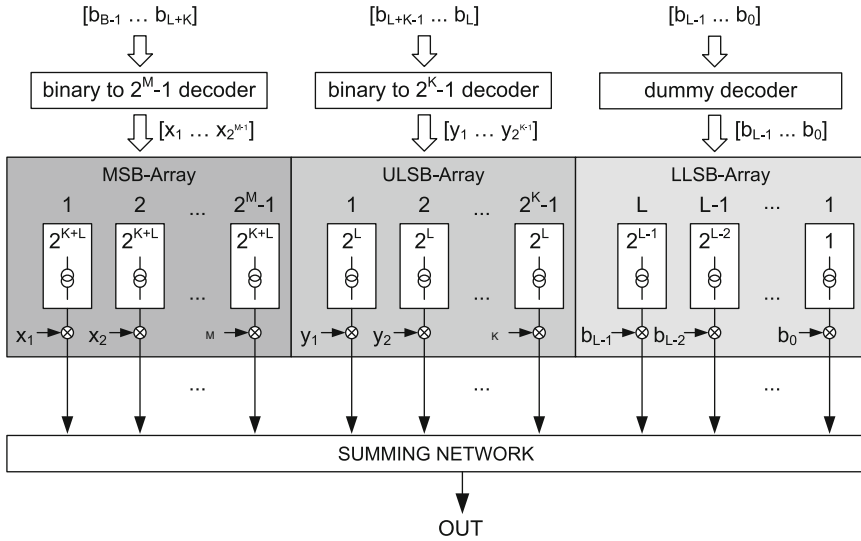


**Fig. 1.19** Segmented D/A-converter with two segments

performance will be. On the other hand, the complexity and silicon area needed for the binary to thermometer decoder is exponentially related to the resolution of the MSB-segment.

In [33] the optimum amount of segmentation for current-steering DACs is empirically stated to be at the point where the analog area (current sources) and the digital area (decoder) are equal. Along this line of reasoning, with the continuing migration to finer geometry technologies the optimum amount of segmentation should be shifting towards fully unary arrays, because analog and digital circuits do not scale equally. At least in uncalibrated D/A-converters the analog area will be dominated by the current source transistors, and these are subject to accuracy and noise requirements. Although the matching generally improves with smaller minimum channel length, various process related effects tend to counteract this trend in deep-submicron technologies [36–38]. Moreover, the continuous reduction of the supply voltage decreases the gate overdrive voltage that can be applied to the current source transistors. This generally worsens the drain current matching for a given transistor area [39]. Because the output voltage swing is also reduced along with the supply voltage, the full-scale current must be increased accordingly, in order to maintain a constant SNR. In a given technology with already maximized gate overdrive this can only be achieved by increasing the transistors' aspect ratio. All these effects taken together do not allow the analog portion of the converter to follow the aggressive “digital” scaling rules.

However, in present technologies segmentation is still generally used for converters having a resolution above 8 bits. The unary MSB-segment in these designs typically realizes 4–8 bits. For still higher resolutions, typically starting



**Fig. 1.20** Segmented D/A-converter with three segments

around 12 bits, an additional low-resolution (2–3 bits) intermediate segment is inserted between the MSB-array and the LSB-array [40–42]. Although the performance is slightly compromised by splitting the current-cell array into more segments, the total area required for the digital circuitry is greatly reduced. In Fig. 1.20 a segmented converter with three sub-arrays is shown. The MSB-segment again represents  $M$  bits in a unary array with  $2^M - 1$  equal elements and thus requires a binary to  $2^M - 1$  decoder. The middle segment, sometimes called the upper-LSB array (ULSB), codes the next  $K$  bits, also in a unary array with  $2^K - 1$  elements. Since  $K$  is usually small, the ULSB-decoder will not add significantly to the overall digital complexity. Finally, the lower-LSB array (LLSB) represents the remaining  $L$  bits in a binary array. The overall resolution of the converter is thus  $B = M + K + L$ . The MSB-elements and ULSB-elements each have a weight of  $2^{K+L}$  and  $2^L$ , respectively.

Two examples of segmented current-steering D/A-converters are described in Chap. 6. Both designs realize a 13-bit converter using three segments:

- MSB-segment: 6-bit unary array
- ULSB-segment: 2-bit unary array
- LLSB-segment: 5-bit binary array

This choice of the segmentation mainly depends on practical considerations. A 6-bit MSB-segment is a compromise between a moderate amount of decoding logic, but considerably improved dynamic performance. The 2-bit thermometer-coded intermediate segment provides a somewhat smoother transition to the binary-coded 5-bit LLSB-array, while the required decoder complexity for the ULSB-segment remains practically negligible.





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