

# Preface

D/A-converters synthesize analog signals at the very heart of digital transceivers, thus linking the world of digital signal processing to the analog signal domain. The integration of the digital signal processor (DSP) together with data converters and analog signal processing functions in advanced CMOS technologies finally enables the realization of complete transceivers on a single silicon chip. This so-called system-on-chip (SoC) integration drastically reduces the cost and the form factor of the overall system, a highly desirable situation in cost-driven hardware development.

The topic of this work is the modeling and the implementation of high-performance current-steering D/A-converters for digital transceivers in nanometer CMOS technology. To comply with the target of SoC integration, the designed converter modules are fully embeddable in a mixed-signal system. They use only core devices, operate from a single supply voltage, and are optimized for small silicon area and low-power dissipation.

In the first part of this book the fundamental performance limitations of current-steering DACs are investigated. Based on simplified models, closed-form expressions for a number of basic nonideal effects are derived and tested. A special focus is put on the signal-dependent noise performance in multitone systems, showing that the traditional full-scale single-tone criteria are not adequate and may lead to substantial overdesign of biasing and/or clocking circuits. The knowledge of the basic performance limits allows to optimize the converter and system architecture already in an early design phase, essentially trading off circuit complexity, silicon area, and power dissipation for static and dynamic performance.

The second part of this book describes the design and experimental verification of four different current-steering DAC testchips, implemented in standard 130 nm CMOS. The converters use a single 1.5 V supply and have a resolution in the range of 12–14 bits for an analog bandwidth between 2.2 MHz and 50 MHz. Sampling rates between 100 MHz and 350 MHz are used. Dynamic element matching (DEM) and advanced dynamic current calibration techniques are employed to minimize the required silicon area. High-resolution converters with an active output stage to maximize the analog output signal swing, traditionally only used for low-frequency

applications, are demonstrated to reach signal bandwidths of 30–50 MHz, while maintaining a dynamic linearity larger than 70 dB over the whole bandwidth.

This book is organized into seven chapters:

- Chapter 1 provides an overview of D/A-converter fundamentals, especially focusing on the current-steering architecture and segmentation strategies.
- In Chap. 2 the generally accepted performance figures used to characterize D/A-converters are reviewed. The impact of correlated bias noise and sampling jitter on the noise performance of a current-steering DAC is analyzed, and, based on simplified models, exact descriptions of the noise spectra for single-tone and multitone signals are derived. The jitter noise expressions obtained for multitone signals in an NRZ-DAC are also verified experimentally.
- In Chap. 3 the static linearity limited by random mismatch of the current sources is explored. Based on a statistical description of the fabrication yield, expressions for the required minimum current-source area fulfilling a given yield specification are derived. The code-dependent output resistance of the current-source array is identified as a further limiting factor for the static linearity. Expressions for the INL of the single-ended and the fully differential converter as a function of the finite output resistance of the unit current cell are given. The second part of Chap. 3 gives a general overview of two known methods to improve the static linearity: DEM and current calibration.
- Chapter 4 analyzes the three basic effects that limit the dynamic linearity of a current-steering D/A-converter. Under the idealizing assumption of perfectly matched current cells, which are also not influenced by any other large-scale imperfections, it is possible to derive closed-form expressions for the nonlinear distortion of a synthesized sine wave. The first effect is given by switching asymmetries that result in unsymmetrical current pulses. These are shown to generate even-order harmonic distortion in fully differential converters. The second effect is caused by the finite feed-through of the output voltage to the parasitic capacitance connected at the common tail node of the current switch pair. The resulting code-dependent error charge packets injected into the output generate odd-order harmonic distortion. The third effect that limits the dynamic linearity of a current-steering D/A-converter is the frequency-dependent distortion due to the code-dependent output impedance of the current-source array. It is shown that in a fully differential converter with standard current-cell architecture this effect is at least within the boundaries of practical sampling frequencies, not likely to become dominant compared to the switching errors. Nevertheless, it is a fundamental limitation to the achievable dynamic linearity, since it cannot be compensated straightforwardly, e.g., by applying a special switching algorithm. The second part of Chap. 4 describes various known circuit techniques to improve the dynamic linearity of current-steering D/A-converters.
- Chapter 5 describes the implementation of two  $\Sigma\Delta$  D/A-converter testchips targeted at wireline communication applications. The first design is a 14-bit DAC targeted at the ADSL2+ downstream bandwidth of 2.2 MHz. It uses a second-order noiseshaper together with a very simple barrel-shift algorithm and

is optimized for low-power dissipation. The second design is a multi-mode  $\Sigma\Delta$ -converter for ADSL and VDSL. An interleaved current-cell architecture implements an effective return-to-zero (RZ) for the single current cell and also allows to use a modified data weighted averaging (DWA) algorithm. With a sampling rate of 350 MHz and an oversampling ratio of only 6, a dynamic range of 12 bits in a bandwidth very close to 30 MHz is demonstrated. Due to the effective RZ, the dynamic linearity around 30 MHz remains above 75 dB. The converter module is readily scalable—by register programming—to lower signal bandwidths, with not only drastically reduced power consumption but also increased resolution.

- In Chap. 6 two Nyquist-rate D/A-converter testchips using dynamic current calibration in the background are described. Both designs implement a segmented 13-bit converter core. The first module is a classical, resistively terminated single-polarity DAC, while the second converter uses a dual-polarity core with active transimpedance output stage to maximize the available voltage swing. In conjunction with an interleaved current-cell architecture this DAC achieves a signal bandwidth of 50 MHz with a dynamic linearity exceeding 70 dB over the full signal bandwidth. The periodicity of the background calibration, normally a source of low-frequency tonal disturbances, is destroyed by the introduction of a randomized calibration slot length. Thereby the calibration refresh tones are spectrally shaped and merged with the noise floor. This randomization also helps to suppress the image tone due to dynamic calibration effects in an interleaved architecture. Two novel strategies to trim the elements in converter segments with different weights are employed. The first design tries to match the segment boundaries by appropriately summing together uncalibrated and previously calibrated DAC elements for comparison with a unique reference element. The second design performs direct calibration of single DAC elements in differently weighted segments. In order to generate the required scaled reference currents with an accurate ratio, a reference cell array is introduced, which calibrates its constituting elements in a separate calibration loop, also running fully in the background.
- Finally, Chap. 7 summarizes the main results of this work, while trying to draw general conclusions. Also, it provides an outlook on future developments that are expected to happen in the area of CMOS current-steering D/A-converters targeted at digital communication systems.



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