

Towards Post-CMOS Molecular Logic Devices

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Abstract The use of molecular devices in post-CMOS devices and structures is described. Particularly we demonstrate the fabrication and characterization of two-novel devices: a two-terminal device which exhibits a two-negative differential resistance peaks and a sub-10-nm-channel vertical molecular transistor which contains a molecular quantum-dot compound. We show that the latter device can be operated in two distinct modes: gate-controlled switch and gate-controlled hysteresis.

1 Introduction

The field of molecular electronics emerged in the past couple of decades and is drawing attention largely in light of the increasing limitations of solid-state microelectronics. Moore's law, the highly cited guideline first mentioned in 1965, predicts a doubling every 18–24 months of the number of transistors on an integrated circuit [1]. With the silicon metal-oxide-semiconductor (MOS) transistor, and later on complementary MOS (CMOS) architecture, this trend has been upheld by industry for the past five decades. Indeed, a decade ago, process technology was at the $0.18\text{ }\mu\text{m}$ (180 nm) node (referring to the channel length of a MOS transistor), while today, the 22-nm node is becoming the industry standard [2].

However, performance limitations are expected to increase with the scaling of devices. Leakage currents can occur by carriers tunneling through ever-thinner gate dielectrics or as subthreshold current between ever-closer source/drain regions, when the transistor is operating in the weak-inversion region. The increase in device density due to scaling also leads to an increase in generated heat and in the need

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to dissipate it. A variety of secondary effects, collectively termed short-channel effects, also play an increasing role in degraded transistor performance [3, 4]. One such example is drain-induced barrier lowering (DIBL). This effect describes a decrease in the potential barrier between the source and channel regions, due to the closer proximity of the drain region. The applied bias on the drain would therefore influence the magnitude of the drain current, which ideally is determined only by the gate voltage. This results in a lowering of the threshold voltage of the MOS transistor and higher subthreshold currents. Another secondary effect is surface scattering. As a result of narrower channel, and together with the lateral extension of the source/drain depletion regions into the channel region, the longitudinal component of the electrical field applied from the gate increases. As a result, carrier mobility is reduced in the lateral direction, as they tend to accelerate towards the gate. These stronger electric fields also increase the probability for electron carriers to tunnel into the gate dielectric. Once there they are trapped and build up charge in the dielectric. Threshold voltage must be increased to compensate for these charges, thereby degrading device performance. This is termed the hot electron effect. Indeed, increased subthreshold conduction and power consumption and the need for effective heat dissipation are some of the most relevant issues currently addressed by the semiconductor industry [5–7].

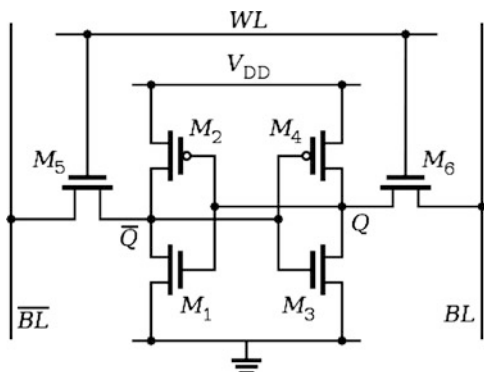
The negative effects of leakage currents are of particular importance for static random access memory (SRAM). An SRAM cell is typically composed of six MOS transistors, and the data bit is stored on four of the transistors, as two cross coupled inverters, as shown in the following figure (Fig. 1).

A key parameter in the design of SRAM circuits is the data retention voltage (DRV) which defines the minimum supply voltage to the circuit at which a data bit can be retained. Typical SRAM operation often requires reducing supply voltage to below the threshold voltage of the transistors, where conduction is primarily by leakage currents. Thus, as subthreshold conduction increases with device scaling, the power consumption of SRAM circuits becomes even more pronounced.

Several process innovations such as the transition to high- κ dielectrics, strained silicon channels, ultra-shallow junctions, and others have been implemented to combat these device performance issues [4]. Developments such as deep UV and immersion photolithography have further pushed the resolution limit for feature patterning [4, 8]. However, these too are nearing a physical limitation. The inevitable consequence of these innovations is an increased burden on R&D and production cost, and diminishing returns with every new technology node [5]. This trend has been termed ironically as Moore's second law. Lastly, with every new technology node, the positive effects of scaling on processing power, speed, and complexity are less pronounced, with other factors such as interconnect and memory access delays being the main limitations on performance [8]. As such, the 2010 update of the International Technology Roadmap for Semiconductors (ITRS) predicts a decline in development, with transistor count doubling only every 3 years starting 2013 [2].

Molecular electronics offers both an alternative and a complement to existing semiconductor technologies [9]. In the ideal scenario, the field addresses electronic devices comprising circuits in which specific molecules, as opposed to transistors or

Fig. 1 Typical setup of SRAM



traditional thin films, are the basic building blocks. Besides the obvious advantage of their small dimensions, individual molecules are identical and are therefore expected to behave robustly as electronic devices, with no variance. The great variety of molecules and the ability to synthesize them as needed leads to a great variety in electrical, mechanical, and optical properties when considered as practical devices. A key difference from conventional semiconductor technology is in the fabrication, which takes on a bottom-up, as opposed to a top-down approach. Whereas in industry, the bulk material is processed down to produce scaled devices, in a bottom-up approach, the molecules are first synthesized and then assembled into structures and circuits of increasing complexity [9–11]. This requires a different approach and design for the fabrication process of molecular circuits. While at heart it is a completely different approach to electronics, it is expected that molecular electronics, at least in the coming years and decades, will see increasing integration, as opposed to competition, with conventional electronics, namely, silicon-based CMOS technology [9, 11]. Recent advances in molecular devices, both two-terminal (such as molecular memristors [12]) and three-terminal devices (molecular transistors [13]), offer appealing alternatives to the current logic and memory technologies. In the following section these advances will be described.

1.1 Two-Terminal Molecular Junctions: Focusing on Negative Differential Resistance

A variety of materials can be exploited on the molecular and nanoscale levels to produce unique electrical properties that can be then used to construct novel electronic devices, with similar functionalities as CMOS devices. One example is phase-change materials (PCM). A common choice of such materials is chalcogenides family [14]. These have the ability to toggle between the amorphous and crystalline phases when heated, for example, by applying an electrical current. The two phases possess different electrical resistivity. Thus, when a given voltage

is applied across a PCM device, the resultant current will either be high or low, depending on the phase of the material. This applied voltage can be considered as a read voltage on a nonvolatile memory (NVM) cell. A program voltage will set the cell to a low-resistance “1” state. This voltage is determined by Joule heating, to a temperature above the crystallization point of the PCM material, but below its melting point. Once cooled, the cell is in the crystalline phase, the low-resistance “1” state. To erase the cell, a higher voltage is required to bring the cell above its melting point, to the amorphous phase, where the high resistance represents the “0” state. As such, NVM devices based on PCM materials are currently in development and production among the leading companies and slated to replace existing floating gate flash memory [15].

A positive effect of scaling such devices, besides increased memory density, is faster program and erase speeds. A PCM-based memory cell’s speed is limited by the cooling time of the material following Joule heating. This cooling time is reduced along with device dimensions. However, there are several hurdles in full adoption of PCM-based memory [15].

Negative differential resistance (NDR) is another property found in some molecular systems and novel materials [16, 17]. It describes a decrease in current in response to an increase in applied bias over a given range, as shown in the following figure (Fig. 2).

An NDR device could cancel out an equal and opposite load resistance when connected in series and theoretically produce infinite power gain [18]. Incorporated into a resonance RLC circuit, an NDR element can produce high-frequency oscillators, operating in the microwave and infrared ranges [19, 20]. Rectifiers are another class of electrical devices that can be constructed using NDR elements [21, 22]. NDR can also be used to induce bistability in a circuit, a condition in which the circuit operates in two stable points. As such, circuits based on NDR elements have the potential to be used as digital logic and memory devices [23–25].

NDR has also been observed in a variety of single-molecular layers, termed monolayers [26]. For example, Chen et al. describe an NDR device in which the active region is a monolayer of 2'-amino-4-ethynylphenyl-4'-ethynylphenyl-5'-nitro-1-benzenethiolate, situated between two Au contacts [27]. An applied positive bias leads to a one-electron reduction from one of the contacts to the molecules. As a result, a radical anion is formed, acting as a charge carrier in the system, increasing the overall current. A higher applied bias leads to an additional one-electron reduction. In this scenario a nonconducting dianion state is reached, drastically reducing the overall current of the system. The group reports a peak current of 1.03 nA. The active layer was situated in circular regions of diameters 30–50 nm. As such, a current density of $\sim 53 \text{ A/cm}^2$ was achieved in the devices. With a valley current of 1 pA, the peak-to-valley ratio (PVR, see Fig. 2) was 1,030, several orders of magnitude greater than possible with semiconductor NDR devices. However, these measurements were conducted at 60 K and significantly diminish approaching room temperature.

Earlier work conducted in our group has also shown NDR in monolayer devices [17]. In this case, a monolayer of a ferrocene-derived compound was used (Fig. 3).

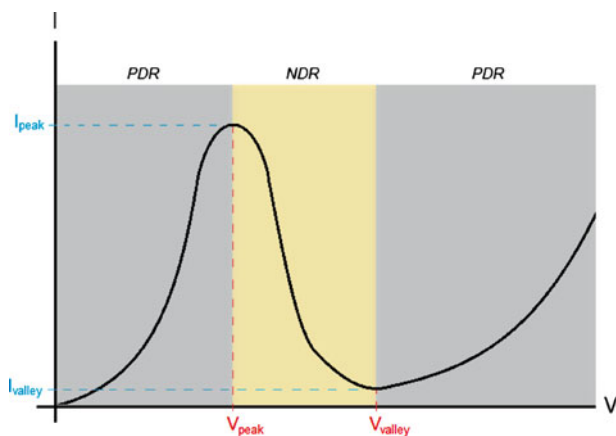


Fig. 2 Current/voltage characteristics of negative differential resistance

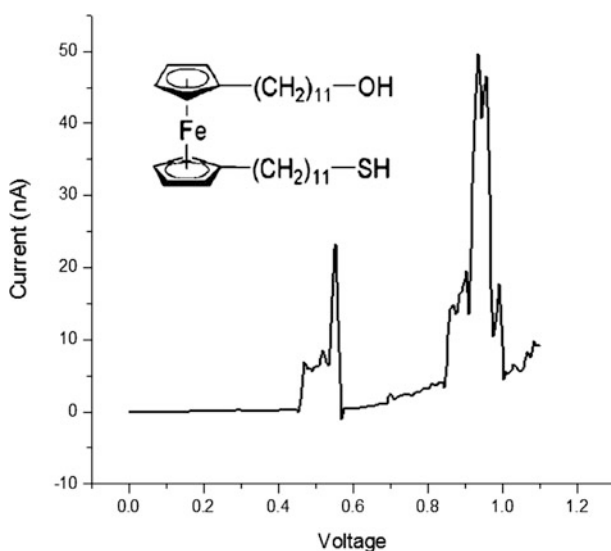


Fig. 3 Ferrocene-derivative molecule used to form a multi-peak NDR device (see [17])

The compound consists of a ferrocene molecule, $\text{Fe}(\text{C}_5\text{H}_5)_2$, synthesized with organic chains on both sides, where one chain is thiolated. The chemical structure of the compound and a typical I/V characteristics are shown in the following figure.

A monolayer of this material was formed over an Au bottom electrode and sandwiched on the opposite end by a Pd top electrode. Electrical measurements of the structure showed two NDR peaks at ~ 0.55 V and ~ 0.92 V. The mechanism responsible for these peaks has been speculated to relate to ferrocene redox reaction centers around the biases at which the peaks occur. Another hypothesis is the

formation of polaronic states which at the molecular junctions allows the formation of NDR [28].

NDR devices have been used in the pre-CMOS days to construct digital circuits. A classic implementation of such a design is the so-called Goto pair, first presented by E. Goto et al. in 1960, with a simple circuit using tunnel diodes [29, 30]. The circuit consists of two NDR devices in series and has since been named the Goto pair. Contemporary research into tunnel-diode logic circuits based on the Goto pair was also conducted by M.S. Axelrod et al. [31]. However, subsequent developments, namely, CMOS technology, have rendered this architecture as obsolete. Nonetheless, in recent years, a growing interest has been observed within academic circles in NDR-based logic and in the Goto pair as an implementation of such circuits [23, 32, 33]. A simple circuit based on the Goto pair is shown in the following schematic (Fig. 4).

The advantageous nature of this circuit for digital applications, as a consequence of the unique IV characteristics of NDR devices, is readily discernable from a load-line perspective. The voltage level of the circuit at the node between the two devices, labeled as n_2 , will be stable at equilibrium points, in which the load and drive currents are equal. This can be seen in the following load-line diagrams, depicting two identical NDR devices.

These equilibrium points are marked as green dots above, at the intersections of the load and drive IV curves on the load-line diagrams. It can be seen that at biases below $\sim 2*V_{\text{peak}}$, with both devices in the PDR region, the circuit essentially behaves as a voltage divider. The corresponding current and voltage at node n_2 are shown at the intersections in Fig. 5a, b. With one stable equilibrium point, the circuit is termed monostable at these biases. Increasing V_{IN} above $\sim 2*V_{\text{peak}}$, the circuit undergoes a monostable–bistable transition (MBT), depicted in Fig. 5c, d. At these higher input biases, three equilibrium points exist for the state of the circuit at node n_2 , in which the drive and load currents are equal. However, at the central point, both devices are in their NDR regions, and the circuit is at a state of unstable equilibrium. Any current fluctuation into node n_2 through the NDR devices will create an imbalance between I_D and I_L , and draw the circuit to one of the two other equilibrium points, where the circuit is at stable equilibrium. At the two stable points, minor current fluctuations will cause a charge imbalance that will dissipate within the circuit, but will not cause a change in the state/voltage at node n_2 . Thus, with the ability to retain one of two voltages, the circuit is suitable for digital applications.

1.2 Three-Terminal Molecular Junctions: Towards Molecular Realization of the Floating-Body (1T) Transistor

For years, floating-body transistors have been touted as an alternative to conventional cache memory. Current capacitor-based cache memory technology is running

Fig. 4 An example of GOTO pair circuit

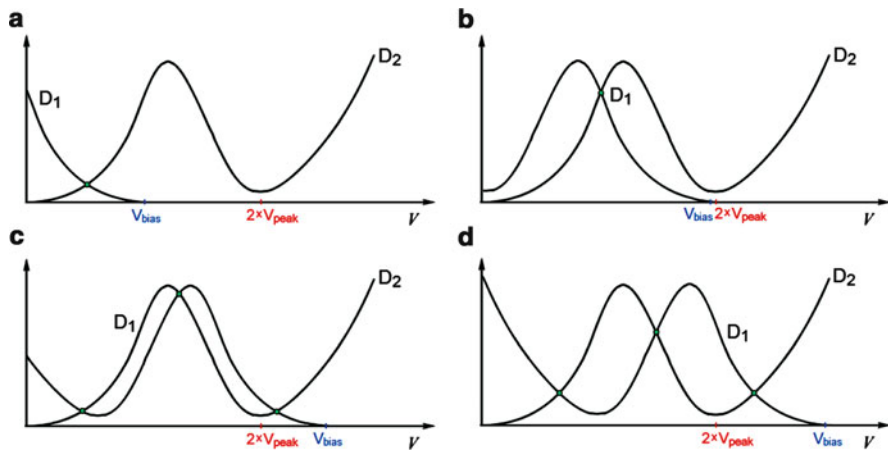
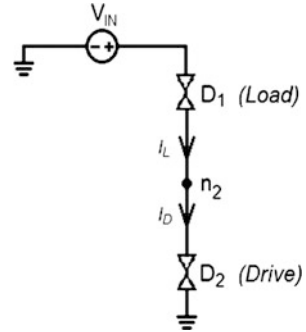


Fig. 5 Load-line diagrams of two NDR devices

out of gas. Since the storage capacitance must be kept constant, for the next generations of conventional 1T-1C DRAM cells beyond the 22-nm technology node, the miniaturization of the bulky storage capacitor will become more and more difficult. In the future, several existing solutions such as trench or stacked capacitors using high- k materials will remain expendable but at the expense of the loss of performances and cost rising.

Several years ago, a new generation of DRAMs using only one transistor, called 1T-DRAM, was proposed as an alternative to the usual 1T-1C DRAM architecture. This memory cell uses the floating body of a single transistor to hold the information, that is, to store the charge. It is also a candidate for increased memory density, compared to the standard six transistor (6T) cache memory that is used on all microprocessors today, as discussed in the introduction. As for 1T-1C DRAM cells, the crucial performance factors to consider are a high retention time, sufficient-sensing margin, low programming bias which enables low power consumption, and further cell scalability.

All the proposed and demonstrated 1T-DRAMs use the majority carriers stored at one interface to modulate the minority carrier current flowing at the opposite interface. This revolutionary principle is based on the coexistence of electrons and holes in the same body which basically requires a two-gate operation or moderately thick films (~ 50 nm). However, ultrathin films (≤ 10 nm) are needed for MOSFET scaling beyond the 45-nm node; this condition also applies to embedded 1T-DRAMs co-integrated with logic circuits. Unfortunately, the super-coupling effect forbids the simultaneous activation of the electron and hole channels, facing each other, in the same ultrathin silicon layer.

Our approach is to explore molecular systems to harvest sub-10-nm molecular transistors and to construct gate-controlled hysteresis device that can be used to form a novel 1T-DRAM. This molecular route is strongly supported by the ITRS vision which states that molecular-based electronics is one of the leading candidates to extend Moore's law [2]. However, this great potential was not realized by now due to the difficulty to fabricate reliable devices in parallel and in mass production. Recently, we and others have demonstrated several routes for the fabrication of molecular transistors which might be integrated in future device technologies. Recently, we reported on the formation of quantum-dot-based room-temperature vertical transistors that can fulfill the demands of future post-CMOS technologies.

Recently, we have demonstrated the fabrication of thousands of vertical molecular transistors on a single chip, all in fabricated in CMOS compatible facilities [13,34–37] (see Fig. 6). Those transistors adopted a *hybrid approach* where CMOS vertical transistors structure was created while specially engineered molecular layers were self-assembled into a predetermined area. Importantly, the molecular layers defined the critical channel width (the molecular size – 1–4 nm) while offering the molecular versatility to determine the transport characteristics of the transistor.

This has been achieved by incorporation of a monolayer composed of a modified C₆₀ molecular quantum-dot (MQD) system [36] or even electroactive protein layers [13,35]. Figure 6 shows the MQT transistor in which it was asymmetrically coupled to the leads of the source and drain device *via* a thin oxide layer on the bottom contact and physical adsorption of Pd on the top contact. This vertical side-gate molecular transistor was operated at low voltages with high gate-voltage sensitivity, thus allowing reproducible and reliable measurements on various types of molecular systems. Moreover, the fabrication methodology allows the formation of multiple arrays of transistors fabricated in parallel with the use of conventional engineering processes and lithographic techniques [13,36].

Figures 7 and 8 show the transistor and hysteresis measurements taken at two different values of VG. It can be seen that two new distinct modes of operations are demonstrated: “voltage-driven switching,” in which the conductance can be modulated by the gate voltage, and a new mode of operation, “voltage-controlled hysteresis,” in which the properties of the loop can be controlled by the gate voltage. While the first method can be exploited for switching applications, the second mode can be used for memory applications.

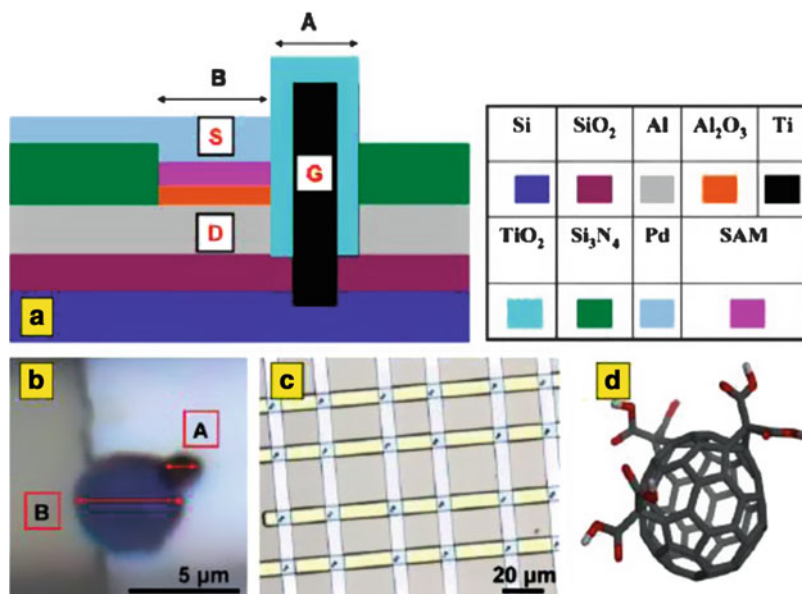
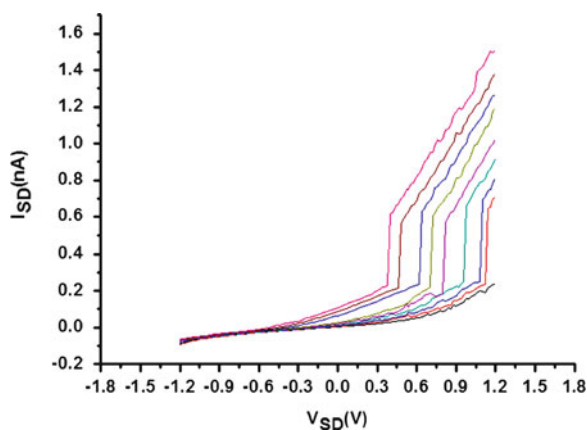


Fig. 6 Schematic representation of the transistor (the dimensions of the layer are unscaled for clarity). A side gate (A) is used to activate molecular layers stacked (B) vertically and separated from the source electrode by an oxide layer. The current is flowing between the source and the drain electrodes (S,D) and modulated by the gate lead (G). (a,b) Optical images of a single device (c) and of an array of transistors (d). The molecular layers are confined

Fig. 7 Gate-controlled switching of MQT transistor (see [36])



Our results can be understood from a consideration of the transistor structure and the polaronic model [28]. We have concluded that a successful operation of an MQD transistor must fulfill some of the following basic experimental conditions:

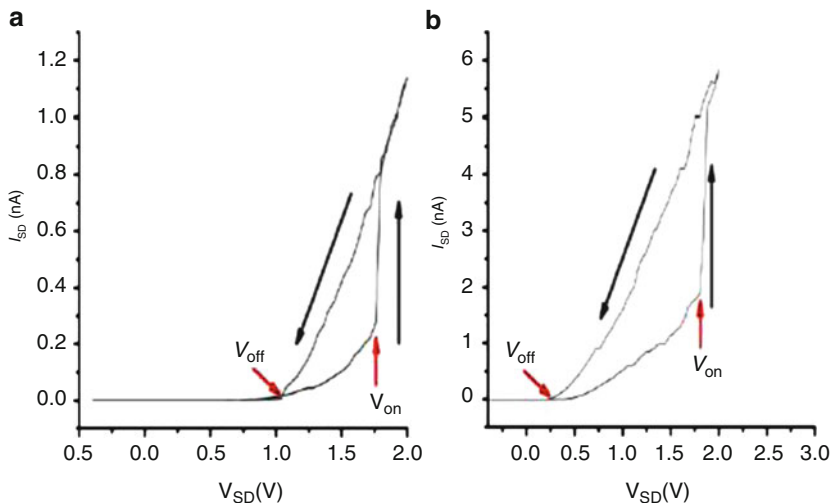


Fig. 8 Gate-controlled hysteresis. I-V curve of a typical molecular quantum-dot transistor exhibiting conductance switching and hysteresis taken at different gate voltages (0.64 V (a) and 1.15 V (b)). Von and Voff are defined at the first discontinuity point and at the crossing point of the reverse and forward scans, respectively

1. The tunneling rates in a polaronic transistor must be considerably slower than the polaronic relaxation time. In practice, this situation can be achieved by lightly coupling at least one of the electrodes to the molecular system. In our case this condition was fulfilled mainly by the introduction of the oxide spacer between the metallic electrode and the SAM.
2. Asymmetric junctions enhance the probability of measuring hysteresis effects. This point was discussed theoretically by D'Amico et al. [38] who noted that although a symmetric situation can also give rise to hysteretic behavior, this would happen only over a finite range of bias voltages, thus decreasing the probability of measuring it. On the basis of our results and on the above analysis, we conclude that asymmetrical junctions are experimentally favorable for molecular-transistor applications.
3. The vertical transistor configuration offers some advantages over the conventional lateral one, since it provides an additional degree of freedom in the choice of materials used for the source and the drain electrodes. While in our case we could easily construct asymmetric junctions by choosing different materials for the leads, in the lateral configuration, this task is very difficult. Furthermore, the vertical configuration allows the fabrication of complex (metal-oxide) contacts as demonstrated in this work.

To summarize, these post-CMOS transistors which operate in low power (below 1V) either in standard CMOS transistor operation mode or in single-electron quantum transistors mode thus offer new type of operation of gate-controlled hysteresis (see Fig. 2), hence offering new mechanism for charge storage.

Furthermore, these transistors offer the use of the inherent quantum effects allowing the operation of **1T-DRAM** in a new fashion utilizing the extraordinary switching and charging properties of a molecular quantum dot transistor [35] which allow the use of novel *advanced logic and memory platforms* that are extremely hard to achieve using current CMOS technology.

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