Preface

In the last years, the world has observed the increasing complexity of integrated circuits (ICs), strongly triggered by the proliferation of consumer electronic devices. The design of complex system on a chip (SoC) is widespread in multimedia and communication applications, where the analog and mixed-signal (AMS) blocks are integrated together with digital circuitry. However, the analog blocks development cycles are larger when compared to the digital counterpart. The two main reasons identified are the lack of effective computer-aided design (CAD) tools for electronic design automation (EDA), and that analog circuits are being integrated using technologies optimized for digital circuits. Given the economic pressure for high-quality yet cheap electronics and challenging time-to-market constraints, there is an urgent need for CAD tools that increase the analog designers' productivity and improve the quality of resulting ICs.

The work presented in this book belongs to the scientific area of electronic design automation and addresses the automatic generation of analog IC layout. An innovative design automation tool based on template descriptions and on evolutionary computation techniques, LAYGEN II, was developed to validate the proposed approach giving special emphasis to the reusability of expert design knowledge and to the efficiency on retargeting operations. The designer specifies the sized circuit-level structure, the required technology, and, also, provides the technology-independent high-level layout guidelines through an abstract layout description, hence forward called template. The generation proceeds in the traditional way, first placement and then routing. For placement, the topological relations present in the template are mapped to a non-slicing B*-tree layout representation, and the tool automatically merges devices and ensures that the design rules are fulfilled. The router optimization kernel consists of a modified version of the multi-objective evolutionary algorithm (MOEA), NSGA-II, and uses a built-in evaluation engine. The automatic layout generation is here demonstrated using the LAYGEN II tool for two selected typical analog circuit structures, namely, a fully dynamic comparator and a single-ended folded cascode amplifier. The layouts were generated for two design processes, United microelectronics corporation (UMC) 130 nm and Austria microsystems (AMS) 350 nm, and the output provided is a GDSII stream format, a file standard for data exchange of IC layout. Automatic generation processes were

performed in less than 5 min, which allow for the designer to quickly obtain a solution. The results were validated using the industrial grade verification tool Calibre® to run design rule check (DRC), layout versus schematic (LVS), and also extraction, in addition post-layout simulations were successfully performed.

This book is organized into seven chapters.

Chapter 1 presents a brief introduction to the area of analog IC design automation, with special emphasis to the automatic layout generation. First, the analog design problem is characterized, then, a well-accepted design flow for analog IC is presented, and finally, LAYGEN II features are outlined.

Chapter 2 starts by addressing the placement problem in EDA, providing a brief overview of the most recent placement tools developed, followed by the presentation of the main references of automatic layout generation tools, and the recent advances in layout-aware analog synthesis approaches. Finally, the available commercial solutions for analog layout automation are outlined.

Chapter 3 gives an overview of the proposed automatic flow for analog IC design, with emphasis on the layout generation task, followed by a general description of the layout generation flow using LAYGEN II. Finally, additional detail about the tool's implementation, inputs, outputs, and interfaces is provided. These interfaces are used by the designer to quickly generate and monitor the automatic generation of the target layout.

Chapter 4 presents the methods used by the Placer to process and place the modules in the floor plan, while following the designer guidelines embedded in the template. First, the general architecture of the Placer is addressed, followed by the description of the high level guidelines present in the template. Finally, the detailed generation procedure for the floor plan, depicting each task implemented in LAYGEN II's template-based Placer is presented.

Chapter 5 covers the general description of the Router architecture, followed by the description of the template information necessary for routing, namely, the connectivity and routing constraints. Then the routing generation procedure is explained, depicting each task implemented in LAYGEN II's optimization-based Router, with emphasis on the evolutionary computational techniques used. Finally, the internal evaluation procedure used to verify if the routing solutions fulfill all the technology design rules and constraints is detailed.

Chapter 6 illustrates the application of the proposed design flow to practical examples. First, a fully dynamic comparator is considered to compare the LAYGEN II results with a hand-made layout using the UMC 130 nm design process. Then, a single-ended folded cascade amplifier is selected to explore the retargetability characteristics of the proposed methodology, using both the UMC 130 nm and the AMS 350 nm design processes.

Chapter 7 summarizes the provided book and supplies the respective conclusion and future work.

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