Preface

Analog and mixed-signal circuits continue to play a major role in modern technologies. Obviously, interfacing with antennas, wires, microphones and image sensors requires analog signal processing such as signal amplification, filtering and conversion from analog to digital. A/D-converters are bridges between the analog real world and the digital world. In practical applications the A/D-converters often become bottlenecks and their design is critical to overall system performance. Furthermore, the A/D-converters show a significant impact on system efficiency (power consumption), product costs (chip area) and robustness. Nevertheless, digital circuits drive the market such as microprocessors and system-on-chip solutions. The technology development has been optimized over the last decades to reduce the power consumption and chip area of digital circuits. Contrarily, the implementation of analog circuits has become more difficult using these modern semiconductor technologies. Smaller transistor sizes come along with a reduced tolerable voltage range resulting in a more challenging design. As a consequence, modern CMOS technologies drive the need for novel architectures to keep pace with improving efficiency of A/D-conversion.

The emphasis of this book is on practical design aspects for broadband analog-to-digital converters for communications. The embedded designs are employed for transceivers in the field of Asymmetric Digital Subscriber Line (ADSL) solutions and Wireless Local-Area Network (WLAN) applications. An area- and power-efficient realization of a converter is mandatory to remain competitive in the market. The right choice for the converter topology and architecture needs to be done very carefully to result in an attractive figure-of-merit (FOM). The book begins with a brief overview of basic concepts about ADSL and WLAN to understand the requirements on Analog-to-Digital (A/D) converters. In both fields of applications it will turn out that a delta-sigma approach is a good choice for fulfilling all requirements. At architecture level, issues on different modulator topologies are being discussed employing the provided technology node. The technology features influence the choice of different architectures in order to improve the circuit implementation. The design issues are pointed out in detail for modern digital Complementary Metal-Oxide-Semiconductor (CMOS) technologies, beginning with 180 nm and go-

ing down to 65 nm feature size. Beside practical aspects, challenges on mixed-signal design level are addressed to optimize the converters in terms of consumed chip area, power consumption and design for yield in high volume production. Thus, careful considerations on circuit- and architectural-level are done by introducing a dynamic-biasing technique, a feedforward-approach and a resolution in time instead of amplitude resolution. In 180 nm CMOS, a 85 dB dynamic range multi-bit delta-sigma A/D converter as well as in 130 nm CMOS, a power optimized 14 bit switched-capacitor delta-sigma modulator, are designed for ADSL applications, achieving 1.8 $\frac{\text{pJ}}{\text{conv}}$ and 0.7 $\frac{\text{pJ}}{\text{conv}}$, respectively. In 65 nm CMOS, a design for a 10 bit delta-sigma converter with a signal bandwidth up to 20 MHz is presented for a baseband WLAN solution attaining 0.15 $\frac{\text{pJ}}{\text{conv}}$. A new architecture is introduced by a time-encoding technique replacing a conventional amplitude quantization.

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Kärnten, Austria Richard Gaggl

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