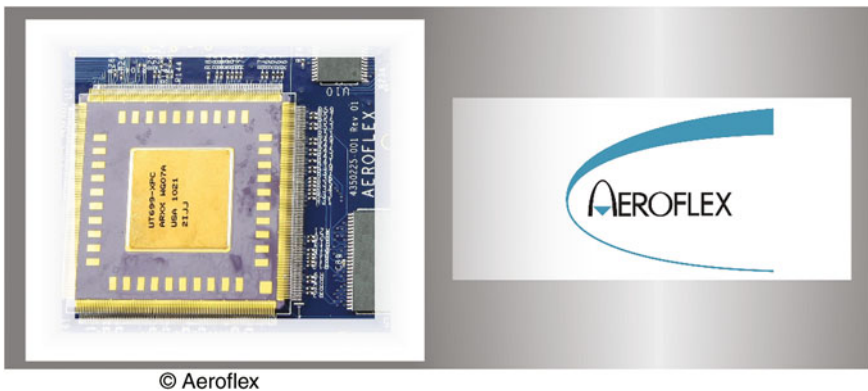


Chapter 2

The OBC Processor-Boards

Sam Stratton and Dave Stevenson



2.1 The Processor-Boards as ITAR Item

The Processor-Board as radiation hard component and as product of a United States company is classified as element falling under the ITAR (International Traffic in Arms Regulations). The boards produced for the University of Stuttgart are provided under the TAA (Technical Assistance Agreement), TA-6151-10. The contributions in this chapter from the side of Aeroflex Inc. have been verified by the Aeroflex legal department to be in agreement with the ITAR rules and the a.m. TAA.

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2.2 The Processor-Board: A Single Board Computer

The OBC Processor-Board was developed as a SBC (Single Board Computer), which also can be used for other purposes than controlling a satellite. Potential other applications in space could be as instrument controller for satellites or space station instruments and many other applications.

A Single Board Computer or SBC for short is a common term used for any computer that incorporates all of the essential components that a processor needs to perform its intended function. The SBC includes all of the memory resources, I/O and communication interfaces necessary to operate. The board is in fact a self-contained computer and functions as such without the need of additional circuit boards (Fig. 2.1).

Fig. 2.1 OBC processor-board flight model in the mounting frame. © Aeroflex Inc./IRS, Uni Stuttgart



Typical home computers do not implement an SBC as their Processor-Board. They will in most cases have a processor on a mother board with additional cards connected to the mother board for functions such as memory control and graphics processing for example. All computers have some basic requirements that are necessary for the computer to operate—requirements such as memory resources, interfaces including a keyboard and a monitor as well as communication interfaces such as Ethernet and USB.

Some of the first computer cards developed in the 1970s were of the SBC type. These were the early days of processor technology, so it was easier to incorporate all of the necessary resources and means of communicating with the processor on a single circuit board. As processor and other memory and interface technology progressed it became necessary to offload some of the functions to different cards. Functions such as Ethernet, memory controllers and graphics processing were typically implemented on separate circuit cards often called ‘daughter’ cards. Today, there are virtually no single board computers in the home PC market.

Though not typically used in home PCs, SBC computers are very typical in satellite applications as well as many industrial and aerospace computer systems. They are a much more specialized type of computer and in the case of satellite and military applications, are designed for more extreme environments.

In general, most SBCs used for satellite or automation purposes will implement specialized operating systems called RTOS (Real Time Operating Systems). One of the main concepts behind an RTOS is the idea commonly referred to as “determinacy”. Determinacy is the ability of a computer system to calculate with great accuracy the response time of any given process. Most satellite implementations of processors require the tasks performed by the processor to be very deterministic.

2.3 Technical Overview

The OBC Processor-Board is a Single Board Computer (SBC) that is designed to perform the main processor function within the OBC system. The board is designed and implemented based on requirements passed down from the University of Stuttgart to Aeroflex Colorado Springs. Requirements were then analyzed by Aeroflex and a design approach was arrived at in consult with the University of Stuttgart. The following subsections describe the flight version of the SBC and not the EM version due to the fact that there are some significant differences (Fig. 2.2).

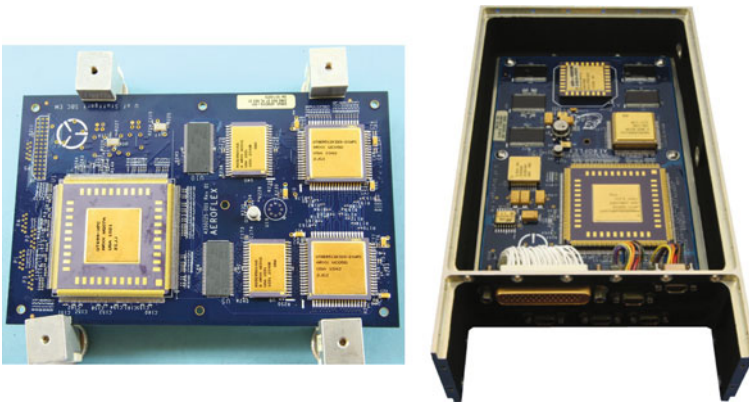


Fig. 2.2 Processor-Board engineering model and flight model. © Aeroflex Inc.

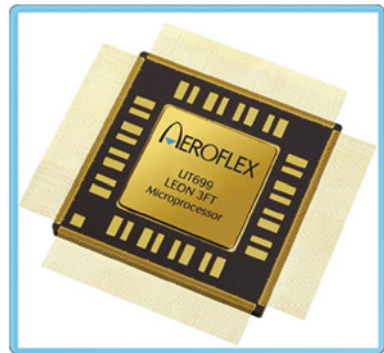
2.3.1 The OBC Microprocessor Device

The processor on an SBC is the heart of the board and is chosen based on the performance requirements of the program. In this case the term ‘performance’ is used in a much broader context than one would usually think. For a satellite,

or other high reliability application, performance is not just a reference to processing power but can and usually does include environmental and mechanical performance as well. The environmental performance capabilities are important because satellite OBCs will typically be subjected to much higher extremes of temperature, and mechanical stress than a typical home PC processor chip. Additional parameters that are considered when choosing a processor for a satellite application are power consumption as well as radiation performance. All of these requirements are important and are considered very carefully before a processor is chosen for any satellite program.

For the FLP satellite's OBC Processor-Board, the Aeroflex UT699 LEON3FT processor was chosen (Fig. 2.3). This processor is highly suited for satellite applications based on all of the above criteria. The LEON3FT is a 32 bit SPARC™ V8 device with many interfaces suitable for multiple types of implementations. For the FLP satellite program, it was decided at the program level to use SpaceWire as the primary interface between all of the boards in the OBC unit. SpaceWire is a high speed serial bus uniquely suited for inter-system communication and control of a satellite. The bus is essentially a bit shipping protocol with the data being defined by the user for their own specific needs. For a full description of the SpaceWire protocol please refer to [11] and [12].

Fig. 2.3 LEON3FT in CQFP package. © Aeroflex Inc.



2.3.2 The OBC Memory Configuration

All SBCs require memory in order to process data and perform tasks. Two different types of memory fulfill different functions inside an embedded computer:

Non-volatile Memory:

The first type of memory is known as non-volatile and is named as such due to the fact that when the power is removed from the board the device retains the data stored inside its cells. Non-volatile memory is essential because it typically contains the operating system the processor will use when it boots on power-up. In a home PC the non-volatile memory is fulfilled by the boot EEPROM and the

hard disk drive though in recent years we are seeing more and more solid state devices take the place of a hard disk. Since there are no hard disk drives that are qualified to fly in space, the non-volatile memory in a satellite needs to be of the solid state variety. Some types of non-volatile memory include Flash-Memory, EEPROM, FRAM, and MRAM. These devices will retain data when not powered.

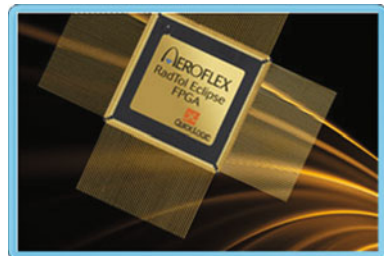
Volatile Memory:

The second type of memory on an SBC is referred to as volatile memory. Volatile memory will not retain data when the power is removed and therefore can only be used by the processor when it is powered up and performing its intended function. Common varieties of volatile memory include SRAM, Synchronous SRAM, Dynamic RAM or DRAM, and Synchronous Dynamic RAM or SDRAM. These are all examples of volatile memory. For satellite applications, the most common form of volatile memory is Static Random Access Memory (SRAM).

2.3.3 The OBC FPGA for Miscellaneous Functions

During the course of designing a processor system, requirements that are not easily fulfilled using a microprocessor, will often require implementation in discrete logic or most likely a Field Programmable Gate Array (FPGA). The FLP program has some OBC Processor-Board requirements that are not easily implemented with software on the LEON3FT. So the design team decided to implement these functions on a radiation tolerant FPGA (Fig. 2.4).

Fig. 2.4 UT6325 RadTol eclipse FPGA. © Aeroflex Inc.



The FPGA is typically a better choice over discrete logic because an FPGA will usually take up less space on the board and will also most likely use less power. The process of choosing an FPGA for a satellite system is similar to the process of choosing a microprocessor. Electrical, temperature as well as mechanical and radiation performance need to be considered prior to making a choice of FPGA. For the FLP satellite program the Aeroflex UT6325 in the CGA484 package was chosen for its radiation performance as well as for its relatively small footprint and ease of implementation. The device is well suited for housekeeping functions and other tasks that would be very difficult if not impossible to implement using discrete logic devices. The device is readily available and has good flight history.

2.4 The OBC Processor-Board Functional Overview

The OBC Processor-Board is a UT699 LEON3FT based 3U PCB card with 8 MB of on board SRAM and 4 MB of on board non-volatile FRAM memory. The primary method of communication on the OBC Processor-Board is through the four SpaceWire ports that are connected directly to the LEON3FT. The SpaceWire ports give access to and from the OBC Processor-Board and the other peripheral OBC Boards in the system. Additional interfaces include Ethernet and RS422 interface which are both used for ground testing and debug of the system. There is also a LEON3FT Debug Support Unit (DSU), that can be accessed using the front panel connector.

The on chip LEON3FT EDAC function has been implemented on the SBC for both the volatile and the non-volatile memory spaces. The following section discuss in more detail all of the interfaces on the SBC.

A top level functional diagram of the OBC flight board is shown in Fig. 2.5 which provides a graphical view of the overall design of the OBC Processor-Board.

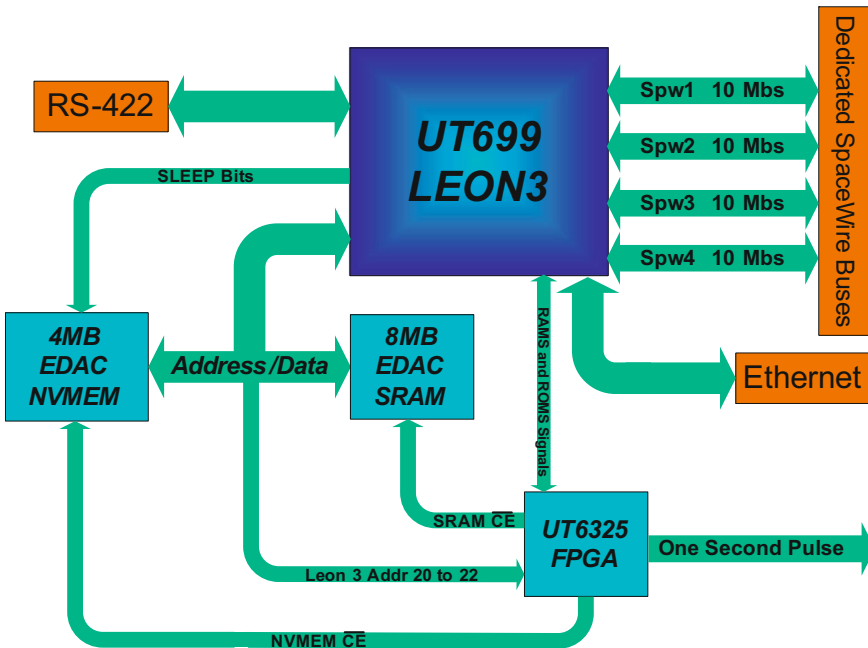


Fig. 2.5 OBC processor-Board block diagram (flight model). © Aeroflex Inc.

One important aspect that will be covered in more detail in later sections is the fact that the FPGA is handling the CE signals to both the volatile and non-volatile memories as explained in more detail in the following section.

2.5 The OBC Processor-Board Memory Interface

All microprocessors require memory to perform their desired function. The OBC Processor-Board memory interface was implemented based on requirements passed down from the University of Stuttgart to the designers at Aeroflex. Any issues or changes to the board during the design process were made in consult with the University.

The amount of on board memory contained on any Processor-Board is a very important element in the performance of the processor. This fact is true of home PCs as well as SBCs and follows the common understanding that more is better. As mentioned previously, the processor requires two types of memory—volatile and nonvolatile.

- **Non-volatile memory:** This type of memory will retain data even when the power to the board has been turned off. It is suitable for storing the processor operating system. This type of memory is similar in function to the boot EEPROM and hard disk used in home computers. It typically is slower than most types of volatile memory which however is acceptable since it is accessed only during boot-up of the computer.
- **Volatile memory:** This type of memory does not retain data when the power to the device is turned off. It is suitable for use by the processor when running its intended tasks (Fig. 2.6).

Fig. 2.6 Aeroflex stacked SRAM on Flight Unit. © Aeroflex Inc.



The amount of each type of memory on the board is dependent on the functional requirements of the board being designed. The non-volatile memory devices need to be dense enough to hold the entire RTOS image as well as any boot code that the user desires.

Non-volatile Memory Resources:

For the FLP satellite program it was decided to use FRAM devices for the flight configuration. On power up of the OBC board the LEON3FT will load the RTOS image from the FRAM devices to the SRAM for flight operation. The FRAM devices also have a ‘Sleep Bit’ that allows the user to set the device in a low power mode once the image has been loaded into SRAM. The interface on the SBC was

designed to use both of the ROM Select (ROMS) signals on the LEON3FT. ROMS[0] begins at address 0x00000000 and ROMS[1] begins at 0x10000000. Each bank of non-volatile memory provides 2 MB of SRAM to the LEON3FT.

Non volatile Interface to LEON3FT:

The non-volatile interface to the LEON3FT is fairly straight forward with the exception of the Chip Enable signals to the devices. The timing of these signals at the 33 MHz system clock used for the LEON3FT is not compatible with the FRAM devices under worst case conditions. It became necessary to use the on board FPGA to force these signals to meet the worst case timing of the FRAM device.

Fig. 2.7 LEON3FT NV memory interface. © Aeroflex Inc.

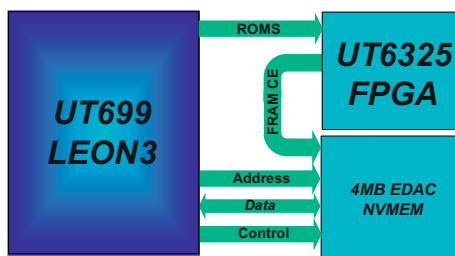


Figure 2.7 shows the top level interface from the LEON3FT to the FRAM devices. The ROMS signal from the LEON3FT to the FPGA, is essentially the Chip Enable signal from the LEON3FT. The FPGA manipulates the timing of the ROMS signal to create CE signals to the FRAM devices. The manipulation is such that the CE signals will meet the timing of the FRAMs and the system impact is the use of *three* wait states required when interfacing to the non-volatile memory space by the LEON3FT. Since these memories are not read from frequently, the impact to the processor performance is almost negligible.

- **LEON3FT Access to NVMEM:**

The LEON3FT processor has two Chip Enables for the ROM memory area on the device. The non-volatile memory devices are mapped into the ROMS[0] and the ROMS[1] space of the LEON3FT. The ROMS signals are Chip Enables for non-volatile memories. The result is there are two banks of 2 MB each of non-volatile memory on the FM SBC.

- **NVMEM Wait States:**

A minimum of *three* wait states need to be set in the LEON3FT Memory Configuration 1 (mcfg1) register when NVMEM accesses are performed. This is to ensure the timing of the LEON3FT interface using the FPGA to control the CE signals to the FRAM devices. The three wait states should be set for both read and write. Refer to the LEON3FT Functional Manual [50] for a detailed description of the mcfg registers in the LEON3FT. Note that on power up the default wait states for the PROM memory area are set to the maximum of 30.

- **NVMEM Sleep Bit Function:**
Each of the FRAM devices on the OBC Processor-Board has a ‘Sleep Bit’ that is used to put the device into a low power mode. Once the program code has been read from the LEON3FT and is stored into SRAM, it is recommended that the user sets these bits low when the devices are not being accessed. The sleep bits are connected to GPIO signals on the LEON3FT and they have pull-ups connected to them because the LEON3FT defaults all GPIO signals to inputs. Having the pull-ups ensures the LEON3FT will have access to the non-volatile memory space after power up or after the LEON has been reset by the FPGA.
- **Sleep Bit Implementation:**
The two Sleep Bits are implemented on the FM SBC using LEON3FT GPIO signals. Each one controls one bank of 2 MB of non-volatile memory. Table 2.1 explains these signals and identifies their default condition.

Table 2.1 NVSLEEP GPIO assignments

Signal name	LEON3FT I/O	GPIO assignment	Reset value	Description
NVSLEEP0	O	GPIO12	High	2 MB Bank 0 Sleep bit
NVSLEEP1	O	GPIO13	High	2 MB Bank 1 Sleep bit

- **NVMEM EDAC Implementation:**
The LEON3FT on chip EDAC has been enabled on the FM SBC. Refer to the LEON3FT Functional Manual for a full description of the EDAC for the PROM memory area.

Volatile Memory Resources:

The SBC contains 8 MB of on-board SRAM. When the LEON3FT is powered up or is reset, it will load the program code stored in the non-volatile memory space into the SRAM memory space. All of the processing for the OBC is done with code running from the SRAM memory space. The SRAM chosen for the OBC Processor-Board is an Aeroflex stacked SRAM device with four die inside a single package. A single RAM Select (RAMS) signal from the LEON3FT is routed to the FPGA and subsequently, four enables are generated from the FPGA to the SRAM device (Fig. 2.8).

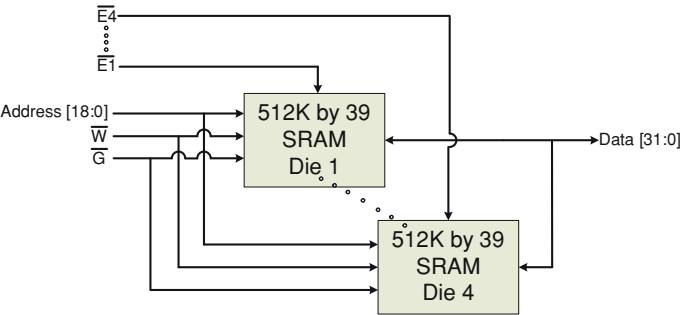
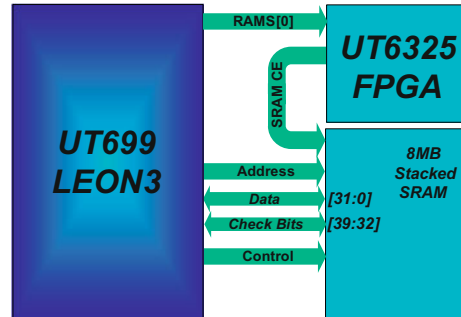


Fig. 2.8 Aeroflex 8 MB stacked SRAM with on chip EDAC bits. © Aeroflex Inc.

- **LEON3FT Access to SRAM:**

There are four Chip Enables on the LEON3FT. The OBC uses one of these signals along with upper address bits to control the four Chip Enable signals to the SRAM device. The 32 bit data bus on the LEON3FT is connected to the lower 32 bits of data on the SRAM device and the Error Detection and Correction (EDAC), check bits are connected to the upper 7 bits of data on the SRAM. Figure 2.9 shows a simplified version of this interface. The SRAM interface does not need any wait states set in the LEON3FT memory controller.

Fig. 2.9 LEON3FT SRAM interface. © Aeroflex Inc.



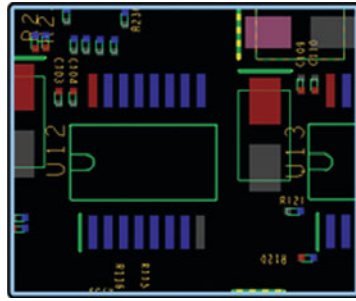
- **LEON3FT SRAM EDAC:**

One of the primary requirements for the OBC Processor-Board was to have all memories protected with EDAC. The OBC Processor-Board utilizes the LEON3FT on chip EDAC for the SRAM memory space. The Check bits on the LEON3FT are connected to the SRAM data bits [39:32]. Memory controller registers manage the function of the EDAC as well as their enabling on the SBC. The reader is referred to the LEON3FT Functional Manual [50] for a description of how the EDAC functions are enabled for the SRAM space.

2.6 The OBC Processor-Board SpaceWire Interface

SpaceWire is a point to point serial bus that supports full duplex communication at a data rate of up to 200 Mbs. The protocol uses a simple 'token' based system to manage data to and from each end point. Each token character tells the receiver of the token that the transmitter has 8 bytes of data space available in its receive buffer. Therefore, if a SpaceWire node has data to send it will send 8 bytes of data for each token it receives. The resulting function is simply as follows: As long as each side has data to send, and the data that gets received is taken out of the receive buffer, the system keeps running. For the FLP satellite program, the SBC implements all four of the dedicated SpaceWire ports on the LEON3FT micro-processor operating at 10 Mbs (Fig. 2.10).

Fig. 2.10 LVDS quad driver footprint on SBC layout. © Aeroflex Inc.



SpaceWire Ports Management:

All four SpaceWire ports on the LEON3FT are enabled for operation using LEON3FT SpaceWire registers. These registers control a number of important characteristics of the SpaceWire ports. Characteristics such as Port Enable, initialization data rate, disconnect time and timeout duration to name a few. The registers are discussed in detail in the LEON3FT User's Guide [50] and the reader is encouraged to refer to this document for detail discussion of the LEON3FT SpaceWire registers.

SpaceWire Clock and Data Rate:

The SBC implements the SpaceWire clock input to the LEON3FT using a 10 MHz oscillator. The registers that set the transmit data rate are set such that the SpaceWire ports operate at 10 Mbs.

2.7 Miscellaneous Functions

The OBC Processor-Board has a number of miscellaneous functions that are not suitable for the LEON3FT microprocessor. These functions have been designed into the UT6325 FPGA and are discussed in the following sections. FPGAs are uniquely suited for Processor-Board utility functions and the UT6325 is used by the OBC Processor-Board designers (Fig. 2.11).

Fig. 2.11 UT6325 in CQFP package. © Aeroflex Inc.



2.7.1 NVMEM Chip Enable

As stated previously, the FM22L16 FRAM devices chosen for the OBC Processor-Board have timing that is incompatible with the timing of the LEON3FT. Therefore, certain signals required to control the memory need to be managed by the on-board FPGA. The signals in this instance are the FRAM Chip Enables. The internal logic of the FPGA ensures the proper timing over worst case flight conditions.

2.7.2 SRAM Chip Enable

The LEON3FT is not designed to interface directly with SRAM devices that implement a stacked die configuration. The used UT8ER2M39 SRAM devices have four die layers inside one package. The on-board FPGA uses one of the Chip Enables from the LEON3FT along with upper address bits to generate the four Chip Enables to the SRAM devices.

2.7.3 Pulse Per Second Interface

A very good example of a utility function suited for an FPGA is the Pulse Per Second requirement (PPS). The signal is used to sync the star tracker interface of the FLP satellite to the LEON3FT. The signal is generated by the on-board FPGA and provided on the 44 pin D-sub connector. Generating this type of signal using MSI devices would require four or five separate chips and would also most likely take up more board space than the FPGA.

The one second pulse is shown in Fig. 2.12 and this scope plot was taken from the OBC FM unit. The timing is measured from the rising edge to the next rising edge. The timing parameters for the signal are shown in Table 2.2. The signal is also routed to one of the GPIOs on the LEON3FT. That way, the signal can be monitored by the LEON3FT if the user desires. The GPIO used for this input is GPIO 10.

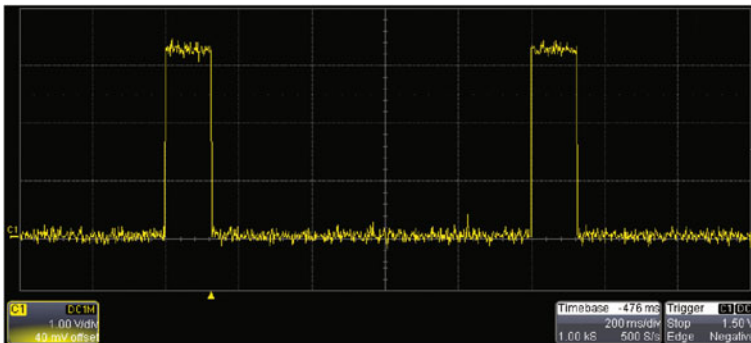


Fig. 2.12 Processor-Board oscilloscope plot of the PPS signal. © Aeroflex Inc.

Table 2.2 Pulse accuracy depending on operating temperature

Temperature range (°C)	Minimum pulse frequency (Hz)	Maximum pulse frequency (Hz)
−55 to +125	0.9999950	1.0000500

One Second Pulse Reset:

There is a signal connected to LEON3FT GPIO 15 and routed to the FPGA that is used to reset the one second pulse. The minimum pulse width in order to reliably reset the one second pulse is two system clock cycles.

2.7.4 Watchdog Signal and LEON3FT Reset

The LEON3FT has a watchdog trip signal on chip and the OBC processor routes that signal to the FPGA. When enabled, the logic inside the FPGA will use the watchdog signal trip to reset the LEON3FT.

Watchdog Trip Enable:

The LEON3FT GPIO14 has been setup to enable the reset of the LEON3FT when a watchdog trip occurs. If GPIO14 is set ‘High’ by the LEON3FT and there is a LEON3FT watchdog trip, the LEON3FT will be reset by the FPGA. The default upon power-up of the Watchdog Trip Enable is disabled (Low).

2.7.5 RS422 Interface

The RS422 interface is implemented using a combination of the inputs on the P5 connector, the LEON3FT GPIO signals and the LEON3FT on chip UART. See also Fig. 2.14.

Unused Transmit and Receive Signal Handling:

If the user does not wish to use the RS422TXEN and RS422RXEN input signals the following settings must be applied:

In the GPIO port direction register at address 0x80000908, bits [5] and [6] have to be set to ‘High’. This will set GPIO5 and GPIO6 to outputs.

2.7.6 Resets

All digital circuit boards need to be reset at the very least on power up. The OBC processor is no exception. There is a Power On Reset circuit that will hold the LEON3FT in reset until the input power is stable (Fig. 2.13).

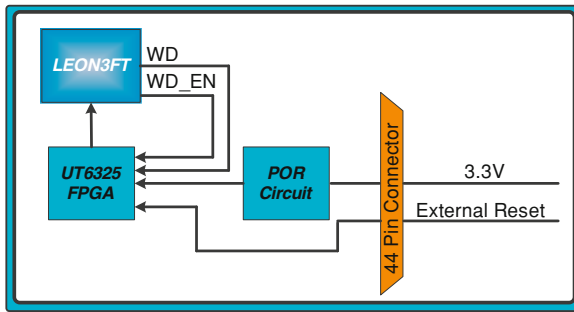


Fig. 2.13 Processor-Board reset lines. © Aeroflex Inc.

POR Reset:

The Power On Reset (POR) on the OBC Processor-Board is approximately 250 ms long. The LEON3FT and the FPGA will be reset at power-up. The FPGA is only reset at power-up and is designed to control the LEON3FT reset.

LEON3FT External Reset:

The external reset signal is provided through the 44 pin connector that is used for an external reset of the LEON3FT. The implementation of this signal should be such that when the user wants to reset the LEON3FT, this signal is to be pulled down to 'Low'. When the reset is terminated, the signal should be left floating. On the SBC, the FPGA performs the reset to the LEON3FT.

2.7.7 Clock Interfaces

LEON3FT System Clock:

The SBC implements the System Clock input to the LEON3FT using a 33 MHz oscillator.

SpaceWire Clock:

The SpaceWire clock as already cited is 10 MHz.

2.7.8 DSU/Ethernet Interface Card (DEI)

For debug and test of the OBC Processor-Boards—both EM and FM models—a small PCB card was designed by Aeroflex Colorado Springs to interface to the LEON3FT DSU and Ethernet ports respectively. Details on this card can be found in [Sect. 11.1](#).

The Ethernet interface on the LEON3FT is implemented by routing the signals from the LEON3FT to the 44 pin D-sub connector. During debug the user will use the DSU/Ethernet Interface card to implement the Ethernet connection.

The LEON3FT microprocessor on the OBC Processor-Board also has a Debug Support Unit (DSU) on the device and these signals are routed on the SBC to the 44 pin D-sub connector. When attempting to access the DSU, the user will use the DSU/Ethernet Interface card.

2.8 Power Specifications

The SBC has a 44 pin D-sub connector which is used for the $3.3\text{ V} \pm 5\%$ input power. In addition there are five MDM 9 pin connectors, 4 of which are for SpaceWire interfaces and one for RS422. The SBC consumes a maximum of no more than 5w at full throughput.

2.9 Mechanical Design and Dimensions

The SBC is based on a 3U cPCI Printed Circuit Board (PCB). The dimensions are 100 mm by 160 mm. Refer to Fig. 2.14 for a conceptual drawing of the board and the connector placement.

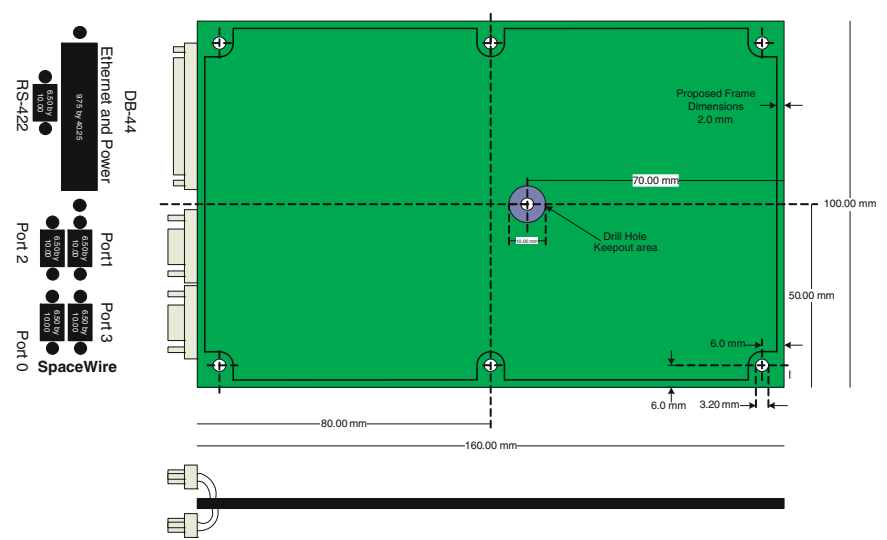


Fig. 2.14 Processor-Board mechanical concept. © Aeroflex Inc.

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