

# Contents

<b>Preface</b> . . . . .	v
<b>Contributors</b> . . . . .	xvii
<b>Acronyms</b> . . . . .	xix
<b>Symbols</b> . . . . .	xxiii
<b>1 Introduction to High-k Gate Stacks</b> . . . . .	1
Samares Kar	
1.1 Thin Tunneling SiO <sub>2</sub> Single Gate Dielectric . . . . .	2
1.2 The Need for High Permittivity Gate Stacks . . . . .	5
1.3 Important Material Constants of the Gate Stack . . . . .	6
1.4 Experimental Values of High-k Material Constants . . . . .	9
1.5 Correlation Between the High-k Material Constants . . . . .	10
1.6 MOSFET: Basics, Characteristics, and Characterization. . .	11
1.7 Hafnium-Based Gate Dielectric Materials . . . . .	12
1.8 Hafnium-Based Gate Stack Processing . . . . .	16
1.9 Metal Gate Electrodes . . . . .	19
1.10 Flat-Band and Threshold Voltage Control . . . . .	23
1.11 Channel Mobility . . . . .	25
1.12 Reliability Issues . . . . .	27
1.13 Lanthanide Based High-k Gate Stack Materials . . . . .	31
1.14 Ternary High-k Gate Stack Materials . . . . .	32
1.15 Crystalline Gate Oxides . . . . .	34
1.16 High Mobility Channels . . . . .	36
1.17 A Figure of Merit for a High-k Material as a Gate Dielectric . . . . .	39
1.18 Summary . . . . .	43
References . . . . .	44

<b>2</b>	<b>MOSFET: Basics, Characteristics, and Characterization . . . . .</b>	<b>47</b>
	Samares Kar	
2.1	Introduction . . . . .	48
2.2	MIS/MOS Structure: Single SiO <sub>2</sub> Gate Dielectric . . . . .	49
2.2.1	Metal-Semiconductor Contact (Schottky Barrier) . . . . .	49
2.2.2	Energy Band Diagram . . . . .	52
2.2.3	Equivalent Circuit Representation . . . . .	53
2.2.4	Electrostatic Analysis . . . . .	56
2.3	Flat-Band Voltage and Threshold Voltage: Single SiO <sub>2</sub> Gate Dielectric . . . . .	59
2.4	Capacitance–Voltage (C–V) Characteristics of the Si/SiO <sub>2</sub> /Metal Structures. . . . .	61
2.5	Drain Current–Voltage Characteristics of MOSFET with SiO <sub>2</sub> Gate Dielectric . . . . .	64
2.5.1	Ideal MOSFET: Linear Regime . . . . .	65
2.5.2	Classical Model . . . . .	67
2.6	High Dielectric Constant (k) Gate Stacks. . . . .	72
2.6.1	Drain Current–Voltage Characteristics of MOSFETs with High-k Gate Stacks . . . . .	73
2.6.2	Composition of the High-k Gate Stack . . . . .	85
2.6.3	Energy Profile of the High-k Gate Stack . . . . .	87
2.6.4	Occupancy of Interface Traps and Bulk Traps in the High-k Gate Stack . . . . .	91
2.6.5	Potential Well and Quantum-Mechanical Phenomena . . . . .	92
2.6.6	Trap Time Constant . . . . .	100
2.7	Nature of Traps and Charges in the High-k Gate Stack . . . . .	105
2.8	Potentials and Circuit Representations of the High-k Gate Stack . . . . .	108
2.8.1	Flat-Band Voltage Characteristics of High-k Gate Stack . . . . .	111
2.9	Impedance Characteristics of Leaky High-k MOS Structures. . . . .	114
2.9.1	Si Channels . . . . .	115
2.9.2	Ge and III–V Compound Semiconductor Channels . . . . .	118
2.10	Parameter Extraction Techniques . . . . .	119
2.10.1	Determination of the High-k Gate Stack Capacitance C <sub>di</sub> . . . . .	120
2.10.2	Extraction of the Surface Potential $\phi_s$ . . . . .	127
2.10.3	Different Techniques for Trap Parameter Extraction . . . . .	131

2.11	A Fundamental Basis for the Ultimate EOT . . . . .	145
2.12	Summary . . . . .	148
	References . . . . .	149
<b>3</b>	<b>Hafnium-Based Gate Dielectric Materials . . . . .</b>	<b>153</b>
	Akira Nishiyama	
3.1	Introductory Remarks and Brief Outline of the Chapter . . . . .	153
3.2	Properties Required for Gate Dielectrics . . . . .	154
3.3	Physical and Electrical Properties of Hafnium Oxide . . . .	156
3.3.1	Dielectric Constant and Microscopic Polarization . . . . .	157
3.3.2	Bandgap and Band Alignment with Silicon . . . . .	158
3.3.3	Compatibility with LSI Processes . . . . .	160
3.4	Hafnium–Nitrogen-Based Gate Dielectrics . . . . .	162
3.5	Hafnium–Silicon-Based Gate Dielectrics . . . . .	164
3.6	Hafnium–Aluminum-Based Gate Dielectrics . . . . .	171
3.7	Doped Hafnium-Based Gate Dielectrics . . . . .	174
3.8	Summary . . . . .	176
	References . . . . .	177
<b>4</b>	<b>Hf-Based High-k Gate Dielectric Processing . . . . .</b>	<b>183</b>
	Masaaki Niwa	
4.1	Introductory Remarks . . . . .	183
4.2	Hf-Based High-k Gate Dielectric Formation Process . . . .	184
4.2.1	Metal Organic Chemical Vapor Deposition . . . . .	184
4.2.2	Atomic Layer Deposition . . . . .	186
4.2.3	Precursors . . . . .	187
4.2.4	Physical Vapor Deposition . . . . .	188
4.2.5	Interfacial Oxide Layer . . . . .	190
4.3	Hf-Based Gate Dielectric Material and Its Intrinsic Phenomena . . . . .	192
4.3.1	Hf-Based Dielectric Material . . . . .	192
4.3.2	Crystallization and Related Issues . . . . .	193
4.3.3	Thermal Treatment and Interfacial Reaction . . . . .	197
4.3.4	Trapping Property . . . . .	204
4.3.5	Doping Effect . . . . .	206
4.4	Device Processing of Hf-Based High-k FET/CMOS . . . . .	209
4.4.1	Bi-Layer System . . . . .	209
4.4.2	Oxidation of Metallic-Hf . . . . .	211
4.4.3	EOT Scaling . . . . .	215
4.4.4	Process Control . . . . .	217

4.4.5	EOT Dependence on Gate Electrode . . . . .	223
4.4.6	Influence of Processing on Device Performance . . . . .	226
4.5	Summary . . . . .	231
	References . . . . .	232
<b>5</b>	<b>Metal Gate Electrodes . . . . .</b>	<b>235</b>
	Jamie K. Schaeffer	
5.1	Reasons for Using Metal Gate Electrodes . . . . .	235
5.1.1	Elimination of Gate Depletion . . . . .	236
5.1.2	Incompatibility of High-k Materials with Poly-Si Gates . . . . .	237
5.2	Work Function Considerations for Metal Gate Electrodes . . . . .	238
5.2.1	Work Function Requirements of Devices . . . . .	238
5.2.2	Methods of Achieving Desired Effective Work Function . . . . .	239
5.3	CMOS Metal Gate Integrations . . . . .	252
5.3.1	Materials Considerations for Metal Gate Electrodes . . . . .	252
5.3.2	Gate First Integration . . . . .	254
5.3.3	Gate Last or Replacement Gate Integration . . . . .	258
5.4	Conclusions . . . . .	259
	References . . . . .	259
<b>6</b>	<b><math>V_{FB}/V_{TH}</math> Anomaly in High-k Gate Stacks . . . . .</b>	<b>263</b>
	Akira Toriumi and Toshihide Nabatame	
6.1	Introduction . . . . .	263
6.2	Anomalous $V_{TH}$ in Si-Gate/High-k MOSFETs . . . . .	264
6.2.1	Poly-Si/High-k MOSFETs . . . . .	265
6.2.2	FUSI High-k MOSFETs . . . . .	267
6.2.3	Oxygen Vacancy . . . . .	269
6.3	Anomalous $V_{TH}$ in Metal/High-k MOSFETs . . . . .	271
6.3.1	Metal/High-k MOSFETs . . . . .	271
6.3.2	Interface Dipole at High-k/SiO <sub>2</sub> Interface . . . . .	272
6.3.3	Dipole Formation Model at High-k/SiO <sub>2</sub> Interface . . . . .	276
6.4	Top or Bottom Interface Dipole? . . . . .	279
6.5	Summary . . . . .	280
	References . . . . .	281
<b>7</b>	<b>Channel Mobility . . . . .</b>	<b>283</b>
	Chadwin Young	
7.1	Introductory Remarks and Brief Outline of the Chapter . . . . .	284

7.2	Background on Mobility and the Different Carrier Scattering Mechanisms . . . . .	284
7.2.1	Phonon Scattering . . . . .	285
7.2.2	Surface Roughness Scattering . . . . .	286
7.2.3	Coulomb Scattering . . . . .	286
7.3	Different Factors of Mobility Degradation in High-k Gate Dielectrics . . . . .	286
7.3.1	Fast Transient Charge Trapping in the High-k Bulk . . . . .	287
7.3.2	Interface Quality . . . . .	289
7.3.3	High-k Dielectric Properties . . . . .	290
7.4	Different Techniques for the Extraction of Channel Mobility . . . . .	292
7.4.1	Split C–V and Conventional $I_D$ – $V_G$ Correction Technique . . . . .	293
7.4.2	Direct Measurement of Inversion Charge Using Charge Pumping (CP) . . . . .	293
7.4.3	Pulsed I–V with Model Fitting and Parameter Extraction . . . . .	294
7.5	Process Optimization . . . . .	295
7.5.1	High-k Layer . . . . .	295
7.5.2	Interfacial Layer . . . . .	295
7.6	High Mobility Channels and Substrates . . . . .	295
7.6.1	Orientation Dependent Mobility Enhancement . . . . .	296
7.6.2	Strain and Germanium-Based Channels . . . . .	299
7.6.3	Compound Semiconductors . . . . .	300
7.7	Summary . . . . .	303
	References . . . . .	303
<b>8</b>	<b>Reliability Implications of Fast and Slow Degradation Processes in High-k Gate Stacks. . . . .</b>	<b>309</b>
	Gennadi Bersuker	
8.1	Introduction . . . . .	309
8.2	Instability Due to Pre-existing Defects . . . . .	311
8.2.1	Fast Transient Instability . . . . .	312
8.2.2	Correction for Fast Instability Process . . . . .	317
8.2.3	Slow Instability . . . . .	321
8.3	Defect Generation . . . . .	324
8.3.1	SILC as Gate Stack Degradation Monitor . . . . .	325
8.3.2	SILC Origin . . . . .	328
8.3.3	Verification of SILC Factors . . . . .	333

8.3.4	Fast Defect Generation Caused by Hole Injection . . . . .	336
8.4	Concluding Remarks . . . . .	339
	References . . . . .	339
<b>9</b>	<b>Lanthanide-Based High-k Gate Dielectric Materials. . . . .</b>	<b>343</b>
	Daniel J. Lichtenwalner	
9.1	Introduction to Lanthanide Dielectrics . . . . .	343
9.2	Lanthanide Materials Properties . . . . .	344
	9.2.1 Physical/Structural Properties . . . . .	345
	9.2.2 Electrical/Dielectric Properties . . . . .	346
9.3	Thin-Film Deposition and Processing . . . . .	349
	9.3.1 Physical Vapor Deposition . . . . .	349
	9.3.2 Chemical Vapor Deposition and Atomic Layer Deposition . . . . .	350
9.4	Lanthanide-Based Dielectric Gate Stacks . . . . .	351
	9.4.1 Lanthanum Oxides and Silicates . . . . .	351
	9.4.2 Aluminates and Scandates . . . . .	357
	9.4.3 Hafnates and Zirconates . . . . .	358
	9.4.4 Multi-Component Dielectrics Summary . . . . .	360
9.5	Threshold Voltage Control . . . . .	360
	9.5.1 nMOSFET $V_T$ Control Strategies . . . . .	361
	9.5.2 pMOSFET $V_T$ Control Strategies . . . . .	362
9.6	Epitaxial Lanthanide High- $\kappa$ Gate Dielectrics . . . . .	362
9.7	Lanthanide Dielectrics on High-Mobility Semiconductors . . . . .	362
9.8	Processing, Scaling, and Integration Issues . . . . .	364
9.9	Summary of Lanthanide Materials and Properties . . . . .	365
	References . . . . .	365
<b>10</b>	<b>Ternary <math>\text{HfO}_2</math> and <math>\text{La}_2\text{O}_3</math> Based High-k Gate Dielectric Films for Advanced CMOS Applications . . . . .</b>	<b>371</b>
	Akira Toriumi and Koji Kita	
10.1	Introduction . . . . .	371
10.2	Dielectric Films for CMOS Applications . . . . .	372
	10.2.1 Figure-of-Merit for High-k Dielectric Films . . . . .	372
	10.2.2 Dielectric Constant and Molecular Polarization . . . . .	374
	10.2.3 Origin of Molecular Polarization . . . . .	376
10.3	$\text{HfO}_2$ -Based Ternary Oxides . . . . .	378
	10.3.1 Dielectric Constant and Structural Phase of Crystalline $\text{HfO}_2$ . . . . .	378
	10.3.2 Control of Structural Phase in $\text{HfO}_2$ . . . . .	379
10.4	$\text{La}_2\text{O}_3$ -Based Ternary Oxides . . . . .	385

10.5	Amorphous Ternary High-k Dielectrics . . . . .	386
10.6	Summary . . . . .	392
	References . . . . .	393
<b>11</b>	<b>Crystalline Oxides on Silicon . . . . .</b>	<b>395</b>
	H. Jörg Osten	
11.1	Introductory Remarks . . . . .	396
11.2	Lanthanide Oxides on Silicon. . . . .	398
11.3	Epitaxial Growth of Lanthanide Oxides on Silicon . . . . .	401
11.4	Electrical Characterization . . . . .	402
11.5	Impact of Oxygen Concentration on Layer Properties . . . . .	404
11.6	Effect of Domain Boundaries . . . . .	408
11.7	Influence of Interface Engineering . . . . .	409
11.8	Impact of Post-Growth Processing . . . . .	413
11.9	Further Applications of Crystalline Lanthanide Oxides . . . . .	418
11.10	Summary and Outlook. . . . .	420
	References . . . . .	421
<b>12</b>	<b>High Mobility Channels . . . . .</b>	<b>425</b>
	Michel Houssa, Peide Ye and Marc Heyns	
12.1	Introduction . . . . .	425
12.2	Challenges Facing High- $\kappa$ Dielectrics on High Mobility Substrates . . . . .	427
12.3	Passivation of Ge for p-MOSFETs . . . . .	428
	12.3.1 Epi-Si Layer Passivation . . . . .	430
	12.3.2 Thermal Germanium Oxide as a Passivating Layer . . . . .	434
	12.3.3 Possible Alternative High- $\kappa$ Gate Dielectrics for Ge Substrates . . . . .	438
12.4	Passivation of GaAs and InGaAs for n-MOSFETs . . . . .	439
	12.4.1 Surface Chemistry and Integration of Atomic Layer Deposition . . . . .	440
	12.4.2 III–V Substrates Engineering for Majority and Minority Carrier MOSFETs . . . . .	443
	12.4.3 Methodology for III–V Interface Characterization. . . . .	447
12.5	Summary . . . . .	452
	References . . . . .	454
	<b>Appendix I: Fundamental Constants . . . . .</b>	<b>459</b>
	<b>Appendix II: Periodic Table of the Elements . . . . .</b>	<b>460</b>
	<b>Appendix III: Physical Constants of Semiconductors . . . . .</b>	<b>463</b>
	<b>Appendix IV: Physical Constants of Si, Ge, GaAs. . . . .</b>	<b>468</b>

<b>Appendix V: Physical Constants of High Permittivity Dielectrics . . . .</b>	<b>470</b>
<b>Appendix VI: Electronegativity Table of the Elements . . . . .</b>	<b>475</b>
<b>Appendix VII: Work Function Table of the Elements. . . . .</b>	<b>477</b>
<b>Index . . . . .</b>	<b>479</b>



<http://www.springer.com/978-3-642-36534-8>

High Permittivity Gate Dielectric Materials

Kar, S. (Ed.)

2013, XXXII, 489 p. 325 illus., 168 illus. in color.,

Hardcover

ISBN: 978-3-642-36534-8