

Preface

Integrated circuits (ICs) are becoming increasingly susceptible to uncertainty caused by soft errors, inherently probabilistic devices, and manufacturing variability. As device technologies scale, these effects can be detrimental to circuit reliability. In order to address this issue, we develop methods for analyzing, designing, and testing circuits subject to probabilistic effects. The main contributions of this work are: (1) a matrix-based reliability analysis framework that can capture probabilistic behavior at the logic level, (2) test generation and test compaction methods aimed at probabilistic faults in logic circuits, (3) a fast, soft-error rate (SER) analyzer that uses functional-simulation signatures to capture error effects, and (4) novel design techniques that improve reliability using little area and performance overhead.

First, we develop a formalism to represent faulty gate behavior by means of stochastic matrices called probabilistic transfer matrices (PTMs). PTM algebra provides a stochastic alternative to the deterministic role played by Boolean algebra. To improve computational efficiency, PTMs are, in turn, compressed into algebraic decision diagrams (ADDs), and ADD algorithms are developed for the corresponding matrix operations.

We propose new algorithms for circuit testing under probabilistic faults. This context requires a reformulation of existing techniques for circuit testing. For instance, a given fault may remain undetected by a given test vector, unless the test vector is repeated sufficiently many times. Also, since different vectors detect the same fault with different probabilities, the number of repetitions required is a key issue in probabilistic testing. We develop test generation methods that account for these differences, and linear programming (LP) formulations to optimize test sets for various objectives.

Next, we propose simulation-based methods to approximately compute reliability under probabilistic faults in practical settings. We observe that the probability of an error being logically masked is closely related to node testability. We use functional-simulation signatures, i.e., partial truth tables, to efficiently compute testability measures (signal probability and observability). To account for timing masking, we compute error-latching windows from timing analysis information.

Electrical masking is incorporated into our estimates through derating factors for gate error probabilities. The SER of a circuit is computed by combining the effects of all three masking mechanisms within a SER analyzer called AnSER.

Based on AnSER, we develop several low-overhead techniques that increase reliability, including: (1) a design method called SiDeR to enhance circuit reliability using partial redundancy already present within the circuit, (2) a guided local rewriting technique to resynthesize small windows of logic to improve area and reliability simultaneously, and (3) a post-placement gate-relocation technique that increases timing masking by decreasing the error-latching window of each gate, and (4) ILP algorithms to retiming sequential circuits for increased reliability and testability.

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