

Chapter 2

Sources of Variation

Variations in process, supply voltage and temperature (PVT) have always been an issue in Integrated Circuit (IC) Design. In digital circuits, PVT fluctuations affect the switching speed of the transistors and thus the timing of the logic. To guarantee fault-free operation for a specified clock frequency, IC designers have to quantify these uncertainties and account for them adequately. This is typically done by guard-banding, i.e. adding sufficient voltage safety margin to ensure proper working even under worst-case condition.

At recent technology nodes, transistor characteristics are more and more influenced also by aging effects. These wear-out effects, namely hot carrier injection (HCI) and bias temperature instability (BTI), degrade the drive current of transistors during use. Hence, further safety margin has to be added, dependent on the specified lifetime of a product.

The following four sections will give an overview of process, voltage and temperature variations as well as aging (PVTa). The necessary fundamentals are briefly explained and the impact on circuit-level timing is discussed.

2.1 Process Variations

As stated in the 2011 International Technology Roadmap for Semiconductors (ITRS) [12], “One of the key problems that designers face due to further shrinking of feature sizes is the increasing variability of design-related parameters, resulting either from variations of fabrication parameters or from the intrinsic atomistic nature which affects, e.g., channel doping.” The sources for the stated device variability are treated in the following. Afterward, the impact of process variations on digital circuits is discussed.

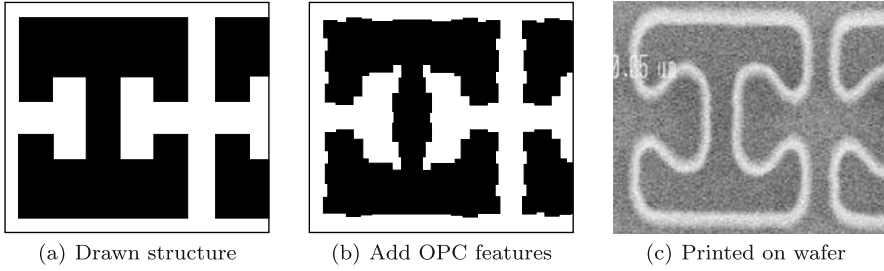


Fig. 2.1 Diffraction causes variations in width and length of transistors. Optical proximity correction (OPC) is used to attenuate these effects [14]

2.1.1 Imperfections of the Manufacturing Process

2.1.1.1 Variations in Critical Dimensions

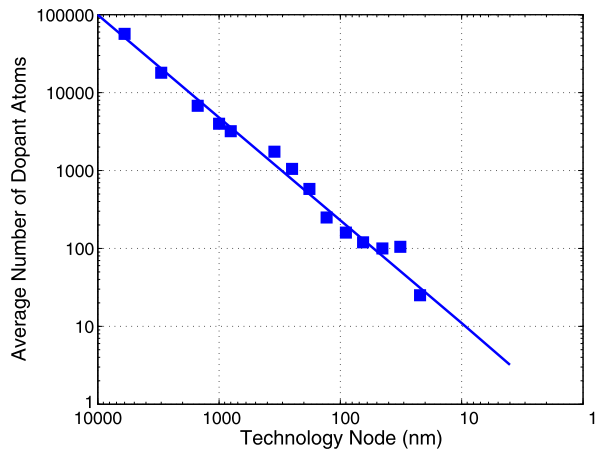
The wavelength of light, used for the lithography process, remained at $\lambda = 193$ nm since the 130 nm node [13]. Thus, it is exceeding more and more the minimum feature sizes, i.e. critical dimensions (CD), of transistors and the device structure gets increasingly blurred due to diffraction, see Fig. 2.1(c). Chip manufacturer try to reduce this effect by applying immersion lithography, phase-shift masks (PSM) and optical proximity correction (OPC), see Fig. 2.1(b). However, the relative fluctuations in transistor dimensions are rather increasing, as it is very challenging to reduce the absolute deviations in the same way as the shrinking feature sizes.

Variations of the transistor's width W and length L directly affect its drive current, which is proportional to W/L . Channel length fluctuations also change the threshold voltage V_t (roll-off effect) and this way additionally shift the drive current. Note that the channel length also varies randomly across the width of the transistor. The so-called line edge roughness (LER) is caused by statistical variations of the photon count or imperfections during photoresist removal [15]. LER increases the I_{off}/I_{on} current ratio for short channel devices used in digital circuits [16].

2.1.1.2 Random Dopant Fluctuation

The channel region of a transistor is doped with impurity atoms. These atoms are randomly placed into the channel—by techniques like dopant implantation—leading to statistical variations in the actual number of implanted impurities. Such a change of the carrier concentration shifts the threshold voltage and thus the drive strength of the transistor. In older technologies, with thousands of dopant atoms per channel region, an absolute deviation by several atoms was negligible. In recent technologies however the nominal number of impurities is only in the range of tens, see Fig. 2.2, leading to increased mismatch due to random dopant fluctuation (RDF).

Fig. 2.2 Number of dopant atoms per channel region over technology nodes [17]



2.1.1.3 Variation of the Gate Oxide Thickness

The gate oxide can be grown with an absolute accuracy of 1–2 inter atomic layers. In former technologies with an oxide thickness (TOX) of tens of inter atomic layers and large gates, TOX induced V_t variations were almost negligible. However, in technologies below 30 nm with oxide thicknesses between 1–3 nm (approx. 5–15 inter atomic spacings), TOX variations can contribute to the threshold voltage uncertainty as much as RDF [18].

2.1.2 Global and Local Process Variations

Usually, process variations are categorized into global and local variations. For global variations device parameters, such as oxide thickness or dopant concentrations, change equally for all transistors. Wafer-to-wafer or lot-to-lot variations fall into that category. In contrast, for local variations—also known as mismatch or random uncorrelated variations—each transistor is affected differently.

In other words, variations are distinguished by their spatial correlation distance. For local variations there is no correlation, whereas for global variations the correlation distance is very large. Note that there are also variation effects in between, leading to die-to-die and within-die variations. However, to cope with process fluctuations, it is still common practice to categorize them into global and local variations [19].

2.1.3 Impact of Process Variations on Digital Circuits

Variations of physical parameters (e.g. oxide thickness or doping concentration) lead to variations of electrical parameters, like threshold voltage or gate capacitance. In turn, this affects the performance of digital circuits as it changes gate delays or leakage currents.

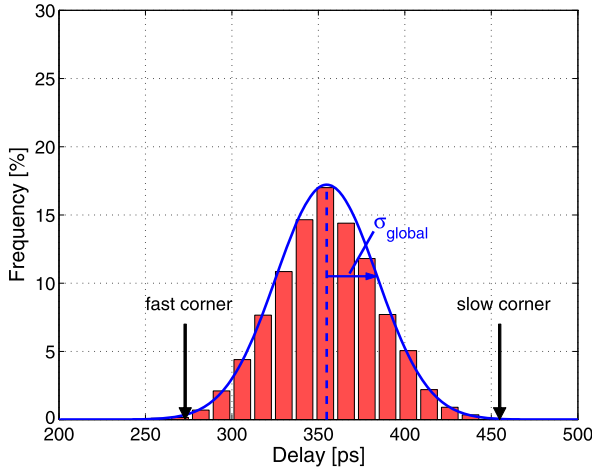


Fig. 2.3 Effect of global variations on the path delay. The depicted histogram results from MC simulations. The *arrows* represent the simulation results for fast and slow corner

2.1.3.1 Global Variations

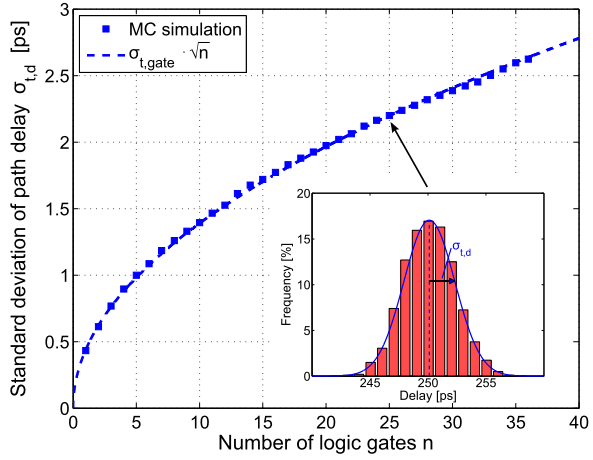
By performing Monte-Carlo (MC) simulations on transistor level, the effect of global variations on the circuit behavior can be explored. Probability distributions for the varying device parameters serve as input for MC simulations. The distributions are based on measured statistics of the manufactured transistors. Therefore, IC manufacturers add Process Control Monitoring (PCM) structures on the scribe-line of the wafers.

The histogram in Fig. 2.3 illustrates the delay of an inverter chain in 65 nm technology under global variations. The delay values of 2000 MC-runs are divided into bins of 12 ps width. As MC simulations are computationally intensive and hence hardly feasible for large designs, corner simulations are typically used to evaluate the impact of global variations.

The corners represent extreme cases, where the devices ultimately diverge from their nominal characteristics. For the fast corner, all process fluctuations increase the drive current of a transistor, leading to maximum speed. At slow corner, a device is ultimately slowed down by the process variations. The simulation results for fast and slow corner are also drawn into Fig. 2.3.

Fast and slow corner are typically defined by multiples of σ_{global} (e.g. three or six sigma) or founded on measured performance statistics of so-called split lots. For split lots, the manufacturing process (doping concentration, oxide thickness etc.) is intentionally biased to obtain extremely slow and fast chips. Besides fast and slow corner, also cross corners exist with maximum p-FET and minimum n-FET speed and vice versa. Cross corners are often critical in analog circuits, but are of minor importance in digital designs.

Fig. 2.4 Effect of local process variations on the path delay



2.1.3.2 Local Variations

Local variations, which are by nature uncorrelated, are increasing due to the scaling in CMOS technologies. This comes from the fact that with decreasing transistor dimensions, the standard deviation of threshold voltage $\sigma_{\Delta V_t}$ and current factor $\sigma_{\Delta k/k}$ ($k = \mu C_{ox} W/L$) are increasing, since they are proportional to the inverse of the square root of the active device area [20]

$$\sigma_{\Delta V_t} = \frac{A_{\Delta V_t}}{\sqrt{WL}} \quad \sigma_{\Delta k/k} = \frac{A_{\Delta k/k}}{\sqrt{WL}} \quad (2.1)$$

where $A_{\Delta V_t}$ and $A_{\Delta k/k}$ are matching parameters characterizing a particular process and manufacturing line.

The impact of local variations on the path delay can be described by a stochastic model of n equal logic gates with a switching time (rise or fall time) of t_{gate} and the corresponding standard deviation of $\sigma_{t,gate}$. The path delay $t_d = n \cdot t_{gate}$ increases linearly with n , whereas the standard deviation of the path delay $\sigma_{t,d}$ increases only proportional to the square root of n and reads as follows¹

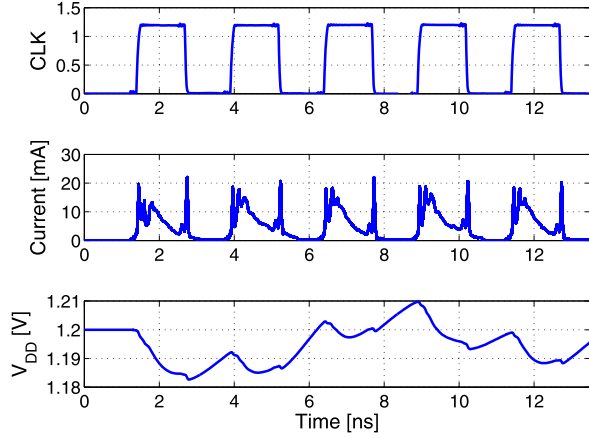
$$\sigma_{t,d} = \sqrt{n} \cdot \sigma_{t,gate} \quad (2.2)$$

Thus, the relative variation of the path delay $\sigma_{t,d}/t_d$ decreases proportionally to the inverse square root of n

$$\frac{\sigma_{t,d}}{t_d} = \frac{1}{\sqrt{n}} \cdot \frac{\sigma_{t,gate}}{t_{gate}} \quad (2.3)$$

¹The derivation for $\sigma_{t,d}$ can be found in the Appendix.

Fig. 2.5 Clock signal, current profile and resulting supply voltage of a 32-bit multiplier circuit. Close to the clock edges, a high current flow can be seen due to the switching activity of the circuit and flip-flops. The combination of IR-drop and di/dt noise in turn leads to voltage drops and—if resonance occurs—also to overshoots



It is a common pitfall, to think that the absolute uncertainty $\sigma_{t,d}$ decreases for long paths. However, only the *relative* uncertainty $\sigma_{t,d}/t_d$ decreases with the path length, whereas the absolute uncertainty $\sigma_{t,d}$ naturally increases, see Fig. 2.4.

2.2 Voltage Variations

2.2.1 Origin of Voltage Fluctuations

Supply voltage fluctuations are mainly caused by IR drop and di/dt noise. IR drop is caused by the current flow over the parasitic resistance of the power grid, whereas di/dt noise is due to the parasitic inductance in combination with capacitance and resistance of power grid and package. These fast changing effects—also called power noise—typically have time constants in the range of nano- to microseconds. Figure 2.5 shows an example of a supply current profile together with the resulting supply voltage sequence for a 32-bit multiplier circuit.

Considering only IR drop, the voltage bounce $\Delta V_{IR\ drop}$ is given by Ohms law

$$\Delta V_{IR\ drop} = R_{grid} \cdot i(t) \quad (2.4)$$

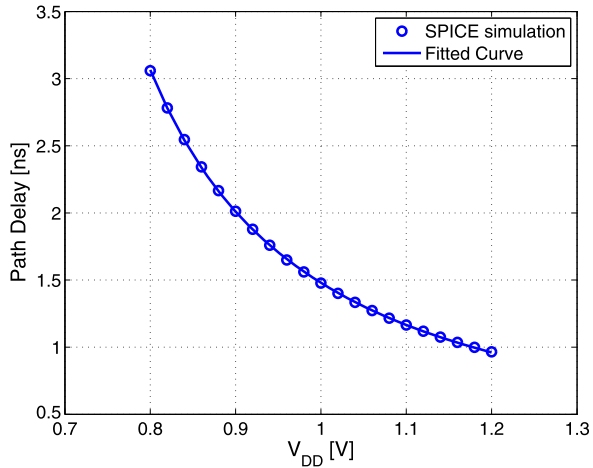
Additionally, the current flow through a parasitic inductance $L_{parasitic}$ causes the voltage bounce

$$\Delta V_{di/dt} = L_{parasitic} \cdot \frac{di}{dt} \quad (2.5)$$

The superposition of both effects can not only lead to voltage drops, but also voltage overshoots, as can be seen in Fig. 2.5.

Besides fast changing power noise effects, also offsets in the voltage regulator can lead to deviations from the nominal supply voltage. Offsets can either result from inaccuracies of the voltage regulator itself, e.g. a DC-DC or LDO regulator, or from the voltage reference circuit, often implemented as bandgap circuit.

Fig. 2.6 Relation between supply voltage and logic delay, illustrated by the most critical path of a multiplier circuit in 65 nm technology. The simulation results can be accurately fitted by Eq. 2.7



2.2.2 Impact of Voltage Changes on the Path Delay

The delay of a CMOS logic gate (e.g. an inverter or a NAND-gate) can be approximated by the following equation [21]

$$t_{gate} \propto \frac{V_{DD}}{b(V_{DD} - V_t)^a} \quad (2.6)$$

where a and b are gate specific fitting parameters and V_t is an effective threshold voltage. The delay of a complete path is obtained by summing up the single gate delays along this path. Consequently, the output delay t_d can be approximated by

$$t_d \propto \frac{V_{DD}}{b'(V_{DD} - V_t')^{a'}} \quad (2.7)$$

with path-specific parameters a' , b' and V_t' . Figure 2.6 shows the simulated path delay of a multiplier circuit for different supply voltages. By applying the appropriate input pattern, the most critical path was sensitized in the simulation. The solid line demonstrates the fit by Eq. 2.7.

2.3 Temperature Variations

Dependent on the thermal conductivity, the dissipated power affects the temperature of a chip. Power dissipation hence leads to global temperature variations as well as local fluctuations in regions of high-activity, so called hot-spots. Additionally, ambient temperature changes lead to global shifts in chip temperature.

Temperature fluctuations typically have time constants in the range of milliseconds to seconds [22]. An increase in temperature typically causes a circuit to slow down due to reduced carrier mobility and increased interconnect resistance, see

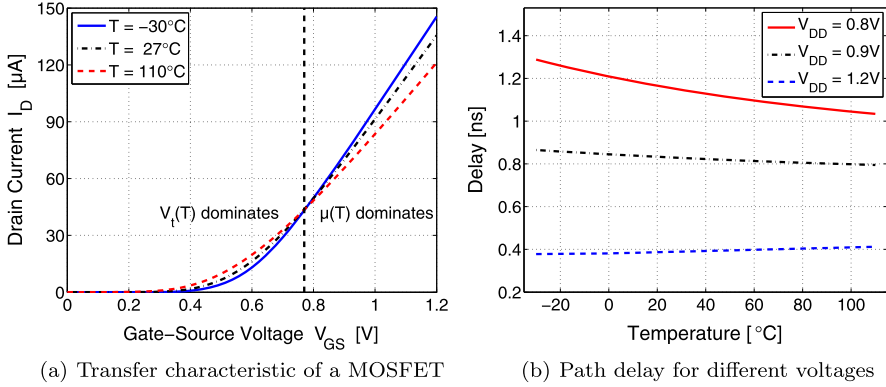


Fig. 2.7 Influence of temperature on device characteristic and path delay

Fig. 2.7(b) ($V_{DD} = 1.2$ V) and [23]. However, for low V_{DD} the circuit is operated in temperature inversion. Here, the effect of decreasing threshold voltage with temperature exceeds the mobility degradation, see Fig. 2.7(a). Consequently, the circuit exhibits an inverted temperature characteristic, as it speeds up with increased temperature and vice versa, see Fig. 2.7(b) ($V_{DD} = 0.8$ V and $V_{DD} = 0.9$ V).

2.4 Aging

Due to increasing electrical fields and new materials, transistor wear-out is of increasing concern in recent technologies. BTI- as well as HCI-effects degrade the speed of transistors during their lifetime and demand for additional safety margin.

2.4.1 Hot Carrier Injection (HCI)

Hot Carrier Injection mainly occurs during switching of logic gates. Carriers are accelerated in the lateral field under the oxide and gain sufficient kinetic energy to be injected into the gate dielectric. This effect is illustrated for an n-MOSFET in Fig. 2.8. The trapped charge increases the threshold voltage of the device and reduces its current drivability. Recent research on HCI is presented in [24].

2.4.2 Bias Temperature Instability (BTI)

BTI results from high vertical fields and thus mainly occurs when a transistor is operated in triode mode (linear region), i.e. high V_{GS} and low V_{DS} is applied. Figure 2.9 shows charge trapping by BTI for an n-FET, referred to as Positive Bias

Fig. 2.8 Hot Carrier Injection (HCI) for an n-MOSFET

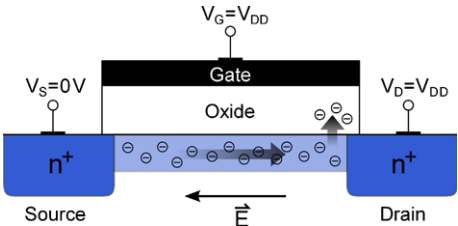
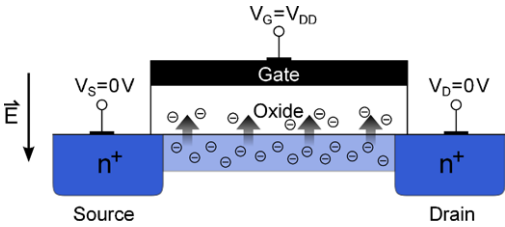


Fig. 2.9 Bias Temperature Instability (BTI) for an n-MOSFET



Temperature Instability (PBTI). Accordingly, the term NBTI is used in the case of a p-FET. PBTI and NBTI increase the threshold voltage of the device and slow down the switching speed [25].

Note that BTI-aging is caused by charge trapping and detrapping with a wide range of capture and emission times [26]. Therefore, small V_t -shifts can be observed already after very short stress times down to microseconds [27]. However, due to the distribution of the capture and emission time constants, considerable V_t -shifts arise only after days, weeks or even years. More details on BTI can be found in [28–31].

2.5 Summary

Figure 2.10 categorizes the discussed variations according to their time constants. As the dynamics of variation effects depend on various circumstances, the shown classification is rather qualitatively.

Process variations occur during fabrication and lead to fixed changes in device parameters. During operation, device characteristics can, however, still be affected by aging induced wear-out. As mentioned before, the trapping events leading to device aging have a wide variety of time constants. However, significant degradation of CMOS logic delays mainly develops in the long run. The temperature, also influencing circuit speed, changes rather slowly, whereas power noise has normally very short time constants.

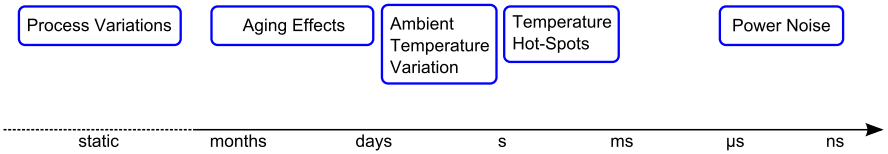


Fig. 2.10 Temporal classification of variations

The shorter the time constant of a variation effect, the more challenging becomes the voltage adaptation to it. In the following chapter, it is explained how Pre-Error AVS effectively handles slow as well as fast changing effects compared to state-of-the-art approaches.

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