

# Preface

Increasing performance demands in today's integrated circuits (ICs), together with limited energy budgets, force IC designers to think about new ways of saving power. One innovative way of doing so is presented in this work. The newly developed Adaptive Voltage Scaling (AVS) scheme tunes the supply voltage of digital circuits according to the present Process, Voltage and Temperature variations as well as Aging (PVT-A). The key components of the proposed approach are in-situ delay monitors (Pre-Error flip-flops), detecting late but still non-erroneous signal transitions (pre-errors). Based on the measured pre-error rate, the voltage is adjusted with a low-overhead control unit connected to the on-chip voltage regulator. This way power consumption is optimized, by exploiting unused timing margin, produced by state-of-the-art worst-case designs.

The presented Pre-Error AVS scheme adapts the voltage during normal circuit operation (on-line) and hence no test intervals, nor interaction with higher system levels is required. To describe the statistics of the closed-loop voltage control, a Markov chain model was developed, which is based on transistor level simulations. With this model, the power saving potential as well as the risk of overcritical voltage reductions can be analyzed very efficiently. Furthermore, the Markov model was extended in order to evaluate the robustness of the control-loop against global and local variations.

The elaborated approach was tested on an arithmetic and an image processing circuit, both synthesized in an industrial 65 nm low-power CMOS technology. For the two designs the Pre-Error AVS concept achieves dynamic power savings of 25 % (including all overheads) while ensuring an error rate below  $1\text{E-}9$ . At the same time the leakage power is reduced by over 30 %.

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