

Contents

- 1 Introduction 1**
 - 1.1 Transistor Scaling 1
 - 1.1.1 The Early Days (1925–1960) 1
 - 1.1.2 The Happy Days of Scaling (1960–2000) 1
 - 1.1.3 Materials-Based Scaling (2000–2010) 2
 - 1.2 What’s Next? (2010–...) 3
 - 1.2.1 High-Mobility Channel Materials 3
 - 1.2.2 Scalable Transistor Designs 4
 - 1.3 Goals of the Book 4
 - 1.4 Organization of the Book 5
- 2 Source/Drain Junctions in Germanium: Experimental Investigation 7**
 - 2.1 Introduction 7
 - 2.2 p-Type Junctions 8
 - 2.2.1 Furnace Annealed Gallium Junctions 8
 - 2.2.2 Furnace Annealed Boron Junctions 13
 - 2.2.3 Conclusions 15
 - 2.3 n-Type Junctions 16
 - 2.3.1 Laser Annealed Arsenic Junctions 16
 - 2.3.2 Conclusions 21
 - 2.4 Benchmarking 21
 - 2.4.1 Electrical Activation Requirements 21
 - 2.4.2 Benchmarking of USJ in Germanium 22
 - 2.4.3 Conclusions 24
 - 2.5 Summary and Conclusions 25
- Appendix 26
 - A.1 Thermal Laser Anneal—sprocess Simulation Parameters . . 26

3	TCAD Simulation and Modeling of Ion Implants in Germanium	27
3.1	Introduction	27
3.2	Ion Implant into Germanium—Monte Carlo Simulations	28
3.3	Ion Implant into Germanium—Analytical Description	32
3.3.1	Dual Pearson Distribution Functions	32
3.3.2	Analytical Model	33
3.3.3	Practical Applications	34
3.3.4	Conclusions	36
3.4	Application to a 70 nm Bulk Ge pFET Technology	36
3.4.1	Imitating Si Doping Profiles—‘Simulation’	36
3.4.2	Experimental Details	38
3.4.3	Electrical Characterization	40
3.4.4	Benchmarking	42
3.4.5	Conclusions	44
3.5	Summary and Conclusions	44
	Appendix	45
A.1	Calibrated Parameters for TaurusMC	45
A.2	Model Parameters: Ion Implants into Crystalline Ge	47
4	Electrical TCAD Simulations and Modeling in Germanium	49
4.1	Introduction	49
4.2	TCAD Models for a Germanium pMOSFET Technology	50
4.2.1	Modeling Mobility	50
4.2.2	Modeling Generation-Recombination	53
4.2.3	Modeling Interface Traps	56
4.3	Electrical TCAD Simulations—65 nm Ge pMOSFET Technology	57
4.3.1	Simulator Setup	57
4.3.2	I_D – V_G and I_D – V_D Simulations	58
4.3.3	Alternative Implant Conditions	58
4.3.4	Interface Traps	60
4.3.5	Conclusions	61
4.4	Impact of Interface Traps MOS Performance	61
4.4.1	TCAD Modeling and Electrical Characterization	62
4.4.2	Uniform Trap Spectra	62
4.4.3	Non-uniform Trap Spectra	63
4.4.4	Experimental Verification	68
4.4.5	Conclusions	70
4.5	Summary and Conclusions	70
	Appendix	71
A.1	TCAD Model Parameters	71
A.2	Recombination	72
A.3	Mobility	72

5	Investigation of Quantum Well Transistors for Scaled Technologies .	75
5.1	Introduction	75
5.2	Motivation—Scalability Issues in Bulk MOSFET Technologies . .	76
5.2.1	Drain Extension Leakage in a 65 nm Bulk Germanium pMOS Technology	76
5.2.2	Short Channel Effects in Bulk Si Technologies	78
5.2.3	Conclusions	82
5.3	Towards a Scalable Transistor Architecture	83
5.3.1	Heterostructures: Fermi Level Continuity	83
5.3.2	A Case Study: SiGe FETs	84
5.3.3	Conclusions	93
5.4	High Electron Mobility Transistors: an Alternative Approach . . .	93
5.4.1	HEMT with Interrupted Delta-Doping Layers	93
5.4.2	Implant-Free Quantum Well FET	94
5.4.3	Conclusions	96
5.5	Operation of Heterostructure Transistors: Analytical Description .	96
5.5.1	Transistor Structure	97
5.5.2	Approximations and Assumptions	97
5.5.3	MOS Capacitor	98
5.5.4	MOS Field Effect Transistor	101
5.5.5	Conclusions	102
5.6	Conclusions	103
6	Implant-Free Quantum Well FETs: Experimental Investigation . . .	105
6.1	Introduction	105
6.2	First-Generation SiGe Implant-Free Quantum Well pFET	106
6.2.1	Device Concept and Fabrication	106
6.2.2	Electrical Results and Discussion	108
6.2.3	Conclusions	111
6.3	Enhancing Performance in SiGe IFQW pFETs	111
6.3.1	Experimental Details	112
6.3.2	Source/Drain Stressors and TCAD Modeling	112
6.3.3	Electrical Results and Discussion	115
6.3.4	Conclusions	116
6.4	Second-Generation Strained SiGe IFQW pFETs	117
6.4.1	Device Fabrication	117
6.4.2	Electrical Results and Discussion	117
6.4.3	Conclusions	119
6.5	Matching Performance and V_T -Tuning in IFQW pFETs	119
6.5.1	Body Bias Sensitivity	120
6.5.2	Multi- V_T Technology	121
6.5.3	V_T Matching Performance	121
6.5.4	Conclusions	122

- 6.6 SiGe Quantum Well Diffusion Study 123
 - 6.6.1 Experimental Details 123
 - 6.6.2 Physical Analysis 123
 - 6.6.3 Conclusions 125
- 6.7 Conclusions 126
- 7 Conclusions Future Work and Outlook 127**
 - 7.1 Conclusions 127
 - 7.2 Future Work and Outlook 129
- References 131**

<http://www.springer.com/978-94-007-6339-5>

High Mobility and Quantum Well Transistors

Design and TCAD Simulation

Hellings, G.; De Meyer, K.

2013, XVIII, 140 p., Hardcover

ISBN: 978-94-007-6339-5