

Preface

Electromigration (EM) has been a dominant failure mechanism for integrated circuits' interconnections since the beginning of integrated circuits (IC). Extensive studies on electromigration, both theoretical and experimental, have been done in the past and modeling of electromigration that enable us to have a better understanding and prediction of the electromigration weak spots and time to failure are also developed. However, almost all the previous works are done on the test structures instead of at the circuit level, and as such, they are useful for the evaluation of interconnect technology in the wafer fabrication. With the increasing interaction between circuit performance and materials that make up an integrated circuit as we advance in IC technology nodes, will there be a difference in the electromigration behaviors between the test structure and circuit level? This book serves as an opening to address this question, and hopes to inspire more research to be done in this area.

In particular, this book aims to model the EM reliability of interconnects at circuit layout level using 3D model. In order to perform the modeling, a method to construct a 3D finite element (FE) circuit model from a given 2D IC layout must be developed so that the transient electro-thermo-structural simulations using both Cadence (a circuit simulator) and ANSYS (a finite element software) can be performed. In this book, a simple two-transistor circuit with two metal layers is used as the example to illustrate the method of such construction.

Once a 3D FE circuit model can be constructed for a given IC layout, and with the FE simulation, the EM weak spots of the interconnects in the IC can be analyzed to study the effects of current density, temperature gradient, and thermo-mechanical stress gradient on the EM reliability of an IC. With this analysis, one can compare the EM weak spots of a 3D circuit structure and a standard line—via test structure under both the EM test condition and the circuit operation condition to answer the question that we posed at the beginning, and the answer is Yes.

With a 3D FE circuit model, we can now examine how we can improve the EM reliability of a circuit based on the circuit model instead of the test structure. Along this rationale, we investigate the effects of barrier layer thickness, dielectric material, layout, and process modifications (e.g., interconnect structures, transistor placement, stress-free temperature of the metallization) on the EM reliability of

integrated circuits, without altering their functionalities and violation of circuit design rules.

It is our hope that this work can push the EM research from test structure to the “system level” so that the research outcome can have a more direct benefit to the circuit designers, leveraging on the maturing of the 3D EM models on test structures that have been reported in the literatures and the increasing computational power of modeling software. This is especially needed as we advance in the IC technology node where interaction between materials, devices, and circuits can no longer be neglected.

Electromigration Modeling at Circuit Layout Level

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