Introduction

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We introduce the emerging applications for ultra low power devices in this chapter. Moore's law continues to drive function integration. The transistor density is defined as the transistor number on one square silicon die that is generally considered the largest manufacturable die. Such a die can now hold over 7 billion transistors. It is about the same as the population of the planet. But whether those transistors are active or not, they consume power. To satisfy Moore's law, die size has been increasing at the rate of 7% per year. The operating frequency has doubled every two years. Therefore to meet the performance goal, the supply voltage scales by only ~15% every two years, rather than the theoretical 30%. Reduction in power consumption is not tracking Moore's Law. Additionally, at smaller geometries the cost of the fabrication is growing substantially, which affects wafer pricing. Hence both power reduction and cost reduction are not tracking Moore's Law. This inspires creative thinking and promotes research and development in low power circuits and architecture. So that raises some interesting challenges about power, cost, and performance that need innovative solutions.

System-on-chip (SoC) has become a reality since increasing complexity is driving new business models. SoC usually integrates all components of a computer or other electronic system into a single chip. The key electronic chip we focus on is a "system-on-chip", which is a must for most modern sophisticated devices. It is critical for chip designers to work directly with system designers or customers in product definition in order to meet the design requirements for power, cost, and performance.

In particular, we focus on short-channel effects, device parameter variations, excessive junction and gate oxide leakage, as the main obstacles dictated by fundamental device physics. Functionality of special circuits in the presence of high leakage, SRAM cell stability, bit line delay scaling, and power consumption in clocks

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and interconnects, are the primary design challenges. Soft error rate control and power delivery pose additional challenges. All of these problems are further compounded by the rapidly escalating complexity of SoC designs. The excessive leakage problem is particularly severe for battery-operated, high-performance SoCs.

1 Emerging Applications

The electronics industry has made spectacular progress since the invention of the integrated circuit in 1958. Discrete devices have been replaced by integrated circuits. In more than 50 years, the technology has rapidly evolved from producing simple chips with several components to fabricating very complicated chips containing billions of transistors. The number of transistors per chip has continued to increase exponentially over the years, which makes feasible more and more functions to be integrated into one chip. At the same time, the minimum feature size of transistors has dropped exponentially accordingly, which reduces both silicon area and cost per function. Most of the research and development efforts have been oriented towards increasing operation speed and complexity. This gives rise to the so-called high performance-to-cost ratio. While paying attention to speed and area, power consumption has been ignored or often considered as of minor concern.

The scenario is, however, undergoing some radical changes. Integrated circuits have incorporated more and more functions on each chip until now it is essentially possible to put an electronic system into a single silicon chip. This chip is termed as a SoC that usually integrates all components of a computer or other electronic system into a single chip. It may consist of digital, analog, and sometimes radio-frequency (RF) functions on a single chip substrate.

The motivation for ultra low power electronics has stemmed from two major requirements: (1) for portable or wearable implantable battery operated systems that are sufficiently small in weight and volume but require long battery operation time; (2) for batteryless systems in which energy is harvested from environment. For example, the chips in various sensor wireless networks can operate with energy harvested from environment, which will be widely used in the internet of thing (IoT) such as smart grid.

Nowadays, SoCs have obtained more and more functionalities. They have become smarter than ever before. Thanks to the rapid development of IC manufacture industry, on any of today's SoCs, extraordinary high dense transistors are integrated. They are the key devices or chips in systems such as portable or wearable medical electron devices, smart phones, wireless smart terminals, multi-media terminals, wireless sensor networks, wearable health care monitoring devices and so on. However, problems accompanying such high density of integration emerge such as dynamic power, leakage power, thermal issues, and limited battery operation hours. In most consumer electronic and bio-medical applications, devices are required to be portable, wearable or even implantable. Hence, the sizes of the systems are forced to be small. As a result compact batteries are required as energy sources for reaso-

nable operation time. Due to limited energy storage capacity of batteries, in order to guarantee a reasonable battery operation time, various low power design techniques are greatly demanded to make a drastic reduction of the power consumption.

Endoscopic capsule is such a kind of application that allows people to directly examine the entire intestine and does not require any sedation, anesthesia or insufflations of the bowel. Such noninvasiveness of medical examination procedure also improves patients' comfort. The small-sized capsule that can be swallowed by an adult is a very complex system in which, a LED, a CMOS image sensor, a SoC and an antenna for wireless transmission are included. The average life time for the capsule is 8 h during which the capsule can travel through the intestine and then evacuate from the human body. The problem is that the evacuation time for various persons is quite different. For this reason we should extend the actual battery operation time with the SoC running inside the capsule to more than 16 h in order to cover a wide range of evacuation time. As a result various low power design techniques are necessary in the capsule SoC.

Another application in which low power SoC is needed is the digital hearing aid system. The purpose of the hearing aid is to amplify sound signal in order to compensate the hearing loss of patients. Compared to the conventional amplifier that provides constant gain for all frequency components, the hearing aid needs to provide different gain for signal in various frequency sub-bands. That's because sensitivity of human ears vary greatly with sound frequencies. Demands for digital hearing aids and other portable digital audio devices are becoming more and more challenging: On the one hand more computational performance is needed for new algorithms including noise reduction, improved speech intelligibility, beam forming, etc. On the other hand flexibility through programmability is needed to allow for product differentiation and longer lifetime of hardware designs. Both requirements have to be met by ultra-low power solutions being operated out of very small batteries. A hearing aid is a quite small device that can be worn behind the ear, fitting entirely in the outer ear or even put inside the canal. In such a small system, a microphone, an amplifier and an output transducer are required to perform sound signal acquisitions, sound amplification and playback, respectively. Recently, digital hearing aid dominates the market. The traditional amplifier is already replaced by the SoC with millions of transistors. The sound signal is firstly acquired and digitized and then processed by a digital signal processor. Sound is amplified in the digital domain. Other advanced functions can also be performed such as directional dependent amplification, echo cancellation and noise suppression or sound classification. Usually the Zinc-air battery is employed to power the whole system due to its relatively larger energy density with small size. However owing to the limit size, the energy capacity is still small. A size-10 battery can provide a current of 1 mA for a total 90 operation hours or 1.5 mA for 60 operation hours. Suppose an 8 h operation time per day, such energy storage is only available for less than two weeks. To prevent frequent battery replacement the SoC inside the hearing aid system must have ultra low power consumptions. Hence, new hearing aids are examples of ultra low power designs and technologies.

Even in energy metering applications, ultra-low power is desirable. First of all, the energy meter is always on. The power dissipated by the energy meter is the power wasted. To prevent tampering and maintain the real time clock (RTC), most energy meters have a battery. It is required that the meters can be in stand-by mode for more than 5 years. In the stand-by mode, some circuits such as the RTC and monitoring circuits have to be active. In certain anti-tampering applications, the meter needs to wake up periodically on the battery to detect or meter, thus ultra-low power is desired. Another requirement of ultra low power is the consideration of the power supply to the metering chip. Using potential transformers (PTs) have drawbacks such as being bulky, leaky, and poor reliability. Use a RC supply can overcome the problems associated with PT based supplies. However, for RC supplies, the smaller the capacitance, the better reliability and lower cost. With smaller capacitance, the RC supply cannot provide so much current, requiring ultra-low power metering chips.

In conclusion, due to its enabling potential for new markets and its importance for competitiveness, the further reduction of the electric power for SoCs and embedded systems has recently become one of the most challenging areas of research and development in this industry. In order to obtain the ultra-low power for these products, the different aspects of ultra-low power design for ASICs and embedded systems at all levels of abstractions from system level to circuit level and technology should be considered.

2 Design Challenges for Ultra-Low Power IC

Power consumption for ICs is as important as performance. The motivation for ultra-low power ICs is portability where battery operation life, increased functionality and heat generation are the key factors. The other application is huge server farms or large volume of devices such as energy metering in smart grids due to environmental awareness. Usually, the amount of energy stored in a battery is directly proportional to the battery weight and size. A battery for portable devices with limited weight and size can store limited amount energy. When a SoC is operated with a battery as a supply, the battery operation time operating the SoC is determined by the ratio of the energy stored in the battery to the average SoC power consumption. Since the battery can be seen as an ideal voltage source with constant output voltage, the power provided by the battery is then directly proportional to the current drawn by the SoC. In order to obtain longer battery operation time, the average SoC power consumption has to be reduced. In Fig. 1, we show a CMOS inverter as an example to explain power dissipation by digital circuits.

It is well known that for digital CMOS circuits, average dynamic current drain can be expressed as:

$$I = \alpha C_{load} V_{dd} f_{clk} \tag{1}$$

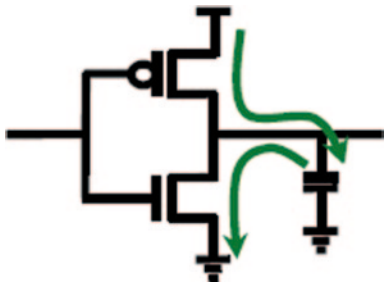

Fig. 1 Dynamic CMOS switching

In the above expressions, α represents the average activity factor of a digital system. C_{load} is the total effective load capacitance. V_{dd} is the supply voltage and f_{clk} represents the system operating frequency. Dynamic power consumes when the output of a gate changes states. Since not all the gates switch at the same time, the term α is introduced to model such effect.

It gives rise to the average dynamic power consumption as follows.

$$P = \alpha C_{load} V_{dd}^2 f_{clk} \tag{2}$$

In the above expressions, dynamic power consumption is quadratically dependent on supply voltage.

Clearly there are two ways for reducing dynamic power in CMOS digital circuits: (1) supply voltage reduction, and (2) activity reduction. Since power consumption depends quadratically on supply voltage, supply voltage reduction can give rise to substantial power saving. There are two schemes to employ supply voltage reduction without compromising performance: multiple power domains, and dynamic frequency and voltage scaling (DFVS).

To reduce the activity factor in CMOS digital circuits, there are three schemes to use for power consumption reduction: clock gating, power gating, or architectural exploration.

There is a design trade-off between chip frequency and voltage. Lowering the voltage will increase delay and reduce highest achievable operating frequency. The other thing we need to differentiate is power and energy. Energy is a time integral of power. With fixed energy, the power can be small with long activity time or the power can be large with short activity time. In the self-harvesting wireless sensing network for example, very small power from environment is harvested, conditioned and stored, the wireless transmitter can transmit data with high power of short period time. Usually the operation duty cycle for sensing wireless network will be less than 1 %.

Power consumption is difficult to estimate. It depends on number of elements, activity factor of each element, specific cells used (size, shape, technology etc.), manufacturing variance, operating temperature. The existing tools use measurements from previous designs, power models, or complicated formulae to estimate power consumption. It is a must to verify functional correctness of circuits that

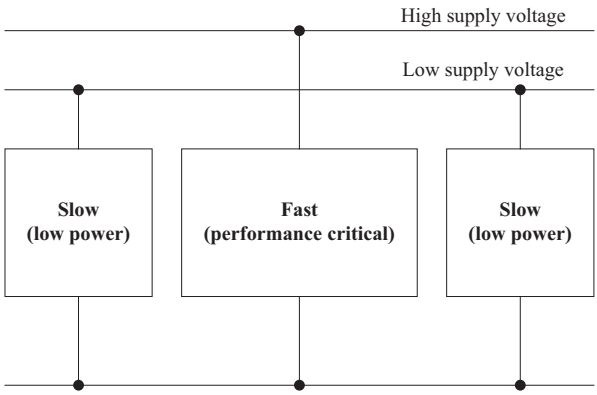

Fig. 2 Multiple power domains

employ low power design techniques. Currently, power saving techniques contain (1) multiple power domains; (2) dynamic frequency and voltage scaling; (3) clock gating; (4) power gating; (5) architectural exploration, etc. Such a multiple power domain is illustrated in the following figure.

In the scheme of multiple power domains as shown in Fig. 2, different blocks operate with different voltages and frequencies to achieve the optimized tradeoff between power and performance. Low power blocks can operate at lower voltage and slower frequency as long as performance meets the requirements. Higher supply voltage is used for performance critical logic, which runs at higher speeds, and consumes higher power. Multiple power domains have asynchronous interfaces for data and clock between power domains. It is necessary to model the data and clock correctly for function and performance verification. When a logic signal from the slow block with the lower supply voltage is connected to the fast block with the higher supply voltage, the signal level is closer to threshold voltage of the transistors, and can consume excessive leakage power and reduce noise margin. This scheme also requires additional power supply grid, and associated support such as decoupling capacitors, to ensure error-free operation.

In the scheme of dynamic frequency and voltage scaling (DFVS) method, power consumption reduction is achieved by dynamically controlling the voltage and the clock frequency. The digital chip is designed to deliver maximum performance at the highest supply voltage. The chip is operated at increased voltage when a higher performance is required. Otherwise, the chip is operated at a lower voltage with substantial power reduction when low power is demanded. On-chip power management circuitry dynamically controls the supply voltage and the clock frequency. The digital chip can detect the performance demand and adjust the clock frequency and the supply voltage accordingly. Special attention should be paid to guarantee that there is no effect on functionality when the supply voltage adjusts according to the tradeoff between power and performance. A well designed digital SoC detects peaks in performance demand, adjusts the supply voltage and clock frequency to deliver the necessary throughput only when needed, therefore considerable saving in power and energy can be achieved.

Table 1 Summary of low-power design techniques

Power-save technique	Benefit	Timing penalty	Area penalty
Clock gating	Medium	Little	Little
Multiple voltage domains	High	Some	Little
Dynamic frequency and voltage scaling (DFVS)	High	Some	Some
Power gating	Huge	Some	Some

In the scheme of the clock gating, effectively preventing the clock from ticking can save dynamic power. The clock signal to a digital block is gated by a control signal, inhibiting the clock when the digital block is not in use, therefore reducing the clock signal activity and the overall dynamic power consumption. The clock gating can be inside latches and on the clock distribution network. In most standard cell libraries, there are special purpose cells that perform the function with a bit cost of area. It is much more effective to reduce power if the same gating function is applied to large sets of registers or the clock distribution network. Approximation of gating functions enables gating more registers with the same function. For example, the register signal *c* is used to select signals *a* or *b*. Then signal *c* can be used as the gating function for *a* and *b*. there are tools to automatically apply gating at the netlist level. Hand crafted clock-gating can be more effective for experienced engineers. Since clock accounts for substantial activity in the digital block, the clock gating results in considerable power saving. The clock gating is reported to reduce power consumption by 20–60 %. This techniques is not limited to clock signals alone but can be used for other signals having high activity. One has to be careful, however, to ensure that the power consumed in the digital block to detect and disable clock gating is considerably lower than the power reduction achieved by the clock gating.

Power gating completely shuts off the power to parts of the design when they are not being used. The virtual power and ground grids need careful design to ensure that logic state is not lost when the virtual supplies collapse. A powered-off gates must not drive powered-on gates since powered-off flip-flops lose their states. They will have arbitrary values when they are turned on. It is necessary to copy the reserved state back when power is restored. In order to avoid the arbitrary values of flip-flops (X value), a power management is needed to control power-off and power-on sequences.

The highest potential for reducing power consumption is at the system architecture level. There are many factors involved such as system partitioning, bandwidth on buses, pipelining, redundancy, and performance-critical blocks, etc. System architects need to make tradeoff among power, cost, and performance. Unfortunately the current power estimation tools are not accurate, which make the process less reliable (Table 1).

In addition to dynamic power consumption, there is another category of power that is the leakage power. It is consumed by each element at all times. It grows exponentially when voltage is reduced as technology shrinks. It increases as transistor size shrinks. Until recently, leakage current was negligible. However, leakage power is now a substantial component of the total power for the advanced technology.

The supply voltage continues to decrease with each technology generation. In order to improve transistor and circuit performance per technology generation, the power supply V_{dd} and transistor threshold voltage V_{th} should reduce at the same rate. However, reduction in V_{th} causes transistor sub-threshold leakage current (I_{off}) to increase exponentially. Notice that in some condition almost half of the power consumption may be from sub-threshold leakage.

Dual or triple V_{th} design technique is widely used to reduce the sub-threshold leakage power. In this technique, the process technology provides two or three flavors of transistors: high threshold voltage (high V_{th}), standard threshold voltage (standard V_{th}), and low threshold voltage (low V_{th}). The high V_{th} transistors yield slower logic, but lower leakage, whereas low V_{th} transistors yield faster logic, but higher (~10X) leakage.

Here is the multiple V_{th} low power design methodology for a typical logic block using path delay distribution. If we use high V_{th} transistors everywhere, then it yields low leakage current, higher delay, or lower frequency. On the other hand, if we use low V_{th} transistors exclusively, then it yields higher frequency, but ~10X higher leakage power. A selective insertion of low V_{th} transistors for performance critical circuits yields higher frequency with lower leakage power.

Coming with nanometer-scale process technology and green-movement of consumer electronics, the methodology of low power-oriented design takes place in the cutting edge implementation needs. Multi-supply Multi-voltage (MSMV) design approach accommodates multiple power domains and multiple voltage levels, which makes ultra-low power chip design much more complicated than the design of a normal chip. The challenges that MSMV implementation design needs to overcome in advanced process nodes: timing, power, design for testing (DFT), design for manufacture (DFM), design for yield (DFY), etc. MSMV scheme of ultra low power solution has the following features: multiple power domains inside, multiple power supplies for chip core cell, multi-V_{th} optimization, level shifter, isolation cell, retention cell, power gating cell, etc.

MSMV solution meets the most up-to-date demand of ultra low power for consumer electronics, such as: mobile internet device, smart phone, GPS, personal media player, other mobile/handheld devices, energy harvesting devices, etc. Comparing two similar SoCs with only one difference, one with MSMV design and the other without it, the power consumption of the SoC with MSMV could be greatly reduced to one-fiftieth (1/50) maximum of the one without MSMV in leakage power. As for dynamic power, it saves up to 70% power consumption in average under normal operation conditions.

The progress of the CMOS technology allows capacitance and supply voltage shrinking down aggressively. For 65 nm general purpose technology, the supply voltage is only 1 V. According to the prediction of ITRS, in 2020, the supply will lower down to only 0.6 V. Although the dynamic power dissipation shown above gets smaller along with the supply voltage, in some specific applications such as endoscopy capsule, digital hearing aids, wireless sensor network nodes, the power consumption is still not very small due to complex functionalities which SoCs perform. Various low power techniques on circuits design are still needed. As we

discussed before, attractive techniques available are power gating, clock gating, multi-voltage/multi-frequency, and parallel processing, but exploring those techniques greatly increases the design effort. Thus new design methods, verification methods are sorely needed. In CMOS design, the leakage power that was assumed to be negligible is becoming more and more significant. The reason for that is that threshold voltage shrinks down much more slowly than that of supply voltage. So the transistors in CMOS logic cannot be completely turned off in the sub-threshold region. As a result the leakage current of a transistor increases drastically. Employing low power technology can greatly reduce the leakage at the cost of transistor performance degradation. Another significant source is the gate leakage current in nano-meter devices. The assumption that the MOS gate is high impedance is not accurate as the device geometry further shrinks.

Analog building blocks such as front-end programmable amplifier, analog-to-digital converter (ADC), bandgap reference, clock generator and low-drop out voltage regulator are necessary in most SoCs. Different analog and RF circuits have different design challenge due to their inherently different architectures. Although progressing of the CMOS technology brings benefits such as performance enhancement and power reduction to the digital design, analog and RF circuits design gets more difficult. Firstly the supply voltage drops while noise does not (more often the noise increases) and hence the dynamic range of analog signal reduces. The voltage headroom is also limited by the supply and swing gets smaller which results into significant distortion problems besides the degradation of signal-to-noise ratio (SNR). Employing operational amplifier and feedback is a popular method to obtain high precision signal conditioning. However, with a low supply voltage, cascode technique is no longer suitable. If cascade is used to increase the gain, more branches between power and ground are needed. More power consumption is required to push poles far away in order that the amplifier is stable in feedback configurations. Another problem associated with SoC is the noise generated by the switching of digital circuits. It can reduce the SNR of the analog circuits significantly. There is no universal way to reduce the power dissipation of analog and RF circuits. Sometimes the figure of merit (FOM) is used to quantify the SNR performance vs. bandwidth vs. power dissipation. In actual industrial designs, optimization is generally towards the whole system instead of merely looking at the FOM of a single block. Also looking at the FOM of a single block can be misleading if the driving circuits and to be driven circuits are not considered.

In this book, ultra low power design techniques are discussed and actual examples of industrial design are introduced. In Chap. 2 the interface to the real world is presented. An important conclusion from this chapter is that analog signal from a sensing network is usually weak and noisy. It needs to be processed before it can be used. Chapter 3 describe low noise low power amplifier. After flicker noise and thermal noise are introduced, the techniques to cancel offset and low frequency noise are presented. Noise reduction-related design examples are given at the end of this chapter. Chapter 4 gives an in-depth view of ultra-low power design principles for both ADC and DAC. Several ultra-low power design examples of ADC and DAC are also presented in the chapter. In Chap. 5, we introduce the ultra-low power

digital circuit design. Sources of power dissipation in CMOS circuits are analyzed. The basic low power design methodologies are given. Application specific instruction-set processors (ASIP) are introduced and optimized for ultra low power audio application. The compromise between power and performance is explored. Chapter 6 discusses ultra-low power transceiver design. After general techniques for ultra-low power transceivers are described, several examples of transceiver designs are given. In the following chapters, real industrial design examples are presented. In Chap. 7, an ultra-low power energy metering chip is presented with the focus on both analog and digital circuit design. Chapter 8 presents an energy metering SoC that explores the system level power optimization as well as circuits-level optimization. Chapter 9 presents an ultra-low power hearing aids SoC and Chap. 10 presents an SoC for capsule endoscope. Both SoCs employ extensively ultra-low power techniques discussed in this book.

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