

Preface

Surveillance systems are important technological tools that enable monitoring environments of interest and detecting potential malicious activities. In a world of increasing crime rates, wars, terrorism attacks, and security breaches, video surveillance is a natural solution for avoidance, detection, and hopefully prevention. Surveillance is ubiquitous, touching a wide range of fields: military, homeland security, public and commercial safety, law enforcement, environmental studies, building preservation, smart rooms, and personal safety at home. Typical surveillance systems consist of multiple spatially distributed cameras that continuously monitor a scene and transmit the collected data to a central room for further activity analysis and visualization. To provide reliable monitoring, current systems rely on robust image processing algorithms distributed across several layers of the network. The basic image processing steps involved are image registration, image fusion, object detection, object tracking, object classification, and activity analysis.

With the advances in imaging, IC manufacturing, and wireless technology, tiny visual sensor nodes are employed to collectively monitor areas of interest. These sensor platforms are defined with low complexity, great mobility, and low power consumption. They are capable of capturing and processing images and intelligently sending just the right amount of data to the control room for further processing. The core components, image registration and fusion as well as object detection and tracking algorithms, are now performed at the camera ends and activity interpretation in the control room. There is more stress, in this case, on the accuracy of the first four steps, so the information sent to the central station is accurate and sufficient to make further decisions. Distributing the processing across various resource-constrained sensor platforms is a challenge yet to be solved. The limited memory, processing capabilities, and power resources of these nodes impose constraints on the complexity and memory requirements of the running algorithms. Target algorithms must be lightweight, with low memory requirements to fit on these nodes while providing robust, accurate, and real-time results. On one hand, continuous research is needed to enhance the efficiency of registration, fusion, detection, and tracking algorithms, to become fully automated and reliable for surveillance purposes. On the other hand and more importantly, intelligent but

lightweight surveillance algorithms should be developed to fully benefit from the features offered by embedded platforms.

This book distinguishes itself by investigating a new paradigm for resource-aware surveillance on visual nodes. Typical surveillance books address the underlying image processing steps from a standard system point of view. A great attention has been given to finding new algorithms, enhancing accuracy, or speeding up existing approaches. With the emergence of multi-sensor surveillance systems, several visual platforms have been proposed, but only basic image processing algorithms were implemented. There is a lack of algorithms aware of the resource-constrained nature of the distributed surveillance platforms. This book addresses these steps from a whole new perspective. It investigates a different type of image processing algorithm and architecture required for such visual sensor nodes. This means a shift from traditional algorithms developed for massive computers to algorithms intended for constrained video preprocessors (low complexity, low memory requirements, and low power).

“Video surveillance using visual nodes: algorithms and architectures” provides a comprehensive study of the different local image processing steps in embedded surveillance. The book tackles the core image processing steps from the resource-constrained application point of view, along with hardware alternatives, simulations, and experimental results. It features the following:

1. An overview of surveillance systems and visual sensor networks: The book surveys overall design considerations, platforms, applications, and research trends. It also identifies practical issues, real-life challenges, as well as potential solutions and recommendations. This is beneficial for both readers interested in these topics and researchers in the field. It helps them gain an in-depth understanding about these topics, state of the art technologies, and future research directions.
2. Novel practical resource-aware image processing algorithms: A set of lightweight and efficient algorithms for image decomposition, registration, fusion, object detection, and tracking are developed. These are proposed for visual nodes in lieu of existing traditional techniques intended for massive computers.
3. Optimized hardware assist architectures: Memory-efficient and high-speed hardware architectures for critical components are developed in conjunction with the optimized algorithms mentioned above. The hardware assistance helps mitigate the burden on the node processor and achieve high-speed and real-time operation.
4. Simulation and experimental results: Developed algorithms and hardware architectures are evaluated and tested using real-life data sequences. Qualitative and quantitative results demonstrate the advantages of these works over traditional massive schemes.

With video surveillance receiving much attention from the academic community, industry, and governments, this book is valuable to a wide range of readers. This includes industry experts, researchers, graduate students, and professors. “Video surveillance using visual nodes: algorithms and architectures” serves as

an all-inclusive unprecedented reference to various theoretical concepts about surveillance systems, visual sensor nodes, and local visual processing on-board taking into account the practical limitations of visual sensor nodes. It introduces readers to a new type of image processing algorithm and hardware architecture suited for low-power and low-memory visual sensor networks of mobile platforms. Moreover, it provides real implementations, simulations, and experimentations demonstrating the improvements achieved with the developed algorithms and hardware architectures.

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Mayssaa Al Najjar
Milad Gbantous
Magdy Bayoumi

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Al Najjar, M.; Ghantous, M.; Bayoumi, M.

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