Preface

Energy efficiency is a widely acknowledged design objective in electronic systems research and development. With continued technology scaling reliability is an emerging concern in these systems due to increased device-level vulnerability in the presence of electromagnetic inductions and process variability. Achieving high reliability and energy efficiency objectives jointly can, however, be challenging as energy minimization techniques exacerbate the reliability further. Hence, energy-efficient fault-tolerant (i.e. reliable) design is currently of high interest to both industry and academia to address these challenges effectively. The aim of this book is to introduce state-of-the-art and emerging issues in energy-efficient fault-tolerant design techniques as applied or prototyped for current or future generations of system-on-chip (SoC). Although necessary brief background has been provided in each chapter, fundamental theories have been omitted or avoided. The reader is expected to have preliminary background of electronic circuits and systems design and synthesis.

The book consists of nine chapters; five chapters (Chaps. 1–5) are dedicated towards systems modeling and design techniques, while four other chapters (Chaps. 6–9) delve into emerging systems architectures and design challenges. The individual chapter outlines are given below.

Chapter 1 (Introduction to Energy-Efficient Fault-Tolerant Systems) provides the necessary background relevant to this book. Low-power design aspects are briefly revisited, and concepts related to faults and reliability are reviewed. Underpinning these basics, challenges of energy-efficient fault-tolerant systems design are highlighted showing various techniques.

Chapter 2 (Reliability Evaluation Techniques) gives a comprehensive review of the reliability models. In particular, methods for evaluating system reliability with stochastic modeling and other combinatorial methods are discussed in details.

Chapter 3 (Energy-Efficient Design Techniques) presents an overview of power minimization and power management techniques. The impact of energy-efficient design techniques on the system reliability is also investigated. Extensive case studies are presented addressing energy-efficient fault-tolerant design techniques.

Chapter 4 (Error Correction Coding for Electronic Circuits) discusses various existing and emerging error detection and correction (EDAC) codes mainly used in sequential circuits. Implementation and suitability of various EDAC codes are detailed with examples, followed by their analyses in terms of fault detection and tolerance capabilities, overheads, and circuit complexities.

Chapter 5 (System-Level Design Methodology) introduces system-level design methodology, particularly suitable for multiprocessor system-on-chip (MPSoC). Various MPSoC design challenges are discussed, highlighting ways to effectively address them using system-level design methodology. Later, an extensive system-level design optimization case study is presented investigating into the impact of application task mapping on MPSoC applications.

Chapter 6 (Fault-Tolerant Reconfigurable On-Chip Network) presents fault-tolerant reconfigurable on-chip networks, which are infrastructure communication architectures for future computing platforms. The impact of workload variations on the fault-tolerance of reconfigurable on-chip network is also studied in details through a number of case studies.

Chapter 7 (Bio-Inspired Online Fault Detection in NoC Interconnect) deals with bio-inspired online and low-cost fault detection capabilities for emerging scalable network-on-chip-based multiprocessor systems. In particular, a novel real-time strategy for detecting faults in NoC interconnect is demonstrated that uses biological synapses and neurons to detect temporal and spatial faults effectively. Analysis of different fault scenarios and results from real-time experiments on an example FPGA implementation are also provided.

Chapters 8 (Power-Efficient Fault-Tolerant Finite Field Multiplier) and 9 (Low-Cost C-Testable Finite Field Multiplier Architectures) investigate into emerging low-complexity techniques for secure and fault-tolerant hardware design. To solve the problem of an attacker injecting faults into the hardware and then analyzing the incorrect outputs, different detection and correction mechanism are studied in detail. The aim is to ensure that the effect of injected errors is not visible at the outputs for the attacker to be able to intercept and compromise the security and fault-tolerance of the system. Moreover, new methods for secure error detection and correction using various type of codes are investigated for scan-based attacks during testing.

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