Chapter 2
Cognitive Radio Architectures

2.1 Introduction

The system architecture for the SDR analog/RF is significantly different from that of traditional narrowband radio systems. In the original software radio proposal by Joseph Mitola in 1992 [8], he proposed an architecture where in the receiver,the RF bandwidth is digitized (no down-conversion), and signal analysis and demodulation is performed in the digital domain. Similarly, in the transmitter, the RF signal is synthesized in the digital domain, converted to analog and transmitted. The conceptual transceiver architecture is shown in Fig. 2.1. The Mitola architecture provides the maximum amount of flexibility through an increase in software capability. However, this architecture imposes impractical requirements on the analog-to-digital and digital-to-analog converters necessary for this architecture. For example, as discussed in [9], a 12 GHz, 12-bit ADC that might be used in a Mitola receiver would dissipate 500W of power! As a result, the ideal goal of communication at any desirable frequency, bandwidth, modulation and data rate by simply invoking the appropriate software remains far from realizable.

A number of SDR[1] architectures for cognitive radios currently being pursued provide only a subset of the functionality of the original software radio proposal. Specifically, in a practical interpretation, a large number of features of the waveform are defined in software, while the SDR hardware provides re-configurability to alter the waveform within certain bounds defined by the actual system. This reconfigurability is commonly expected to encompass at least multiple radio access technologies (RAT) using a single transceiver IC over a wide frequency bandwidth [10]. However, in this book, we will focus on a much broader scope of cognitive radios that does not limit itself only to multi-standard, multi-band communications.

In order to co-exist with currently employed transceivers without causing them harmful interference, the SDR often needs to incorporate the most stringent

[1] Note that a software-defined radio (SDR) is not the same as a software radio as prosposed by J. Mitola which relies on RF digitization. In this book, we reserve the term SDR for all radio architectures that provide adequate flexibility for cognitive radio functionality.

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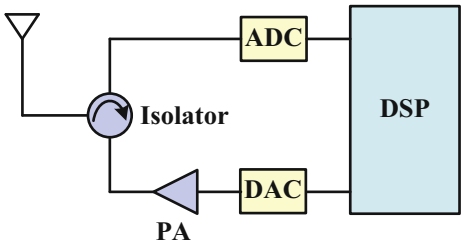

Fig. 2.1 Functionality of an envisioned software radio by J. Mitola [8]

specifications among all the radio access technologies being employed in the frequency range of interest.

For cognitive radio functionality, the SDR architecture can be considered a combination of a spectrum signaling transceiver system, and a sensing receiver system. Architecture options for these two systems are discussed below.

2.2 Signaling

For purposes of signaling, the SDR is essentially narrowband. As observed in [9], for most civilian applications of cognitive radios, only a particular narrow band of RF frequencies are of interest at a particular time for transmission of the message signal. However, this narrow frequency band may occur anywhere along the entire bandwidth of operation of the SDR. In order to cover the entire range, multiple receiver front-ends may be used, each dedicated to its narrow band of operation [11, 12]. However, it is easy to see that such an approach is power and area inefficient. Instead, it is desirable to use a wide-tuning range frequency synthesizer in conjunction with a wideband/wide-tuning[2] front-end for covering the frequency range as shown for a receiver in Fig. 2.2. The number of such front-ends required will only be equal to the maximum number of non-contiguous frequency channels to be simultaneously used (typically assumed to be a single channel at present).

2.2.1 Receiver

An example wide-tuning receiver architecture is shown in Fig. 2.2. Each component in this architecture is discussed below.

RF Bandpass Filters For the receiver architecture, co-existence with employed technologies necessitates the use of RF bandpass filters. As shown in Fig. 2.2, these

[2] In this book we make the following distinction between wideband and wide-tuning circuits. We use the term wideband for circuits that work over a large instantaneous bandwidth in RF. Wide-tuning circuits, on the other hand, function over a narrow instantaneous bandwidth, but can be tuned over a large frequency range.

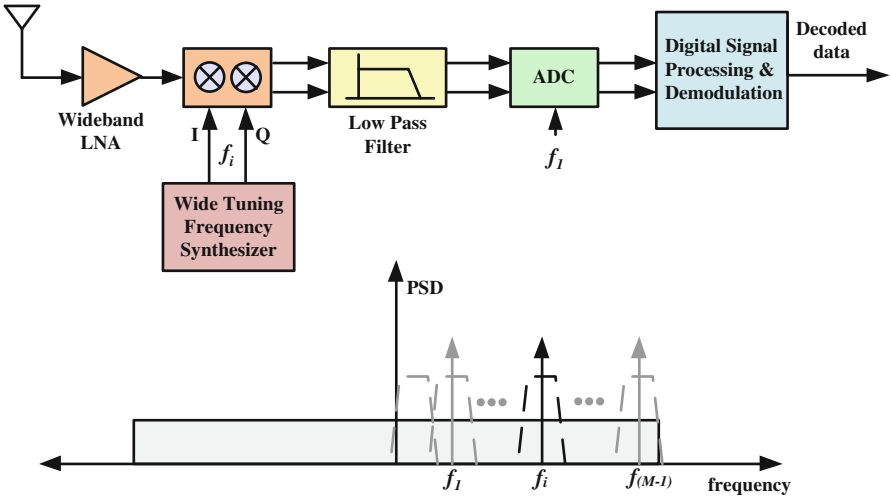

Fig. 2.2 A narrowband, wide-tuning signaling/scanning approach for signal reception and decoding

filters precede the LNA, and therefore their insertion loss directly compromises the receiver noise figure. Also, in order to remove large out-of-band blockers typical in the RF environment, high quality factors are mandated. Consequently, traditional RF architectures commonly use off-chip surface acoustic wave (SAW) filters to fulfill the front-end filtering requirements.

Unfortunately, SAW filters do not offer frequency tuning, and therefore, are not suitable for the SDR signaling architecture desired. As a result, the RF front-end filter is an important criteria for the realization of efficient SDRs. There has been significant research on tunable RF bandpass filters in recent years. A number of MEMS-based tunable filters, based on switched capacitors, have been developed [13–17]. A variety of varactors have also been utilized to realize frequency tuning [18–20].

More recently, driven by the vision of complete integration, a number of on-chip tuned filters are being developed. After initially working with the idea of on-chip switched capacitor LC filters [21], these filters have more recently been based on a revived idea originally published in 1960 [22] called the N-path filter. Recent work on this concept, using frequency-translation of complex impedances to a local oscillator frequency, is promising [23–27].

LNA Traditionally, LNAs have been designed as narrow-band solutions to attain a required performance over a small bandwidth. For the purpose of signaling in SDRs, these architectures need to be extended to one of three possibilities:

1. *Multiple narrowband LNAs in parallel:* As discussed already, this is a wasteful idea in terms of area; moreover, it requires the implementation of RF switches that are challenging to design, and increase parasitics in the RF path.
2. *A wideband LNA:* Wideband LNAs can be designed either by preceding a narrowband design with a wideband LC-ladder filter [28, 29], or using broadband

architectures [30]. The former uses multiple inductors using up valuable real-estate. The latter use MOS transistors and resistors (broadband elements) but typically suffer from a noise figure higher than 5 dB when power matched at the input. Such a high noise figure does not satisfy the stringent requirements of an SDR. Using global feedback improves the noise figure, but at the expense of stability [31]. Noise canceling schemes have been proposed to improve the noise figure below 2.5 dB for wideband architectures [9, 32], and are a promising candidate for SDRs.

However, wideband architectures provide little suppression for out-of-band blockers. Consequently, their broad input bandwidth increases the linearity requirements significantly.

3. *A wide-tuning narrowband LNA:* For signaling purposes, narrowband LNAs that are tunable are the preferred option. They not only provide suppression for out-of-band blockers but are expected to provide a lower noise figure (< 2 dB) compared to their broadband counterparts. However, tuned LNAs have so far either provided multi-band (discrete frequency switching) operation [33, 34] or low tuning range (e.g.: 23 % in [35]). For wider tuning range, switched inductors [36] may be utilized.

Frequency Synthesizer A wide-tuning range frequency synthesizer is a critical building block for the signaling receiver [37]. The following requirements can be identified for the synthesizer:

- Wide-tuning range, at least in excess of 67 % (f to $2 \times f$) such that lower frequencies can be obtained by integer division
- Low phase noise, such that the phase noise skirts do not cause down-conversion of spurious signals onto the desired signal (reciprocal mixing)
- Fast-settling behavior, to enable fast band-switching in the SDR
- Fine-frequency resolution determined by the minimum channel spacing desired

The first two requirements stem from the limitations in the voltage controlled oscillator (VCO). Unfortunately, these two performance features of VCOs: phase noise, and tuning range, strongly trade-off with one another. On-chip VCOs are based on two popular architectures: LC tank based, and ring based. Of these, LC tank VCOs are traditionally well suited for low phase noise applications, but suffer from a low tuning range. On the contrary, ring oscillators provide a wide tuning range, but suffer from poor phase noise. Consequently, there has been a significant effort toward realizing wide-tuning range LC VCOs for SDR applications.

Varactor based tuning typically provides 10–15 % tuning range [38, 39]. Use of switched capacitors in conjunction with varactors can provide a larger tuning range, but is still limited to about 50 % [40, 41]. Figure 2.3 shows the frequency tuning range and center frequency of published LC VCOs in the last decade. As seen, only one VCO (out of about 100) covers the tuning range required (66.67 %) to obtain all lower frequencies by division. Moreover, the tuning range requirements are made more challenging by PVT variation.

In Chap. 3, a new technique for obtaining a very wide-tuning range (up to 160 %) in LC VCOs while providing low phase noise throughout the tuning range is discussed.

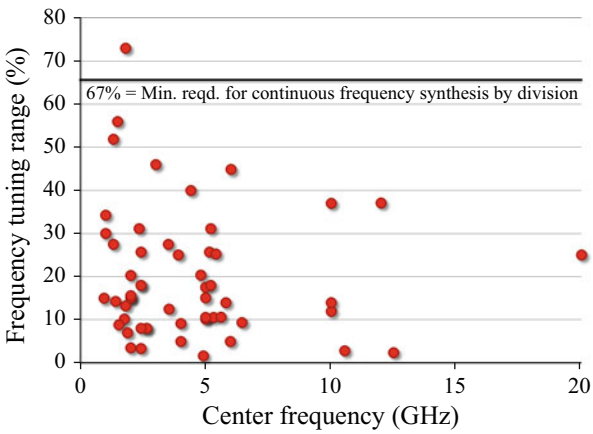

Fig. 2.3 A survey of frequency tuning range of LC VCOs published in IEEE journals and conference proceedings appearing between 1992 and 2010

The oscillators described are based on switched inductors, and provide a viable option for the SDR signaling architecture.

Mixers For complete on-chip solutions, homodyne architectures have been the preferred choice. Homodyne architectures ease the requirements on the IF filter; however, they suffer from a number of issues including flicker noise, dc offsets, and second order non-linearity in circuits[3]. A high-pass filter may be used to filter out the low frequency components; however, this contributes to information loss and is not the preferred solution for very narrow-band architectures (e.g. GSM). Consequently, homodyne architectures have gained popularity for moderate to wide bandwidths, especially in SDR applications. Due to their lower flicker noise and excellent linearity, passive mixers have often been the preferred choice for SDR applications [9, 42].

Considering that a tuned RF filter does not provide as effective out-of-band rejection as fixed RF filters, and that SDR applications often require more stringent out-of-band rejection specifications [42], harmonic reject mixers become critical. To understand the problem of harmonics, consider the scenario shown in Fig. 2.4a. Despite the use of a variable bandwidth, band-select filter, large out-of-band blockers are not sufficiently suppressed. Subsequent mixing with a square wave (most mixers perform hard-switching) down-converts the desired signal, but also the interferers around the LO harmonics as shown in Fig. 2.4b. Consequently, the IF (zero-IF in this case) signal is significantly corrupted as shown in Fig. 2.4c.

To alleviate the problem of harmonic mixing, multi-phase harmonic rejection mixers can be employed [26]. Such mixers have been employed in a number of SDR architectures [9, 42], providing 30–40 dB harmonic rejection. Further harmonic rejection can be obtained using digital correction [42].

In addition, mixer first architectures [43], and a linear LNTA followed by a passive mixer [42] architectures have gained popularity due to their improved linearity and subsequent capacity to handle large out-of-band interference.

[3] In case a single mixer is used, it also suffers from LO pulling, LO re-radiation, reciprocal mixing, etc. However, using a multi-step down-conversion mitigates these effects.

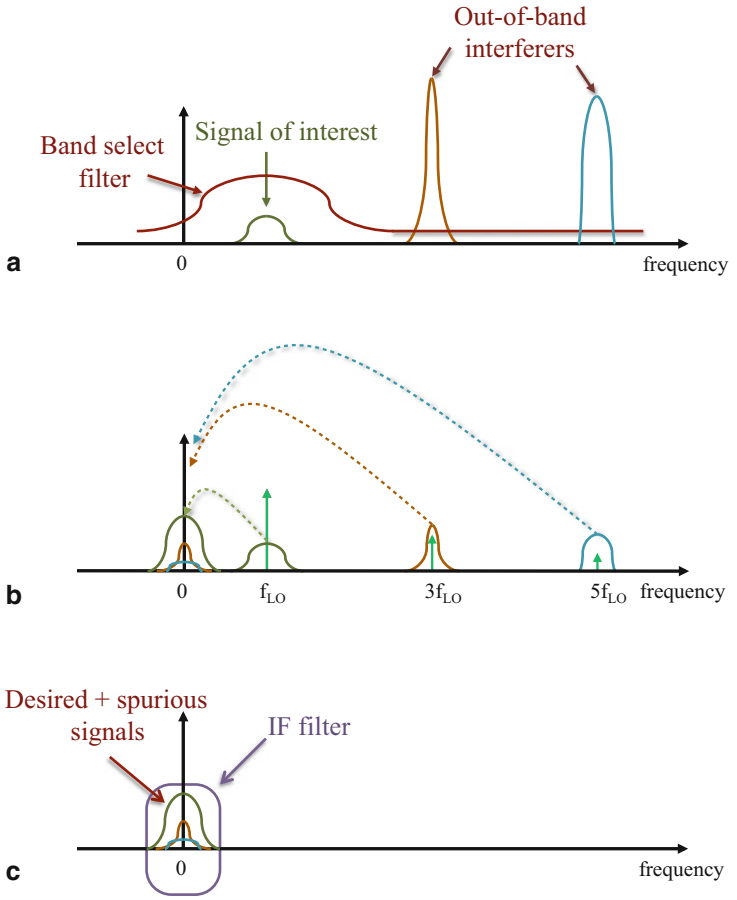

Fig. 2.4 The problem of harmonic down-conversion in a receiver

Baseband Filters Prior to digitization by an ADC, a variable bandwidth analog baseband filter is required to attenuate interferers to reduce the ADC dynamic range. Additionally, the baseband filter acts as a variable pole anti-aliasing filter (AAF) prior to sampling. Various techniques can be used to implement the baseband filter, broadly classified into continuous time and discrete time varieties. Continuous time filters have the advantage of not suffering from aliasing issues, but typically have poorer accuracy due to matching limitations. These filters can be realized using op-amps or using Gm-C filters [44–46]. Programmability can be achieved by switching resistors and capacitors, or by tuning these elements. However, the accuracy of these filters in sub-micron processes, and their lack of easy programmability have made way for active research in discrete time variations for SDR applications.

Discrete-time baseband filters are based on switched capacitors and can be implemented with or without active elements [9, 47–50]. The ease of programmability in these filters arises from the dependence of the filter notches on the clock frequency

which can be tuned easily. Note that discrete-time filters require an anti-aliasing pre-filter that may be constructed using a combination of mixer output poles, current domain sampling, etc.

Analog to Digital Converter (ADC) ADCs for signaling applications typically require a high dynamic range to accommodate a variety of access technologies, and the remaining in-band blockers. Additionally, a relatively large (tens of MHz) bandwidth is required to accommodate wide-band access technologies.

For high dynamic range applications, $\Sigma - \Delta$ ADCs [51] have been the popular choice. $\Sigma - \Delta$ converters are based on $\Sigma - \Delta$ modulators that perform noise shaping on an oversampled signal using negative feedback techniques. The feedback loop suppresses the non-idealities in the quantizer, improving the effective resolution despite the use of a lower resolution quantizer. The shaped noise is filtered in the digital domain to obtain the ADC bits; as a result of the large amount of digital processing involved in the $\Sigma - \Delta$ ADC, these converters scale well with technology. Typically, $\Sigma - \Delta$ converters have been bandwidth limited due to quantizer latency, and parasitic poles, and sampling speeds have been limited to 1 GHz for 70 dB dynamic range. This results in bandwidths in the tens of MHz. However, in recent years, wideband $\Sigma - \Delta$ architectures that provide both the high dynamic range of $\Sigma - \Delta$ ADCs, as well as wideband digitization have been explored [52, 53]. These circumvent the speed limitations to provide signal bandwidths above 100 MHz alongside a high (> 70 dB) dynamic range.

For obtaining even larger bandwidths (usually at the expense of dynamic range), Nyquist ADCs are the more popular choice. Pipeline ADCs are the most popular choice for increasing the input bandwidth (> 200 MHz with 14–16 bit resolution) [54, 55]. For increasing the dynamic range, calibration techniques are popularly used [56]. However, the use of high-gain, wideband amplifiers and complex calibration techniques increase their power consumption, area, and design complexity.

Recently, successive approximation register (SAR) Nyquist ADCs have been used for moderate dynamic range (8–11 bit) at moderate speeds (< 100 MHz). SAR ADCs provide the advantage of very high power efficiency (low FOM) as they use just a single comparator for comparison [57–59]. However, they use N steps for providing an N-bit resolution, limiting their inherent speed. To overcome the speed limitation, time-interleaving is popularly used with the SAR architecture. Additionally, the SAR ADC resolution is limited by gain, offset, timing errors, and capacitor matching, and calibration techniques can be used for overcoming these [60].

A plot of the dynamic range and bandwidth of published ADCs [61] is shown in Fig. 2.5.

2.2.2 Transmitter

A generic transmitter architecture for SDR signaling applications is shown in Fig. 2.6. The critical blocks in this architecture comprise a wide-tuning frequency synthesizer, similar to one discussed in Sect. 2.2.1, a wideband mixer, similar to one discussed in

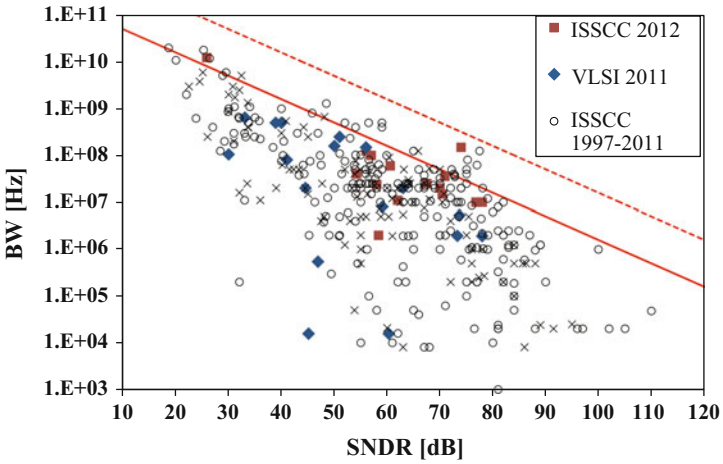

Fig. 2.5 A survey of ADCs from 1997–2012 [61]

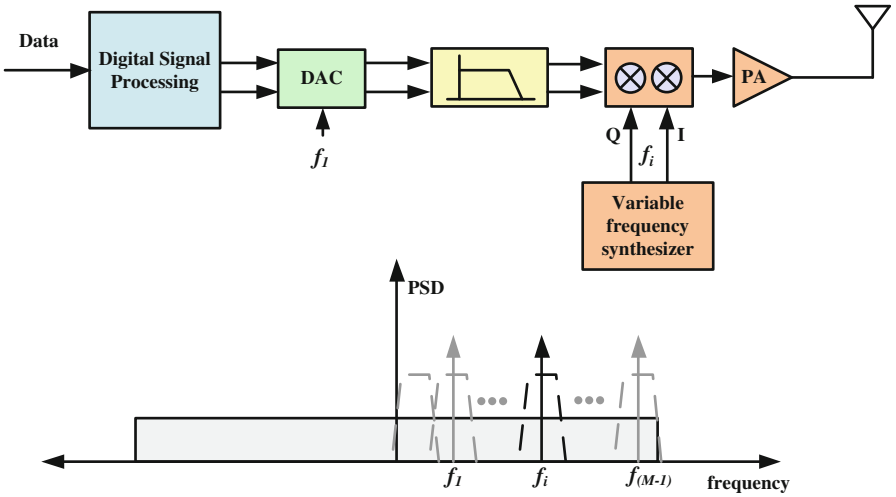

Fig. 2.6 A narrowband, wide-tuning approach for signal transmission

Sect. 2.2.1, and a wideband, linear power amplifier (PA). Linearization techniques for wideband SDR architectures are discussed in [62]. Harmonic mixing [26] may be used; moreover, the mixer and power amplifier may be combined to obtain a linear power mixer [63].

2.3 Spectrum Sensing

Spectrum intelligence or knowledge about the spectral and spatial electromagnetic spectrum around us is of critical importance for dynamic spectrum access in cognitive radios. One of the primary bottlenecks in implementing dynamic spectrum

access is reliably detecting primary users before deciding on the frequency, channel, access and modulation formats of transmission for the secondary user. The problem of primary user detection is further complicated by multi-path fading and hidden node/shadowing effects [4]. Some of these problems can be mitigated somewhat by using cooperative techniques across multiple sensors [64]. However, the issue of identifying primary user activity with varying modulation formats and signal power levels, over a wide swathe of spectrum, using limited power continues to confound the industry.

From an SNR perspective, the optimal method for signal detection is a matched filter. However, such a coherent detection technique requires *a priori* knowledge of the primary user signals and modulation formats. Worse still, a cognitive radio based on coherent detection with matched filters would require a dedicated radio for each primary user class. One method to address this problem is to employ a blind, non-coherent detection scheme using energy detection. Despite the implementation simplicity of this approach, non-coherent energy detection schemes require a large number of samples $[O(1/SNR^2)]$ and therefore, a longer sensing time. Moreover, such a scheme would be unable to distinguish noise and in-band interference from primary user signals, or work for spread spectrum signals (direct sequence and frequency hopped). An intermediate approach would be to use feature detectors which rely on some knowledge (or feature) of the primary user. Cyclostationary feature detectors rely on detecting the built-in periodicity of modulated signals such as their carrier frequency, bit rate, repeated spreading, pulse strains, hopping sequences, and pilots. Moreover, even in the absence of clock timing or phase knowledge, cyclostationary feature detectors obtain considerable improvement in detection performance [65]. A brief description of the spectral correlation function on which cyclostationary feature detectors are based is provided in Appendix A.

Spectrum Sensing Architectures There are two fundamentally distinct options for realizing a spectrum sensing receiver for an SDR front-end: a scanner type, and a wide instantaneous bandwidth digitizer type.

1. Scanner: In this scheme, a narrowband, wide-tuning receiver scans and digitizes the entire bandwidth (similar to a spectrum analyzer) progressively for digital analysis. The digital signal processing backend processes each digitized band sequentially and stitches the frequency domain outputs to obtain a spectral map of the environment. The architecture used for this scheme is very similar to that used in the signaling receiver discussed above (Fig. 2.2). However, in order to overcome practical wireless communications issues such as multi-path, fading, hidden nodes, interference problems in the context of an unknown signal, etc [4, 66], the sensitivity and dynamic range requirements of the architecture are more challenging than the signaling scheme. Moreover, note that sensing may be a blind detection problem, as opposed to signaling where *a priori* knowledge of the transmitted signal is available.
   Although the scanning architecture is able to re-use much of the signaling architecture (or vice versa), this detection technique suffers from multiple short-comings. These systems lack the agility required to be able to detect any fast-hopping

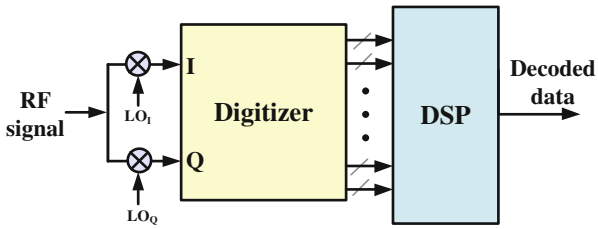

Fig. 2.7 A wideband RF to digital conversion architecture for spectrum sensing

signals. Frequency domain stitching in the digital domain is power hungry due to the phase distortion of the analog filters that select each digitized sub-band. Moreover, stitching the frequency domain information from multiple scans is imperfect in the face of multi-path; consequently, signals spanning multiple scan bandwidths are imperfectly reconstructed. Due to these and other reasons, it is desirable to construct a real-time instantaneous bandwidth digitizer (similar to J. Mitola's original software radio idea) as part of the spectrum sensor.

2. Wide instantaneous band digitizer: Unlike the scanning type architecture, a wide instantaneous band digitizer digitizes the entire wide RF bandwidth instantly, and performs the digitization in a real-time. Understandably, the wideband digitizer has widely been considered as one of the bottlenecks to the realization of an SDR based cognitive radio. A significant number of efforts in recent years have focused on parts of this larger issue by addressing wider bandwidths, broadband matching, higher front-end linearity, and most importantly, wideband analog to digital converters.

   Several architectures have been proposed for the RF front-end. Of these, the most popular is the generalization of the Mitola receiver architecture as shown in Fig. 2.7 effectively performing an RF to digital conversion (R-to-D). Typically, the front-end requires a wideband low noise amplifier prior to the RF digitizer. Moreover this front-end needs to handle a large dynamic range due to the large peak to average power ratio (PAPR) of broadband signals. The increase in the PAPR for larger bandwidths is depicted in Fig. 2.8. As shown in the specific example, the PAPR for the narrowband signals is only 2, while that for a wideband signal (5 times the bandwidth) with multiple signals, all having similar powers, is 10. In this case, the PAPR grows linearly with an increase in bandwidth. As a result of this increased PAPR of the wideband inputs, a very linear RF front-end is necessitated. The linearity requirements of the LNA have been addressed in [67–69]. Another approach comprising a low noise transconductance amplifier (LNTA) followed by mixers is discussed in [42]. Moreover, passive mixer first topologies have also been proposed for high IIP_3 performance [43].

   The digitizer block shown in the figure is essentially an equivalent ADC with performance specifications beyond that achievable using state-of-the-art converters discussed in Sect. 2.2.1. This wideband digitizer can be implemented using multiple techniques, all based on some form of multiplexing in order to ease the requirements on the ADCs. A time-multiplexed wideband approach using time-interleaving as shown in Fig. 2.9 was proposed in [70]. This scheme reduces the

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