

# Preface

This book is motivated by the challenges faced in designing a high speed low power on-chip communication framework in modern digital ICs. As VLSI fabrication technology scales, an increasing number of processing elements (cores) on a chip makes on-chip communication a new performance bottleneck. The Network-on-Chip (NoC) paradigm has emerged as an efficient and scalable infrastructure to handle the communication needs for such multi-core systems. In most existing NoCs, design decisions are made assuming that the NoC operates at the same or lower clock speed as the cores, which slows down the communication system. Since the NoC connects the cores across the entire chip, it becomes difficult to operate the NoC at a high frequency. Another major challenge in designing a high speed NoC is the difficulty of distributing a high speed, low power clock across the chip.

This book consists of three parts. In the first part, we propose several techniques to address the issue of distributing a high-speed, low power, low jitter clock across the IC. We primarily focus our attention on resonant standing wave oscillators (SWOs), which have recently emerged as a promising technique for high-speed, low power clock generation. In addition, we also present a dynamic programming based approach to synthesize a low jitter, low power buffered H-tree for clock distribution.

In the second part of this book, we use these efficient clock distribution schemes to present a novel fast NoC design that relies on source synchronous data transfer over a ring. In our source-synchronous design, the clock and data NoC are routed in parallel yielding a fast, robust design. The source synchronous NoC is clocked by SWOs, which operate significantly faster than the cores that are served by the rings. This allows us to significantly improve the cross section bandwidth and the latency of the NoC. We develop a deadlock-free routing protocol for the source-synchronous ring-based NoC. Our modified source-synchronous design allows the cores to extract a low jitter clock directly from the high speed ring clock by division, and hence the cores operate synchronously with the NoC. This is significant since it eliminates synchronizer latencies that are typically incurred in an asynchronous design. Using the above modified design, we propose a class of source-synchronous, floor-plan friendly NoC topologies which consume significantly lower area compared to a state of the art mesh. Architectural simulations on synthetic and real traffic show that our source-synchronous NoC designs can provide significantly lower latency

while achieving the same or better bandwidth compared to a state of the art mesh, while consuming lower area. In addition, our routing scheme performs well under adversarial traffic as well. The fact that the our ring-based NoC runs significantly faster than the mesh contributes to these improvements. Moreover, since our proposed NoC designs are fully synchronous, they are very amenable to testing as well.

In the final part of this book, we explore an alternate scheme of achieving high-speed on-chip data transfer. Traditional pulse-based on-chip data transfer achieves a maximum data transfer rate of one bit per wire per clock cycle. Instead, we propose the use of sinusoidal signals of different frequencies as information carriers for on-chip data transfer. The key advantage of our method is the ability to superimpose such sinusoids and thereby effectively send multiple logic values along the same wire in a clock cycle. Experimental results show that for the same throughput as that of a traditional scheme, we require significantly fewer wires. The proposed sinusoidal data transfer scheme can be used for fast off-chip data transfer as well.

In summary, this book presents techniques to address the issue of chip-wide clock distribution, as well as the issue of designing a fast NoC in addition to exploring alternate schemes of achieving high-speed on-chip data transfer.

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September 2013

Source-Synchronous Networks-On-Chip

Circuit and Architectural Interconnect Modeling

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2014, XIII, 143 p. 95 illus., 10 illus. in color., Hardcover

ISBN: 978-1-4614-9404-1