

# Contents

|          |  |           |
|----------|--|-----------|
| <b>1</b> | <b>Introduction</b>  | <b>1</b>  |
| 1.1      | Terminology  | 1         |
| 1.2      | Performance Evaluation Metrics for a Network-on-Chip         | 5         |
| 1.3      | Network-on-Chip Design Aspects                               | 7         |
| 1.3.1    | Topology   | 7         |
| 1.3.2    | Flow Control   | 7         |
| 1.3.3    | Routing  | 8         |
| 1.3.4    | Arbitration  | 9         |
| 1.3.5    | Buffering  | 9         |
| 1.4      | The Need for a Fast Network-on-Chip Design                   | 10        |
| 1.5      | Clock Distribution for fast Networks-on-Chip                 | 10        |
| 1.6      | Source Synchronous Network-on-Chip Design                    | 11        |
| 1.7      | Fast On-chip Data Transfer Using Sinusoid Signals            | 12        |
|          | References   | 12        |
| <b>2</b> | <b>Clock Distribution for Fast Networks-on-Chip</b>          | <b>15</b> |
| 2.1      | Resonant Oscillators   | 15        |
| 2.1.1    | Traveling Wave Oscillators                                   | 16        |
| 2.1.2    | Standing Wave Oscillators                                    | 16        |
| 2.2      | Phase Locked Clock Generation and Distribution Using SWOs    | 18        |
| 2.2.1    | Introduction   | 19        |
| 2.2.2    | Previous Work  | 22        |
| 2.2.3    | Our Approach   | 23        |
| 2.2.4    | Experiments  | 32        |
| 2.2.5    | Conclusion   | 38        |
| 2.3      | Automated Methodology to Generate Low Jitter Buffered H-tree | 39        |
| 2.3.1    | Introduction   | 39        |
| 2.3.2    | Previous Work  | 43        |
| 2.3.3    | Our Approach   | 44        |
| 2.3.4    | Experimental Results   | 49        |
| 2.3.5    | Conclusion   | 52        |

|          |  |            |
|----------|--|------------|
| 2.4      | Tiled SWO-based Clock Distribution .....                               | 54         |
| 2.4.1    | Introduction .....   | 55         |
| 2.4.2    | Previous Work .....  | 56         |
| 2.4.3    | Our Approach .....   | 57         |
| 2.4.4    | Experiments .....  | 61         |
| 2.4.5    | Conclusion .....   | 62         |
| 2.5      | Chapter Summary .....  | 63         |
|          | References .....   | 65         |
| <b>3</b> | <b>Fast Network-on-Chip Design .....</b>                               | <b>67</b>  |
| 3.1      | Circuit Design of a Source Synchronous Ring-based NoC .....            | 68         |
| 3.1.1    | Introduction .....   | 68         |
| 3.1.2    | Previous Work .....  | 69         |
| 3.1.3    | Our Approach .....   | 71         |
| 3.1.4    | Experimental Results .....   | 78         |
| 3.1.5    | Conclusion .....   | 81         |
| 3.2      | Architectural Simulations of a Source Synchronous Ring-based NoC ..... | 82         |
| 3.2.1    | Introduction .....   | 82         |
| 3.2.2    | Previous Work .....  | 83         |
| 3.2.3    | Our Approach .....   | 84         |
| 3.2.4    | Experimental Results .....   | 88         |
| 3.2.5    | Conclusion .....   | 97         |
| 3.3      | Source Synchronous H-tree based NoC .....                              | 98         |
| 3.3.1    | Introduction .....   | 99         |
| 3.3.2    | Previous Work .....  | 100        |
| 3.3.3    | Our Approach .....   | 102        |
| 3.3.4    | Experimental Results .....   | 105        |
| 3.3.5    | Conclusion .....   | 113        |
| 3.4      | Exploring Ring of Star and Spine with Ring Topology for NoC ....       | 114        |
| 3.4.1    | Introduction .....   | 114        |
| 3.4.2    | Previous Work .....  | 115        |
| 3.4.3    | Our Approach .....   | 115        |
| 3.4.4    | Experimental Results .....   | 117        |
| 3.4.5    | Conclusion .....   | 123        |
| 3.5      | Chapter Summary .....  | 123        |
|          | References .....   | 126        |
| <b>4</b> | <b>Fast On-Chip Data Transfer Using Sinusoid Signals .....</b>         | <b>129</b> |
| 4.1      | Introduction .....   | 129        |
| 4.2      | Previous Work .....  | 130        |
| 4.3      | Our Approach .....   | 131        |
| 4.3.1    | Overview .....   | 131        |
| 4.3.2    | Transmitter .....  | 131        |
| 4.3.3    | Receiver .....   | 133        |

|              |   |            |
|--------------|---|------------|
| 4.4          | Experiment .....                                | 135        |
| 4.5          | Conclusion .....                                | 136        |
|              | References .....                                | 137        |
| <b>5</b>     | <b>Conclusion and Future Work .....</b>         | <b>139</b> |
| 5.1          | Future Work on Resonant Clocking .....          | 139        |
| 5.2          | Future Work on Fast Network-on-Chip .....       | 139        |
| 5.3          | Future Work on Fast On-Chip Data Transfer ..... | 140        |
| <b>Index</b> | .....   | <b>141</b> |

Source-Synchronous Networks-On-Chip

Circuit and Architectural Interconnect Modeling

Mandal, A.; Khatri, S.P.; Mahapatra, R.

2014, XIII, 143 p. 95 illus., 10 illus. in color., Hardcover

ISBN: 978-1-4614-9404-1