

Preface

This book includes, but is not limited to, the research work on post-silicon validation during the author Xiao Liu's Ph.D. study. Post-silicon validation is an emerging research field, and limited publications are available to summarize the state of the art on it. Interested readers can refer to our survey paper [1] to know more background.

The book is roughly divided into three parts. The first part (Chaps. 1 and 2) covers the background of VLSI design trends, validation challenges, and current solutions that resolve various problems in post-silicon validation.

The major target of this book is how to conduct signal tracing effectively to provide sufficient observability and controllability during the debug process with low-cost design for debug (DfD) structures. Starting from Chap. 3, we present our automatic solutions to address the problem.

The second part (Chaps. 3–5) introduces several novel tracing solutions proposed in this book. The tracing techniques described in Chaps. 3 and 4 are for tackling functional error, by enhancing visibility and improving error detection quality, respectively, while Chap. 5 describes another tracing solution to deal with electrical error. In Chap. 3, based on the fact that logic values can be restored structurally, we define several evaluation metrics in a theoretically precise manner and conduct structural analysis to estimate visibility, which is then used to guide our trace signal selection algorithms for debugging functional errors. With this technique, the visibility can be dramatically enhanced by state restoration with selected trace data. The work in Chap. 3 is published in [8, 9]. Chapter 4 addresses the limitation that current tracing solutions constrain the debug capability by statically tracing the same signals in the circuit. Motivated by the above limitation, we propose a multiplexed signal tracing strategy. Within the strategy, we divide the tracing procedure into a few periods and develop the algorithms to selectively trace a different subset of accessible signals in each period, so that error detection quality will be improved. This work is published in [12]. Chapter 5 presents a tracing solution for tackling speedpath-related electrical error. This error only occurs under certain electrical environments and is extremely challenging to be root-caused. In our work, we first model the behavior of such electrical error. Accordingly, we propose a trace signal selection method for monitoring these errors. In addition, we develop a novel trace qualification technique that relies on

reconfigurable logic to only store useful traced data, which improves the utilization of the trace buffer. To the best of our knowledge, this is the first tracing solution for debugging electrical errors in general logic circuits in post-silicon validation. With the technique, we are able to detect speedpath-related electrical errors at its root-caused site, on the exact error occurrence cycle, and without requiring any supporting “golden vector”. The tracing solutions included in [Chap. 5](#) are published in [11]. It is recommended to read [Chap. 3](#) before [Chaps. 4](#) and [5](#) because the probability-based terminologies defined in [Chap. 3](#) are further extended to apply on the methods in [Chaps. 4](#) and [5](#).

The third part ([Chaps. 6–8](#)) includes the solutions on cost-effective trace interconnection fabric design. The fabric introduced in [Chap. 6](#) is for increasing the bandwidth of trace data by reusing existing test data transfer channel. The solution is further extended to avoid data corruption during multi-core debug [4]. [Chapters 7](#) and [8](#) include different trace interconnection fabrics to facilitate flexible tracing and systematic tracing during post-silicon validation. To provide sufficient flexibility, we present a novel transfer structure and its optimization technique in [Chap. 7](#). By combining multiplexor network and non-blocking network effectively, the technique can achieve high debug flexibility with minimized hardware cost. This work is published in [6]. On the other hand, we develop a low-cost fabric to support systematical error localization. As to be detailed in [Chap. 8](#), with the fabric we can conduct an automatic tracing procedure to localize error with a few debug runs, so that the efficiency of error localization is greatly improved. Moreover, the fabric is inherently with high capability to tolerate unknown values in “golden vector”. This work is published in [13]. The solutions proposed by [Chaps. 6–8](#) are complementary ones so that the readers can freely read any chapter without going through others.

Every chapter in this book is largely self-contained. One thing to be noted is that the terminologies defined in each chapter are applicable for that chapter only.

Apart from the above automatic solutions on post-silicon validation included in this book, the author also conducted a series of works, which mainly focus on power relevant issues in manufacturing test, during his Ph.D. study. The author observes that growing test data volume and excessive test power are two of the major concerns for the industry when testing large integrated circuits. Various test data compression (TDC) schemes and low-power X-filling techniques were proposed to address the above problems. These methods, however, exploit the very same “don’t-care” bits in the test cubes to achieve different objectives and hence may contradict each other. To address this problem, we propose several holistic solutions that target both issues together. In [2, 3, 5], we consider test power reduction in the code-based test compression environment. By studying and utilizing the features of different encoding techniques, our entropy-based generic solution is able to dramatically reduce test power with little compression ratio loss. For the linear decompressor-based TDC scheme widely used in the industry, we present a novel solution in [7] that dynamically extracts the relationship between don’t-care bits in test patterns and then utilizes it to conduct effective X-filling for various power reduction objectives. These solutions outperform existing solutions significantly in test power reduction. Besides, we find that when testing delay

faults on critical paths, conventional structural test patterns may be applied in functionally unreachable states, leading to over-testing or under testing of the circuits. In [10], we propose novel layout-aware pseudo-functional testing techniques to tackle the above problem. First, by taking the circuit layout information into account, functional constraints related to delay faults on critical paths are extracted. Then, we generate functionally reachable test cubes for every true critical path in the circuit. Finally, we fill the don't-care bits in the test cubes to maximize power supply noises on critical paths under the consideration of functional constraints. The technique is able to exercise the worst-case timing of critical paths in functional mode, which facilitates to reduce test escapes and test overkills simultaneously and guarantees high test quality.

To conclude, the solutions proposed during the author Xiao Liu's Ph.D. study aim at improving both validation and test quality on high reliable electronic devices.

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