

Chapter 2

A Piezo-resistive, Temperature Compensated, MEMS-Based Frequency Synthesizer

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Abstract This paper describes a frequency synthesizer based on a MEMS resonator. Uniquely, the piezo-resistive properties of silicon are exploited to read out the resonator, resulting in low impedance levels at resonance frequencies up to several 100 MHz. A 55 MHz MEMS oscillator with a phase noise of -128 dBc/Hz @ 1 kHz offset and a -140 dBc/Hz noise floor has been realized. The oscillator is combined with a programmable PLL to realize a complete frequency synthesizer that can generate output frequencies ranging from 25 MHz to 200 MHz. It achieves ± 20 ppm frequency accuracy over temperatures ranging from -20°C to $+85^\circ\text{C}$, and draws 15 mA from a 2.5 V supply at an output frequency of 25 MHz.

2.1 Introduction

An emerging class of high performance Phase Locked Loop (PLL) based frequency synthesizers uses MEMS resonator technology replacing the bulky quartz resonator as frequency referencing element [1]. The extraordinary small size, high level of integration, low cost and high volume manufacturing capability that is possible with MEMS appear to open exceptional possibilities for creating miniature-scale precision reference oscillators at low cost. The MEMS resonator can be combined with a PLL in a single module using a standard low cost plastic package. It can be expected that a MEMS-based PLL has a superior noise performance and frequency stability compared to self-referenced CMOS synthesizers, since the MEMS-based oscillator is based on mechanical resonance exhibiting a much higher Q -factor than

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LC based electrical resonators. At the same time, it is expected that the use of MEMS reduces the size and cost and increases the level of system integration compared to quartz referenced PLLs, since the processes and materials being used are often CMOS compatible and use the CMOS manufacturing infrastructure. MEMS technology allows the realization of high performance frequency synthesizers with low noise and a high degree of frequency stability without the need for an external quartz crystal. Thereby reducing the footprint of the synthesizer, reducing the number of I/O pins on the package and associated solder connections, and ease of design-in.

As a rule of thumb, the reference frequency, f_{ref} produced by the MEMS oscillator should be chosen as high as possible in order to minimize the noise and spur contribution of the MEMS reference oscillator to the PLL's output frequency [2]. The first reason is that a PLL which employs a sequential phase-frequency detector and charge pump (PFD/CP) is in reality a sampled system, due to the nature of the PFD. As a consequence, the sampling process places an upper limit on the open-loop bandwidth of the PLL in relation to f_{ref} . The second reason to keep f_{ref} high is to minimize the amplitude of spurious components at offset frequencies $N \cdot f_{ref}$ with N being an integer number. The spurious signals result from leakage currents at the voltage controlled oscillator (VCO) input and at the loop filter or from CP imperfections. The third and most important reason to maximize f_{ref} is because the equivalent synthesizer phase noise floor is effectively multiplied by M^2 , where M is the division ratio of the main divider, when converted to the output of the VCO. So, to minimize the noise contribution from the synthesizer blocks one needs to minimize the divider ratio M . By maximizing f_{ref} the division ratio M is minimized for a given output frequency. Higher reference frequency at the PFD can be used resulting in smaller multiplication factors. The expected improvement in the phase noise of $20 \cdot \text{Log}(M)$ is somewhat reduced due to the fact that the PFD adds more noise at higher frequencies. A phase noise improvement of $10 \cdot \text{Log}(M)$ is however realistic. In practice an upper limit of f_{ref} is set by the fact that driving the PFD for standard CMOS technology beyond a frequency of 130–150 MHz will cause strong degradation of the phase noise [3] and a f_{ref} in the range of 50–150 MHz seems ideal.

Conventional MEMS resonators are based on capacitive transduction: the resonator motion is detected through a capacitance measurement that measures the change of capacitance between the resonator perimeter and a sense electrode held at fixed position. Capacitive resonators have the intrinsic disadvantage of having relatively high impedance compared to piezoelectric resonators, such as quartz. These limitations find their origin in the low level of electro-mechanical coupling that can be achieved with capacitive transduction since measured change in capacitance as a result of the resonator's motion is extremely small, and tends to decrease even further at high resonance frequencies as a result of reduced resonator dimensions at higher frequencies. As such, capacitive transduction of MEMS resonators seems to be in conflict with the desire to have high oscillation frequencies of the reference oscillator interfacing the PLL.

However, an advantage of capacitive transduction is that it allows for the use of single crystal silicon (SCS) as the resonating medium without the need of having

lossy metal electrodes present at its surface, as is the case in piezoelectric MEMS resonators, such as the ones based on aluminum-nitride. Silicon resonators typically show a much higher Q -factor and very little aging compared to their AlN counterparts. Furthermore, SCS resonators are relatively easy to process using SOI wafers and can easily be vacuum packaged on wafer level. Therefore, it is desired to investigate transduction techniques that increase the coupling factor of SCS resonators without having to resort to the lossy piezoelectric and metal thin films exhibiting low Q -factor. A promising transduction scheme that is compatible with SCS exploits the piezo-resistive properties of silicon to sense the mechanical vibration of the MEMS resonator. This concept allows for realizing miniature resonators with a high frequency fundamental tone combined with high output signal and associated low effective impedance. Piezo-resistive resonators are very well suited to realize MEMS based reference oscillators in the 50–150 MHz frequency range that is ideal for interfacing with high performance PLL based frequency synthesizers.

2.2 Oscillator Based on Piezo-resistive Resonator

Instead of detecting gap modulation, as is done in capacitive based resonators, a direct measurement of mechanical strain that is build up inside the resonator body is used to sense its motion. The mechanical strain is detected by means of the piezo-resistive effect. Although silicon is not piezo-electric, it exhibits a strong piezo-resistive behavior and therefore resonators made from Si, and SCS in specific, are well suited to adopt this transduction principle. In this way, strain rather than gap variation is the parameter that is being sensed. The output current can be tailored by the DC bias current that is sent through the resonator.

The unique property of this type of resonator is that its output signal is insensitive to geometric scaling and is therefore suitable for achieving high resonance frequencies because the transduction efficiency does not depend directly on the resonator size. Fundamental mode resonators with resonance frequency at 1.1 GHz with $Q = 550$ [4] and higher order modes up to 4.5 GHz with $Q = 11200$ [5] and more recently even up to 40 GHz with $Q = 130$ [6] have been demonstrated. It is shown that at 1.1 GHz the effective impedance is reduced by orders of magnitude as a result of the piezo-resistive instead of capacitive readout. In [7] a piezo-resistive SCS 10 MHz resonator is demonstrated with a $Q = 125.000$ underpinning the fact that very high Q -factor can be achieved using piezo-resistive transduced SCS resonators.

The resonator described in this work is a dogbone shaped resonator having a fundamental tone at 55 MHz, measuring $20 \times 40 \mu\text{m}^2$, and is etched and released in a $1.5 \mu\text{m}$ -thick SOI layer. The MEMS resonator is sealed in a low pressure ambient using NXP's proprietary thin-film capping technology, which is a low-temperature ($<400^\circ\text{C}$) and low-cost CMOS-compatible process. Figure 2.1 shows a cross-section of a capped resonator. The cavity under the cap can sustain <40 mbar of

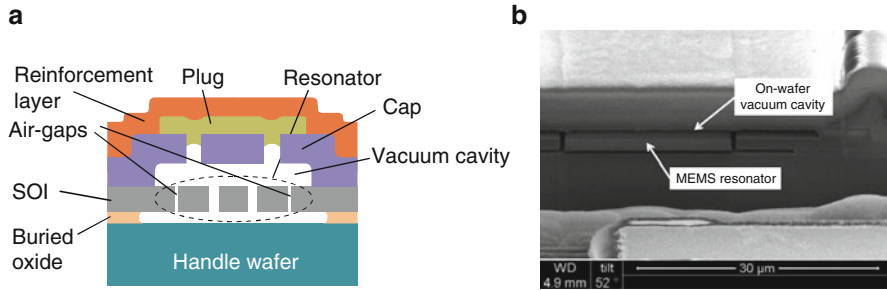


Fig. 2.1 (a) Schematic cross-section of on-wafer vacuum package. (b) FIB cross-section

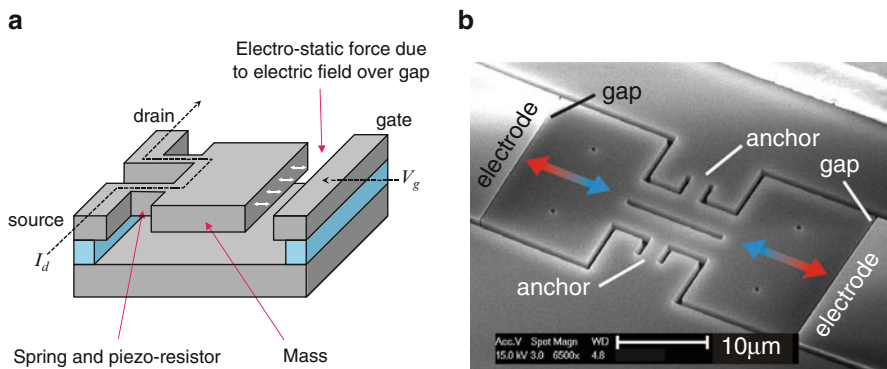


Fig. 2.2 (a) Schematic layout of a piezo-resistive dogbone resonator. (b) SEM top view of realized dogbone resonator

pressure, which is enough to enable resonance with a Q-factor of $>40,000$. The resonator process flow including thin film encapsulation of the resonator has been proven to be manufacturable with high process yield and to survive various accelerated lifetime tests, such as HAST, TMCL, and HTSL, as well as the steps needed for die assembly, such as wafer grinding, dicing and plastic injection molding.

The resonator vibration is sensed using the piezo-resistive effect, causing a strain induced change in the resistance of the spring piezo-resistors. The piezo-resistors can be readout by applying a current bias, I_d over the source-drain terminals that also serve as mechanical anchors of the resonator. At resonance, the modulation of the piezo-resistors results in an AC voltage across the anchors. In the realized device, depicted in Fig. 2.2b, the layout depicted in Fig. 2.2a is mirrored along the source-drain axis in order to have no net force acting on the anchor points when the resonator heads are in resonance. This results in very little loss of vibration energy into the substrate and therefore allows for a high Q-factor [8].

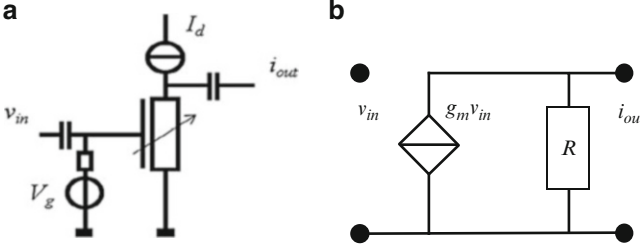


Fig. 2.3 (a) Piezo-resistive resonator equivalent electrical model including bias sources. (b) Small signal model of the resonator

The dogbone resonator is actuated by an electrostatic force, F_{el} via an electrode separated from the dogbone head by a narrow gap of 200 nm, as depicted in Fig. 2.2. The F_{el} is generated by an AC voltage, v_{gap} that is superimposed on a DC bias voltage over the gap, V_{gap} . On its turn, V_{gap} is set by the difference of the applied gate bias, V_g and the voltage on the resonator head. The voltage on the resonator head is set by I_d and the resistance, R of the dogbone and is equal to $I_d R/2$. In most cases, v_{gap} can be approximated by the externally applied AC voltage v_{in} , since the AC voltage on the resonator head is typically much smaller than v_{in} . Furthermore, the electrostatic force scales with change in gap capacitance per unit of displacement of the resonator head and is therefore dependent on gap width, g and frontal area of the dogbone head A_h ,

$$F_{el} = v_{gap} V_{gap} \frac{\epsilon_0 A_h}{g^2} = v_{gap} (V_g - I_d R/2) \frac{\epsilon_0 A_h}{g^2} \approx v_{in} (V_g - I_d R/2) \frac{\epsilon_0 A_h}{g^2} \quad (2.1)$$

The electrical model of the dogbone resonator is described by a time-alternating resistor R with proper bias current I_d and voltage V_g applied, as is shown in Fig. 2.3a. The F_{el} induces a mechanical strain and therefore a relative change in resistance r/R in the two piezo-resistors. The output current i_{out} is simply given by,

$$i_{out} = I_d \frac{r}{R} \quad (2.2)$$

The relative change in resistance r/R is proportional to the resonant displacement of the resonator and is described by a Lorentzian function centered around the mechanical resonance frequency, ω_0 of the resonator that is scaled by the electrostatic force $\alpha V_{gap} v_{in}$ acting on the resonator head,

$$\frac{r}{R} = \frac{\alpha V_{gap} v_{in}}{1 - \frac{\omega^2}{\omega_0^2} + j \frac{\omega}{\omega_0 Q}} \quad (2.3)$$

The pre-factor, α is a constant that sets how strong the F_{el} is concentrated in the resonator springs multiplied by the piezo-resistive gauge factor and has a negative

value for the silicon crystal orientation with respect to the dogbone orientation being used. By combining Eqs. 2.1, 2.2, and 2.3 it can be seen that the relation between i_{out} and v_{in} can be described by a transconductance, g_m as is schematically depicted in Fig. 2.3b,

$$\begin{aligned}
 g_m &= \frac{\alpha}{1 - \frac{\omega^2}{\omega_0^2} + j \frac{\omega}{\omega_0 Q}} I_d V_{gap} \\
 g_{m,max} &= -j\alpha Q I_d V_{gap} \\
 g_{m,norm} &= \frac{|g_{m,max}|}{Q}
 \end{aligned} \tag{2.4}$$

The maximum value of transconductance, $g_{m,max}$ is reached at frequency $\omega = \omega_0$. From Eq. 2.4 it can be seen that the transconductance at resonance frequency is about Q-factor times larger than off-resonance. Hence, the resonator serves as a frequency selective filter in the oscillator loop. It is noted that at resonance there is a 90° phase shift between i_{out} and v_{in} . This is fundamentally different from capacitive or piezo-electric resonators where there is no phase shift between v_{in} and i_{out} at resonance. For convenient comparison of different bias conditions $g_{m,max}$ can be normalized to Q-factor and is called $g_{m,norm}$.

The measured transconductance at resonance of the dogbone resonator is shown in Fig. 2.4 as a function of the product of V_{gap} and I_d when I_d is varied from -2.5 to $+2.5$ mA. From Fig. 2.4a it can be seen that there is indeed a linear relation between the $V_{gap}I_d$ and $g_{m,max}$ as predicted by Eq. 2.4. However, it can be seen that the slope is reduced for large values of I_d . This can be attributed to a small reduction in the Q-factor for large currents caused by a thermal damping effect [9], as is evident from Fig. 2.4c. The bias current dependency is absent when plotting $g_{m,norm}$, as can be seen from Fig. 2.4b underpinning the validity of the simple resonator model. The resonator is typically operated using V_g values between -5 and -10 V and I_d values between $+1$ and $+2$ mA resulting in an inductive behavior of $g_{m,max}$ with values between $-j80$ and $-j320$ $\mu\text{A/V}$, which is equivalent to an impedance of $3\text{--}12$ k Ω or an inductance lying between 9 and 36 μH .

The load, source, and feedthrough capacitances need to be taken into account when inserting the resonator in an oscillation loop, as is schematically depicted in Fig. 2.5. Of particular interest is the feedthrough capacitance, C_{ft} . The C_{ft} causes a feedthrough current, i_{ft} that is preceding the voltage at the resonator input v_{in} by 90° . Therefore, this current cancels in part the inductive current caused at resonance induced by $g_{m,max}$. For the oscillator to lock at the mechanical resonance frequency it is required that $|g_{m,max}| > |\omega_0 C_{ft}|$. In practice, the C_{ft} originates from gate to drain coupling between bond wires and substrate coupling on the MEMS die and is approximately 50 fF which is equivalent to an admittance of $+j18$ $\mu\text{A/V}$ at 55 MHz, which is typically well below the transconductance $g_{m,max}$ of the resonator as is required. Another important impedance is the capacitance at the resonator drain to ground, C_l which is in parallel to the resonator resistance R . Both impedances set

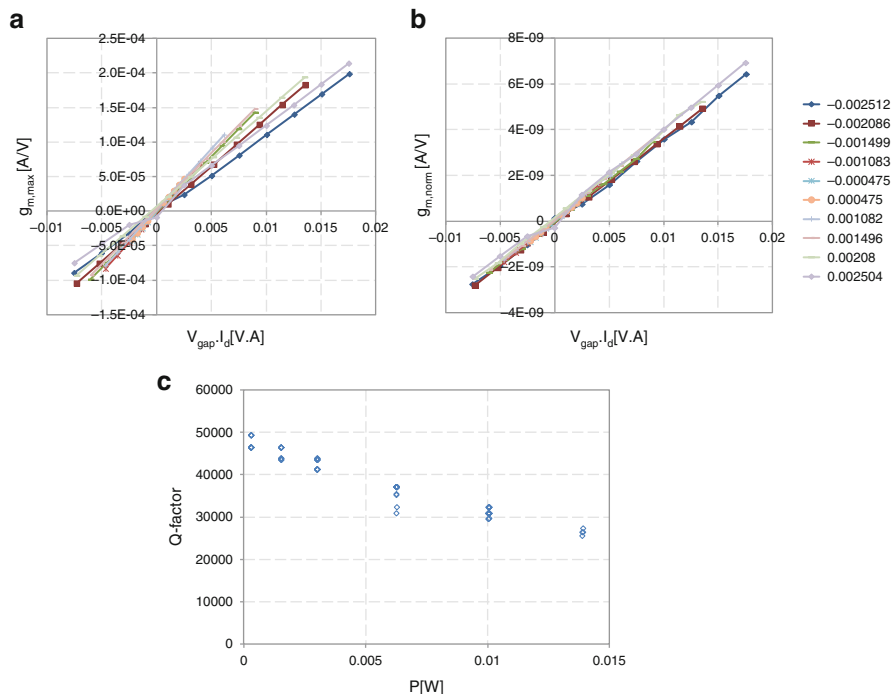


Fig. 2.4 (a) Measured $g_{m,max}$ versus $I_d \cdot V_{gap}$ for different I_d levels varying from -2.5 mA to $+2.5$ mA. (b) $g_{m,max}$ normalized to Q-factor versus $I_d \cdot V_{gap}$ for different I_d levels. (c) Measured Q-factor as a function of dissipated power inside the resonator body

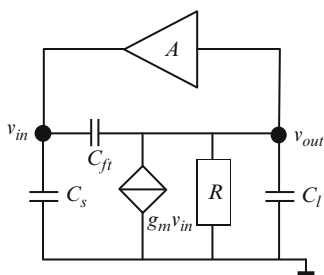


Fig. 2.5 Resonator placed in an oscillator loop, with $R = 600 \Omega$, $C_{ft} = 50$ fF, $C_s = C_l = 1$ pF

the phase between i_{out} and the voltage, v_{out} at the input of the amplifier. In our case the resonator resistance is set at 600Ω by choosing the appropriate doping level in the SOI layer. The C_l consists of bondpad capacitance on the MEMS die and the amplifier die and is estimated to be 1 pF resulting in a phase difference between i_{out} and v_{out} of 10° at 55 MHz. Therefore the total phase shift between v_{in} and v_{out} is

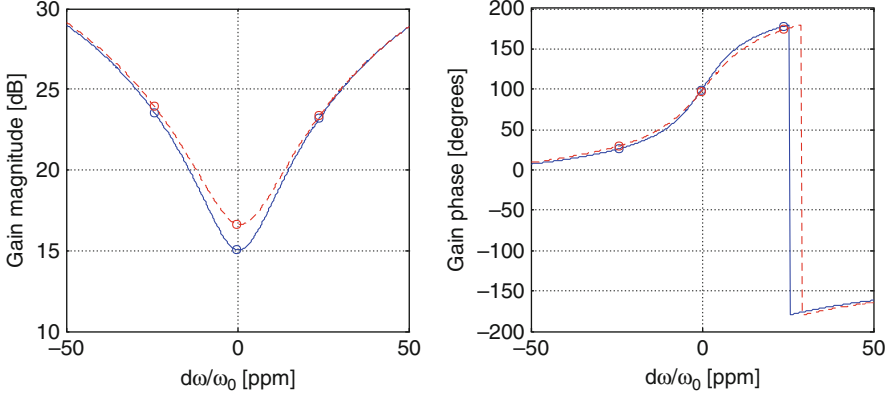


Fig. 2.6 Required amplifier gain and phase to sustain oscillation at $V_g = -8$ V, $I_d = 1.75$ mA, $Q = 40.000$, $f_0 = 55$ MHz, $R = 600$ Ω , $C_l = C_s = 1$ pF, $C_{ft} = 50$ fF. Dots are for $d\omega/\omega_0 = -1/Q$, $\omega = \omega_0$, and $d\omega/\omega_0 = +1/Q$, respectively. *Blue solid line* include thermal expansion effects while the *red dashed line* does not

estimated to be $-90-10^\circ = -100^\circ$. Based on this simple model the voltage attenuation of the resonator at resonance frequency ω_0 can be written as,

$$\left| \frac{v_{out}}{v_{in}} \right| = \frac{|g_{m,max} - \omega_0 C_{ft}|}{\sqrt{\left(\frac{1}{R}\right)^2 + (\omega_0 C_l)^2}} \quad (2.5)$$

Assuming resonator bias of $V_g = -8$ V and $I_d = 1.75$ mA, corresponding to $g_{m,max} = 270$ μ A/V, results in a voltage attenuation of -17 dB according to Eq. 2.5. Therefore, the amplifier, A in Fig. 2.5 should be able to provide a gain of $+17$ dB and a phase rotation of $+100^\circ$ in order to sustain oscillation.

Using a more sophisticated model, the complex amplifier gain is calculated as a function of oscillation frequency, as is shown by the blue solid line in Fig. 2.6. It can be seen that the phase rotation is indeed close to 100° , as predicted by the simple model. However, the required gain at ω_0 is calculated to be 15 dB, which is 2 dB less than predicted by Eq. 2.5. The difference can be attributed to thermal forces acting on the resonator body that help to reduce the resonator attenuation. This can be concluded from a simulation where it is assumed that there is no thermal expansion of the resonator, as indicated by the red dashed curve in Fig. 2.6. This thermal expansion effect is neglected in Eq. 2.5.

From Fig. 2.6 it can be seen that the phase selectivity of the oscillator is very good: $\pm 75^\circ$ change in loop phase results in only $\pm 1/Q$ frequency pulling. This phase margin is much more than $\pm 45^\circ$ typical for a quartz resonator for similar pulling levels. This is a direct result of the fact that our resonator has an inductive and not a resistive behavior at resonance as is the case with piezo-electric and capacitive resonators. This complex admittance in combination with the complex

feedthrough admittance of opposite sign causes a very large phase rotation of 360° around resonance.

One important characteristic of the piezo-resistive transduction is that in addition to mechanical noise, now the resonator is also a source of electrical noise originating from the electrical energy dissipated in the resistor. Obviously, these additional noise sources need to be taken into account when optimizing the phase noise of the oscillator. The white noise of the resonator contributes to the phase noise floor. The current noise originating from the resonator is expressed as,

$$\overline{i_{noise}^2} = \frac{4k_bT}{R} df \quad (2.6)$$

The ratio of this undesired noise and the desired signal generated by the resonator sets the fundamental lower limit of the phase noise floor. From Eq. 2.1 the mean-squared signal from the resonator is expressed as,

$$\overline{i_{signal}^2} = \frac{1}{2} \left(I_d \frac{r}{R} \right)^2 \quad (2.7)$$

Therefore the noise-to-signal ratio output of the resonator is written as,

$$\frac{\overline{i_{noise}^2}}{\overline{i_{signal}^2}} = \frac{8k_bT}{I_d^2 R} \left(\frac{r}{R} \right)^{-2} df \quad (2.8)$$

Or expressed in terms of $g_{m,max}$ and v_{in} ,

$$\frac{\overline{i_{noise}^2}}{\overline{i_{signal}^2}} = \frac{8k_bT}{\left(v_{in} g_{m,max} \right)^2 R} df \quad (2.9)$$

Half of this ratio goes into phase noise, assuming that the white noise is evenly spread over amplitude and phase. From Eq. 2.8 it can be easily understood that lower phase noise is achieved by increasing the DC power dissipation in the resonator and by increasing the level of resistance modulation. In Fig. 2.7 the measured resistance modulation is shown for a large population of more than 1,100 devices when driving the resonator with $V_g = -5$ V and AC peak voltage $v_{in} = 1V_{pk}$. It can be seen that under these bias conditions the average resistance modulation is $r/R = 8\%$. Assuming 2 mW of dissipation inside the resonator and a resistance modulation level of 8% gives a fundamental phase noise floor of -149 dBc/Hz. In practice, a few dBc/Hz still needs to be added to account for noise contributions of the amplifier and resonator bias sources. In Fig. 2.8 the measured phase noise of a complete oscillator is plotted for $v_{in} = 0.5V_{pk}$, $V_g = -8$ – 10 V, and $I_d = 1.75$ – 2 mA. The measured phase noise is approximately 7 dB above the fundamental minimum as estimated from Eq. 2.9. The 7 dB added noise is attributed to contributions from the bias source and amplifier. Furthermore, it is demonstrated that a low near carrier noise of only -128 dBc/Hz at 1 kHz offset can be realized.

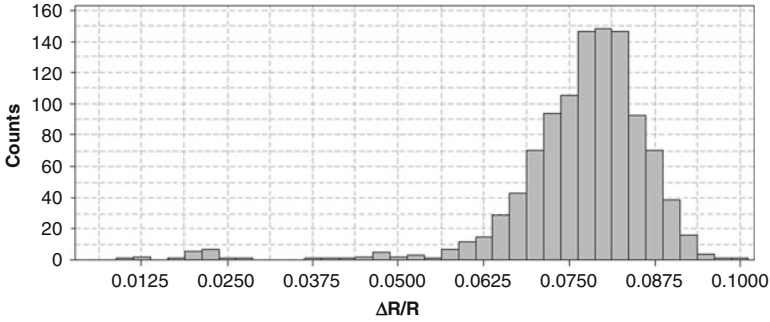


Fig. 2.7 Measured r/R modulation of a dogbone resonator for a population of 1,100 devices driven at DC bias $V_g = -5$ V and AC peak voltage $v_{in} = 1V_{pk}$. Average r/R is 8 %

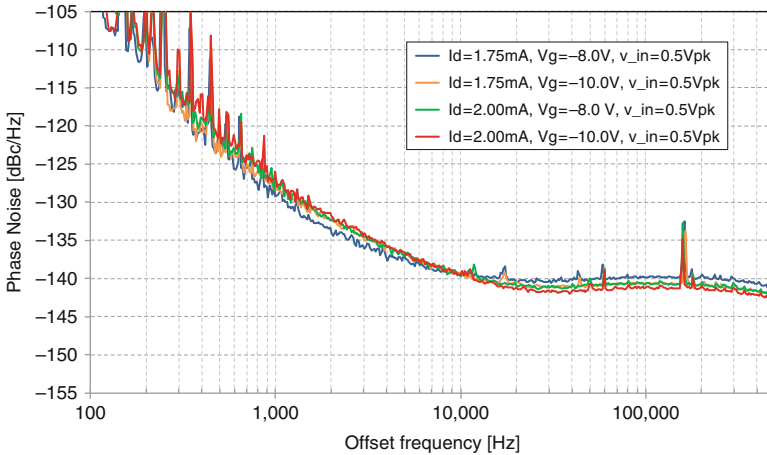


Fig. 2.8 Measured phase noise under different resonator bias conditions. Measured noise floor is below -140 dBc/Hz and is about 7 dB higher than the fundamental minimum set by the noise contribution from the resonator itself

Apart from noise requirements or non-deterministic frequency stability, an oscillator also has to fulfill requirements regarding its deterministic frequency stability and absolute accuracy. The uncompensated temperature stability of MEMS resonators is approximately -30 ppm/K and is inferior to that of quartz and can be attributed to the relatively large negative temperature coefficient, dE_{Si}/dT of the Young's modulus of SCS. In a piezo-resistive resonator the temperature is not only determined by the ambient temperature, but also by the additional heating of the resonator caused by the power dissipated through the bias current I_d . In Fig. 2.9 the resonance frequency of the resonator is shown, both as function of power dissipated in the resonator and ambient temperature. It can be seen that increasing these parameters reduces the resonance frequency of the dogbone resonator, as expected.

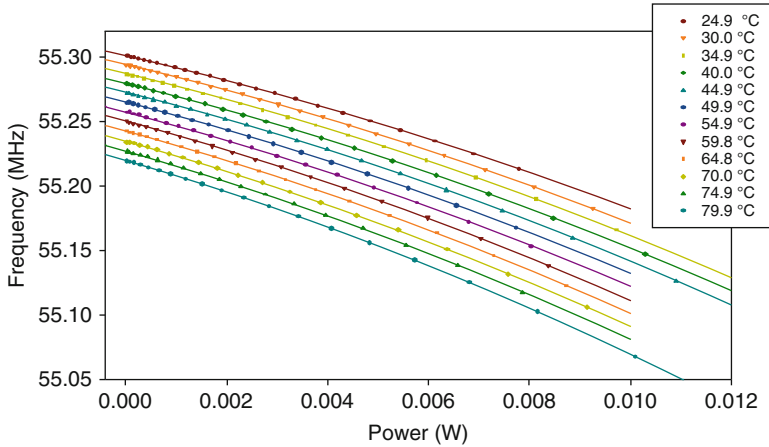


Fig. 2.9 Measured resonance frequency of a non-oxidized resonator as a function of ambient temperature and power dissipation inside the resonator body

Compensation of the temperature dependency of the Young's modulus can be achieved through material modification of the resonator. Silicon and most other materials exhibit a negative temperature dependence of the Young's modulus. When these materials are combined with a material with an opposite signed Young's modulus temperature dependence, such as SiO_2 , then temperature drift compensation is achieved [10]. Considering the spring of the dogbone resonator it can be seen that the strain is evenly distributed over its cross section. For cancelling the temperature drift it is therefore necessary that a cross-section holds approximately equal amounts of Si and SiO_2 , since the temperature derivative of the Young's modulus of silicon dE_{Si}/dT is about equal in magnitude to the temperature derivative dE_{SiO_2}/dT . This in general means that the thickness of the oxide layer increases when resonator dimensions increase and can lead to excessive oxidation times in the case the resonator is thermally oxidized. The fact that the output current of a piezo-resistive resonator is not dependent on its dimensions, as opposed to a capacitive bulk mode resonator, makes the piezo-resistive concept well suited for this oxidation technique, since the required oxide thickness for first order temperature drift cancellation can in practice be limited to only a few 100 nm, as is shown in Fig. 2.10a. It can be seen that the temperature coefficient of the resonance frequency is increased by increasing the oxide thickness at a rate of 0.12 ppm/K/nm. Figure 2.10b shows the temperature drift of an oxidized Si resonator compared to a non-oxidized resonator, AT-cut quartz resonator, and a tuning fork quartz resonator when the oxide thickness is tuned to cancel the first order drift term. It can be seen that the oxide layer effectively compensates for the first order temperature drift even when considering accuracy to which the thickness of the SiO_2 layer can be controlled in production. Higher order drift terms still remain which are attributed to higher order drift terms of the SCS itself.

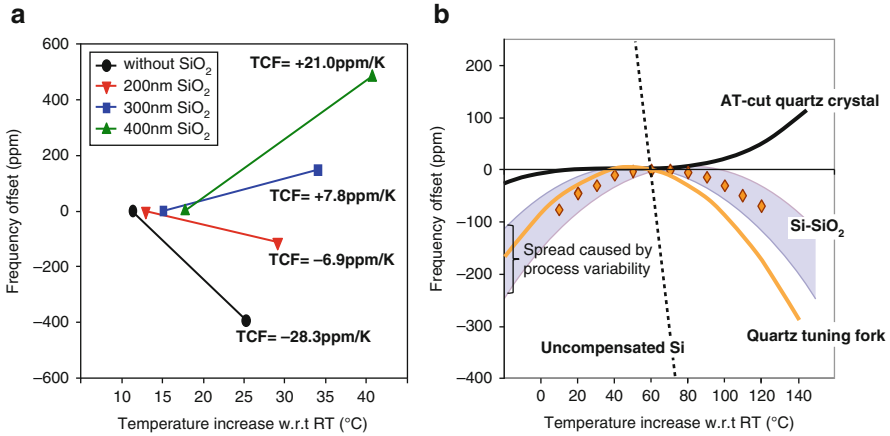


Fig. 2.10 Measured temperature drift reduction through thermal oxidation of the resonator. (a) Temperature drift as a function of oxide thickness. (b) Residual, high order temperature drift compared to quartz and non-compensated SCS

A drawback of oxidizing the resonator is that the oxidation causes a considerable shift of resonance frequency at fixed temperature, since the Young's modulus of SiO₂ $E_{SiO_2} = 60$ GPa is considerably lower than the Young's modulus of Si $E_{Si} = 130$ GPa. Growing an oxide layer on the resonator reduces its stiffness and hence lowers its resonance frequency at a rate of -380 ppm/nm for our dogbone resonator [11]. This dependency is much stronger than the oxide thickness dependency of the first order temperature drift and limits the overall frequency accuracy caused by variations in oxide thickness. Uniform thermal oxidation of SCS resonators alone does not lead to the level of accuracy in resonance frequency that is typically required for reference oscillators and timing applications. However, in PLL based synthesizers the offset in resonance frequency and any residual temperature drift can easily be calibrated out during product calibration, hence elegantly solving the issue of process induced spread of the MEMS resonance frequency and temperature drift.

2.3 Frequency Synthesizer Based on Piezo-resistive MEMS Oscillator

The frequency synthesizer product comprises a MEMS die stacked on top of an ASIC die in a lead-less plastic package with a 5.0×3.2 mm² footprint, as is shown in Fig. 2.11. The frequency synthesizer has a LVCMOS frequency output that is programmable between 25 and 200 MHz. The current is drawn from a 2.5 to 3.3 V supply voltage and consumes less than 50 μ A in standby mode.

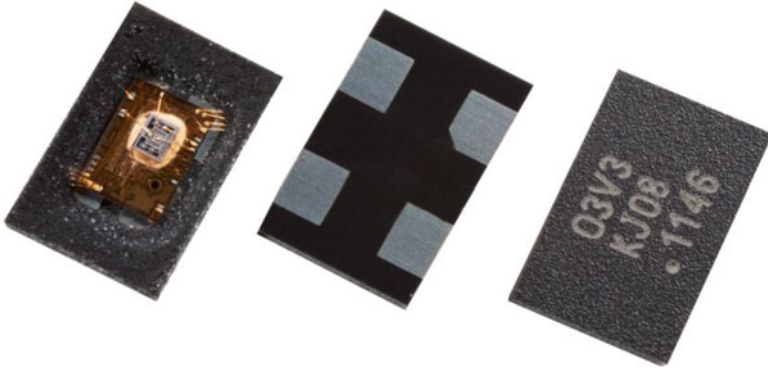


Fig. 2.11 Product assembled in a leadless 4-pin plastic package measuring $5.0 \times 3.2 \text{ mm}^2$. *Left:* The MEMS resonator chip is stacked and wire bonded to the ASIC. *Middle:* Bottom view of package showing supply, ground, enable, and frequency output pins. *Right:* Top view of package

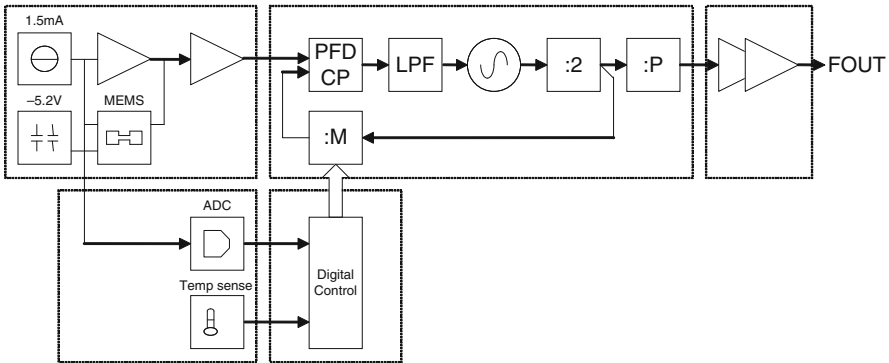
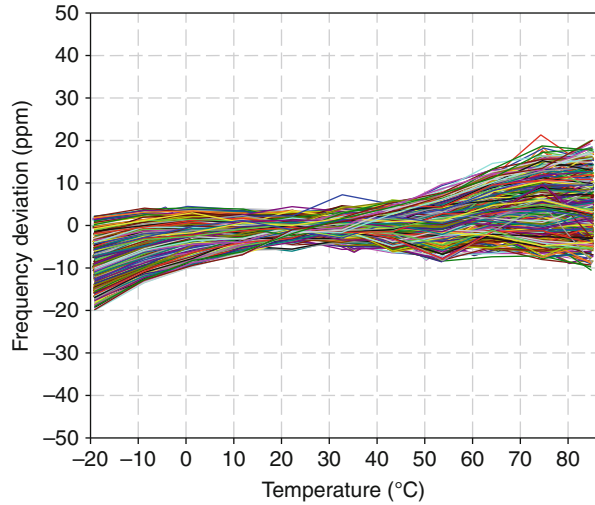


Fig. 2.12 System architecture of the frequency synthesizer

The system architecture is shown in Fig. 2.12 indicating the various functional blocks. The MEMS resonator is biased at -5 V at the gate terminal using a charge pump. On the drain port the resonator is biased at 1.5 mA coming from a current source. The resonator drain signal is amplified by a two-stage amplifier and the amplified signal is fed back to the gate terminal with proper phase shift. The output of the MEMS oscillator is fed into the PFD which drives the CP that generates a correction voltage that is fed into a VCO. The VCO is based on a 2 GHz LC tank that is continuously tunable over the full temperature range via a varactor. A varactor instead of a capacitor bank is used to stabilize the VCO frequency over temperature in order to avoid discrete frequency steps at the VCO output. The frequency range of $25\text{--}200 \text{ MHz}$ can be programmed in 30 Hz steps by setting the proper values of the frac-M divider, the P divider, and by selecting the proper VCO band through a switched capacitor bank that is integrated in the LC tank. Several low-dropout regulators (LDOs) are in place to stabilize the supply voltage for the different circuit blocks.

Fig. 2.13 Frequency stability against ambient temperature, and supply voltage varied from 2.4 to 3.6 V, measured on 110 samples



The frequency offset and temperature drift of the MEMS is compensated for by programming the value of the frac-M divider in the PLL. For temperature drift correction both the ambient temperature as well as the power dissipation inside the resonator needs to be known. The ambient temperature is measured with a PTAT sensor that is integrated on the ASIC. The power dissipation inside the resonator is derived from the stabilized 1.5 mA resonator current bias plus a voltage reading through an ADC connected to the resonator drain terminal. The shift in MEMS frequency is calculated by feeding the resonator drain voltage and the PTAT sensor output into a polynomial with coefficients that are pre-programmed in the MTP. The calculated MEMS frequency shift sets the value of the frac-M divider in the PLL and compensates the temperature induced frequency shift of the MEMS at the input of the PFD. Frequency calibration is done at room temperature only and is used to compensate for manufacturing spread in the MEMS resonance frequency. The frequency versus temperature relation is not calibrated for individual samples and is assumed to be the same for all MEMS resonators. This single temperature insertion calibration results in a frequency spread of less than ± 20 ppm over a temperature window of -20°C – $+85^{\circ}\text{C}$ and supply window of 2.4–3.6 V, as is shown in Fig. 2.13 on a population of 110 samples. It should be noted that in this case a non-oxidized resonator was used.

Measured phase noise at 100 MHz output frequency is shown in Fig. 2.14. Integrated phase jitter is measured to be 0.44 ps in the 1.9–20 MHz band and 2.96 ps in the 12 kHz–20 MHz band. Current dissipation as a function of output frequency for supply voltage of 2.5 and 3.3 V under minimal loading condition on the output pin is shown in Fig. 2.15a. It can be seen that current consumption is less than 15 mA at 25 MHz and increases up to a maximum of 22 mA at 200 MHz output frequency. Zooming in on the power budget breakdown as depicted in the pie chart of Fig. 2.15b it can be seen that the VCO is with 43 % the largest contributor to

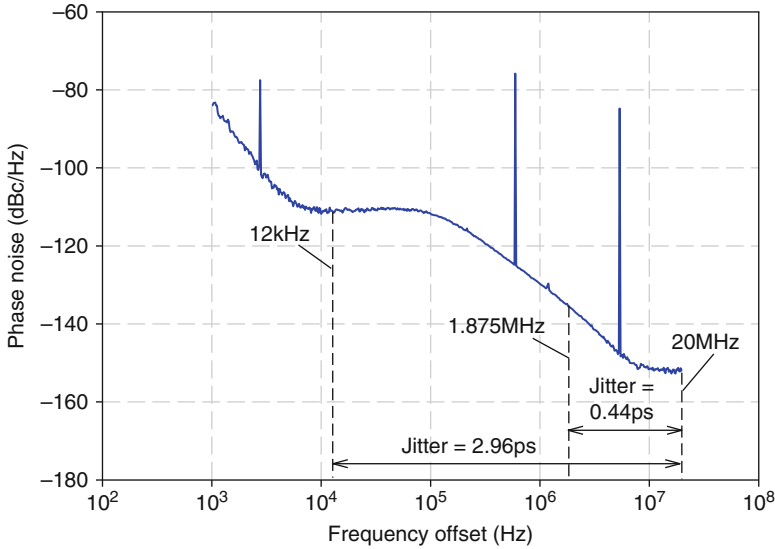


Fig. 2.14 Measured phase-noise of a frequency synthesizer programmed to output 100 MHz

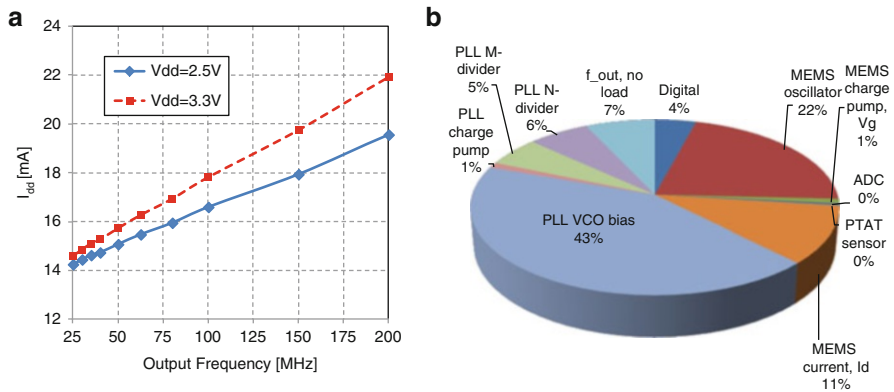
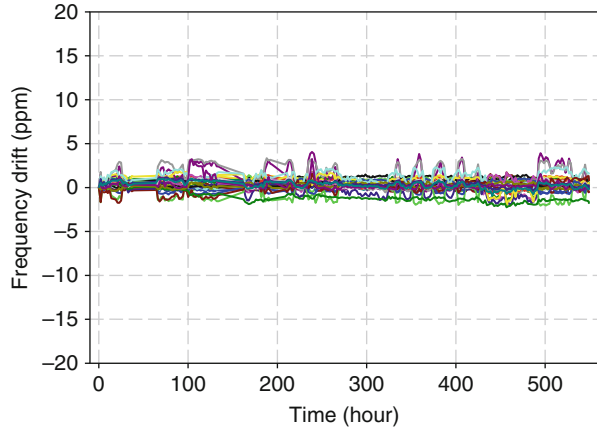


Fig. 2.15 (a) Current consumption, I_{dd} of the complete synthesizer under minimal load condition measured for $V_{dd} = 2.5$ V and $V_{dd} = 3.3$ V supply voltage. (b) Break down of power consumption over different circuit blocks when output frequency is programmed at 25 MHz

overall power dissipation followed by the MEMS core amplifier including MEMS drain bias consuming a combined 33 % of total power.

An ageing test is performed on a population of 30 products to assess frequency stability over time, as is shown in Fig. 2.16. During the ageing test the product is kept in an oven at $+85^{\circ}\text{C}$ and powered at nominal supply voltage. It can be seen that no fails occur and no significant frequency ageing is observed over a period of more than 25 days.

Fig. 2.16 Life-time test at 85°C on 30 samples, lasting for 25 days, showing a frequency stability of better than ± 4 ppm



2.4 Conclusion and Outlook

A piezo-resistive transduced MEMS resonator has the unique property that its output signal is not reduced when scaling down its physical dimensions. This makes it suitable for realizing fundamental tone MEMS oscillators with high output frequency in the 50–150 MHz range that is ideal for interfacing with high performance PLL based frequency synthesizers. A low noise, 55 MHz fundamental tone piezo-resistive MEMS oscillator is demonstrated with a phase-noise floor below -140 dBc/Hz and near carrier noise of -128 dBc/Hz at 1 kHz offset.

The first order temperature induced frequency drift of the SCS resonator can effectively be reduced by coating the resonator with a layer of thermally grown SiO_2 . The oxide thickness should be in proportion with the resonator dimensions in order to effectively remove the first order drift term. It is desired that resonator dimensions are small in order not to require excessively thick SiO_2 layers and associated complications in wafer processing. Also this aspect combines well with piezo-resistive instead of capacitive transduced resonators.

A fully functional PLL based frequency synthesizer running from a 2.5–3.3 V supply has been realized based on a 55 MHz MEMS reference resonator. The MEMS die containing the piezo-resistive resonator is stacked on top of and wirebonded to the ASIC. The stacked die is assembled in a low cost 4-pin leadless plastic package measuring $3.2 \times 5 \text{ mm}^2$. The frequency drift with temperature of the uncompensated MEMS resonator is effectively monitored measuring the (a) ambient temperature with a PTAT sensor and (b) power dissipation inside the resonator that is induced by the resonator bias current. Both parameters are used for programming the frac-M divider in the PLL thereby stabilizing the frequency at the VCO output. It is demonstrated that a frequency accuracy of ± 20 ppm over -20°C – $+85^\circ\text{C}$ is realized for a population of 110 products incorporating a non-oxidized resonator using only a single insertion frequency

calibration at room temperature. The timing jitter level at the output of the frequency synthesizer is sufficiently low for clocking low- to mid-end high speed digital data transmission.

Future work will focus on further reducing the jitter, especially jitter contributions within the loop bandwidth of the PLL that find their origin in the PFD/CP and MEMS core. Furthermore, it is expected that the incorporation of oxidized MEMS resonators will further improve overall frequency stability over temperature of the synthesizer to levels well below 20 ppm.

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