

Chapter 2

Design of Double-Pole Four-Throw RF Switch

2.1 Introduction

The industrial, scientific, and medical (ISM) radio bands were originally reserved for the use of radio-frequency (RF) energy for industrial, scientific, and medical purposes such as radio-frequency process heating, microwave ovens, and medical diathermy machines. The powerful emissions of these devices can create electromagnetic interference and disrupt radio communication using the same frequency, so these devices were limited to certain bands of frequencies. In general, communication equipment operating in these bands must accept any interference generated by ISM equipment [1, 2]. Nowadays CMOS wideband switches are designed primarily to meet the requirements of devices transmitting at ISM band frequencies (900 MHz and above). The low insertion loss, high isolation between ports, low distortion, and low current consumption of these devices make them an excellent solution for several high-frequency applications [3].

This chapter begins with an introduction to the various families of switch topologies used in earlier researches [4–6]. Specifications for an integrated CMOS switch are then developed, followed by a description and working of the topology used in this book. Based on earlier reported works [7] and datasheets of existing parts [8], a set of specifications are analyzed for an integrated transceiver switch for advanced wireless local area network (LAN) systems [9, 10]. The asymmetry in the received and transmitted power levels can be effectively used to arrive at a set of specifications which can be met by designs in a CMOS technology.

2.2 Comparison of Various Switches

There are varieties of switches available in the market; however, the most important and basic types of switches are discussed as follows.

2.2.1 PIN Diode Switch

A PIN diode is a semiconductor diode in which a high resistivity intrinsic (I) region is sandwiched between p-type and n-type region and named as P-I-N. Without bias, the diode behaves like a capacitance and with biasing the diode behaves like an inductor. It has a very significant linearity, so it can be used for high-frequency (HF) applications and very high power applications; however, as the higher DC power applied, the lower insertion loss occurs. PIN diode is a current-controlled resistance that operates as a variable resistor at RF and microwave frequency regime of the electromagnetic spectrum. The resistance value of the PIN diode is determined only by the forward-biased DC current. An additional feature of the PIN diode is its ability to control large RF signals while using much smaller levels of DC excitation. In the ON-state, the diode is biased using a large current of about 10 mA which ensures that the AC resistance is low [8]. In the OFF-state, the PIN structure has a low junction capacitance which ensures the large isolation. PIN diodes can be fabricated in silicon and gallium arsenide and it shows very significant insertion loss (<1 dB) and power handling (>5 W) up to very high frequencies; their static power consumption due to the bias current remains a severe limitation [9]. Since a large bias current is typically required for switch operation, it must be supplied through a choke. Due to limitations of static power consumption, diode switches are being gradually replaced by GaAs MESFET, which offers only slightly worse performance for significantly lower static power consumption.

2.2.2 GaAs FET Switch

A GaAs-integrated circuit switch is an integrated circuit using field-effect transistors to achieve switching between multiple paths [10]. It acts as a voltage-controlled resistor, used for the broadband usually from 0.5 to 4 GHz. This switch specially tuned for application at 5–6 GHz, with low insertion loss of 0.25 dB with good isolation performances and low power consumption and better switching speed. However, it can work up to maximum control voltage of 6 V. To avoid the above disadvantages of the PIN diode switch and GaAs switch, we proposed the CMOS switch. A CMOS switch is an integrated circuit using MOSFET to achieve switching between multiple paths [11]. It has low dependency of the P_1 dB versus control voltage with better switching speed. Other parameters for the CMOS switch are discussed in this chapter and following chapters.

2.2.3 MESFET Switch

The Metal Semiconductor Field Effect Transistor (MESFETs) are majority carrier devices and applicable for high-speed operation. It can be implemented using silicon, gallium arsenide, and indium phosphide [12]; however, silicon-based

MESFETs are incapable of handling large powers and typically slower than those implemented using the other materials. For high-power (>1 W) and high-frequency (>1 GHz) applications, the MESFETs are implemented using GaAs. This is due to large band gap of GaAs, and hence a large breakdown voltage that allows high voltage operation with no reliability concerns can be achieved [13]. For the design of a GaAs MESFET, the main trade-off is between its ON-state resistance and OFF-state capacitance. In order to achieve a low insertion loss, a large device with a low ON-resistance can be used. This degrades the isolation performance since the OFF-state capacitance will be large. An important limitation is that they cannot be integrated with silicon-based transceivers. Another limitation of GaAs MESFET switches is their power handling capability, as compared to PIN diodes [8, 9]; GaAs MOSFET switches do not consume static power, which makes them attractive for low-power wireless communication devices.

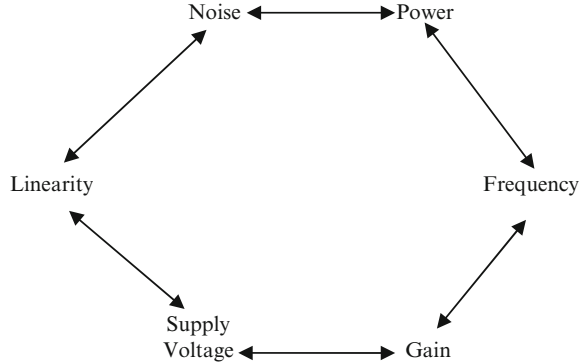
2.2.4 MOSFET Switch

The Metal-Oxide-Semiconductor Field-Effect-Transistor (MOSFET) is one of the simplest switch options. It is available in a Complementary Metal-Oxide-Semiconductor (CMOS) process, and its performance improves every decade. Only silicon-based MOSFETs are suitable for the switch due to the absence of a gate insulator for other materials [14]. The ON-resistance of silicon MOSFET is significantly inferior to a GaAs MESFET due to poor electron and hole mobility in channel at low electric fields. Recent technology offers very small channel length MOSFETs with a better $R_{ON} \times C_{OFF}$ product [15]. The thin gate dielectric and small channel length permit a low voltage operation. The channel resistances and the substrate resistances are the main sources of power loss in the MOSFET. The substrate resistance may be reduced by grounding the substrate as close to the device as possible. The low quality factor of the source and drain parasitic junction capacitors can also lead to significant losses, especially as the frequency of operation increases. The linearity of the MOSFET switch is limited for large signal swings due to conductivity modulation caused by a changing gate-source (V_{gs}) and drain-source (V_{ds}) voltage for a large signal input.

2.2.5 MEMS Switch

The Micro-Electro-Mechanical (MEMS) switches are micro-machined devices which use a mechanical and physical movement to achieve ON (short) or OFF (open) circuit in the transmission line [16]. The mechanical and physical movement of MEMS switch controls the impedance of a transmission line. Generally RF MEMS switches are designed to operate in millimeter wave or microwave frequencies (0.1–100 GHz) regime of the spectrum. The RF MEMS switches have an advantage over the traditional RF switches with their broadband operation, high

Fig. 2.1 Radio-frequency design hexagon



isolation, low insertion loss, low power consumption, simple biasing networks, and low intermodulation products [17]. However they have several disadvantages like slow switching speed in the orders of microsecond, high actuation voltage requirement, and hot switching effects in high-power applications.

RF circuits suffer from trade-offs among various parameters as shown in Fig. 2.1 an RF design hexagon, where six important circuit parameters are shown to trade-off each other. It is interesting to point out that in some cases (e.g., power amplifiers) if the supply voltage is reduced, the power dissipation may increase [18]. For this reason, supply scaling in RF circuits lags behind that in digital circuits. The RF design hexagon also indicates that simple figures of merit such as the transit frequency, unity power gain frequency, and gate delay cannot be easily used to predict RF performance because they do not reflect many of the trade-offs [19].

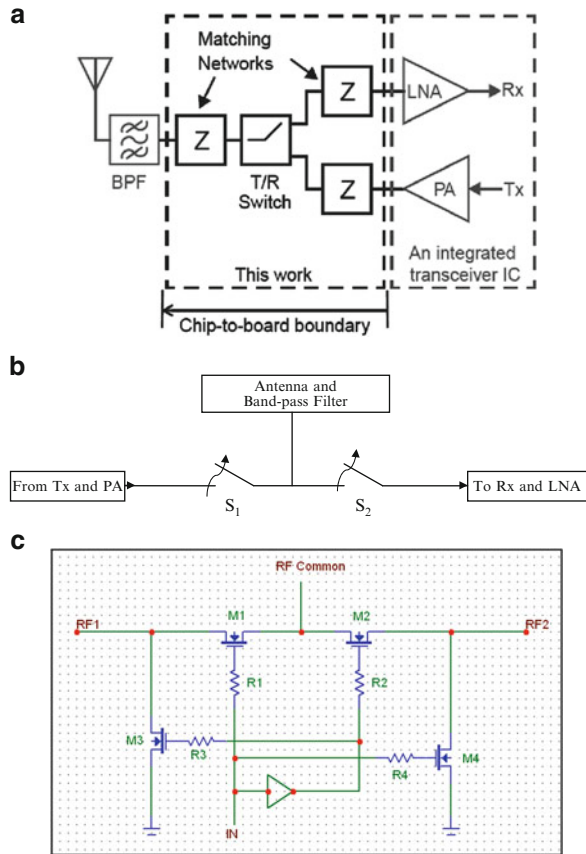
2.3 RF Transceiver Systems

A superheterodyne RF transceiver architecture contains a few blocks which are implemented off-chip, as shown in Fig. 2.2a. This includes the antenna, preselection band-pass filter, intermediate frequency filter, and transceiver switch. While efforts are being made to integrate these blocks on a single chip using standard CMOS technologies [19–21], the quality factor of on-chip inductors and the substrate parasitics of MOSFETs are also very important limiting factors.

Earlier, the reported literatures [3, 22] suggest that receivers are being integrated from the low-noise amplifier onwards while the transmitters are integrated up to the power amplifier. An integrated transceiver switch which includes matching networks for the low-noise amplifier and power amplifier will push the integration boundary further towards the antenna as shown in Fig. 2.2a. However, such an improvement also decreases board component count and hence total cost. Therefore, the transceiver switch is a desirable, as well as a suitable candidate for evaluating the impact of the inductive substrate bias technique.

The purpose of a transceiver switch is to alternately couple the antenna to either the transmitter or the receiver and to protect the receiver while transmitting high power.

Fig. 2.2 A radio front-end block diagram with (a) the integration of transceiver switch and matching networks, (b) simplified schematic of a transceiver switch, and (c) typical transistor based transceiver switch [22]



The effect of integrating the transceiver switch is to push the chip-to-board boundary closer to the antenna. A simple schematic of a transceiver switch is shown in Fig. 2.2b. The switch operates in either the transmit (T_x) mode, in which power is transmitted from the power amplifier (PA) to the antenna, or in the receive (R_x) mode, when power is delivered from the antenna to the LNA [23–25].

These two switches, S_1 and S_2 , are operated by using opposite phases of control signal (V_{ctrl}), thereby ensuring that the antenna is connected to either the LNA or the PA, but not both. Ideally, for all input power levels, the S_1 switch and S_2 switch would be perfect “short-circuited” with zero impedance when closed and perfect “open-circuited” with infinite impedance when the contacts are separate or open. To improve their bandwidth, wideband switches use only n-channel MOSFETs in the signal path. An n-type MOSFET switch has a typical -3 dB bandwidth of 400 MHz, almost twice the bandwidth performance of a standard switch with n-type MOS transistor and p-type MOS transistor in parallel. This is a result of the smaller switch size and greatly reduced parasitic capacitance due to removal of the

p-channel MOSFET. The n-channel MOSFETs act essentially as voltage-controlled resistors. The switches operate as follows:

$$V_{gs} > V_{th} \rightarrow \text{Switch ON}$$

$$V_{gs} < V_{th} \rightarrow \text{Switch OFF}$$

where V_{gs} is the gate-to-source voltage and V_{th} is defined as the threshold voltage above which a conducting channel is formed between the source and drain terminals. As the signal frequency increases greater than several hundred MHz, parasitic capacitances tend to dominate. Therefore, high isolation in the switch OFF-state and low insertion loss in the switch ON-state can be achieved. For the wideband applications, it is a quite challenging task for the switch designers. The channel resistance of a switch should be limited to less than about $6\ \Omega$ to achieve a low-frequency insertion loss of less than 0.5 dB on a line with $50\ \Omega$ matched impedances at the source and load [24, 26, 27].

2.4 RF Transceiver Switch

For transmitting process, as the voltage V_1 goes high (+5 V or high level) and voltage V_2 goes low (–5 V or low level), then these condition turns transistor M_1 and transistor M_4 in ON-state and transistor M_2 and transistor M_3 in OFF-state. For receiving process, as the voltage V_1 goes low (–5 V or low level) and voltage V_2 goes high (+5 V or high level), then these condition turns transistor M_1 and transistor M_4 in OFF-state and transistor M_2 and transistor M_3 in ON-state. Transistor M_3 and transistor M_4 shunt the signal in receive and transmit mode, respectively, and thus increase the isolation. Capacitance C_1 and C_2 allow DC biasing of the transmitting and receiving nodes. The purpose of resistance R_1 , R_2 , R_3 , and R_4 is to improve DC bias isolation and has a value of about 10 k Ω . This circuit has very good isolation in OFF-state but suffer from high loss in ON-state because of the shunt transistors. It also has nonlinear properties when the power of the signal increases.

The FETs have an interlocking finger layout that reduces the parasitic capacitance between the input (RF_X) and the output (RF_C), thereby increasing isolation at high frequencies and enhancing cross talk rejection. For example, when M_1 is ON to form the conducting path for RF_1 , M_2 is OFF and M_4 is ON, shunting the parasitics at RF_2 to ground, as shown in Fig. 2.2c. In the normal operation, the switches can handle a 7 dBm (5 mW) input signal. For a $50\ \Omega$ load, this corresponds to a 0.5 V rms signal or 1.4 V peak to peak for sine waves. The power handling capability is reduced at lower frequencies for the following two reasons:

- a. Since the n-type MOSFET structure consists of two regions of n-type material in a p-type substrate. Parasitic diodes are thus formed between the n and p regions. When an AC signal, biased at nearly zero volts DC, is applied to the source of the

transistor, and V_{gs} is large enough to turn the transistor ON ($V_{gs} > V_{th}$), the parasitic diodes can be forward biased for some portion of the negative half-cycle of the input waveform. This happens if the input sine wave goes below approximately 0.6 V, and the diode begins to turn ON, thereby causing the input signal to be clipped (compressed).

- b. The less power handling capability at lower frequencies is the partial turn-ON of the shunt n-type MOSFET device when it is supposed to be OFF. This is very similar to the mechanism described above where there was partial turn-ON of parasitic diode. In this case, the n-type MOSFET transistor is in the OFF-state, by the way of $V_{gs} < V_{th}$. With an AC signal on the source of the shunt device, there will be a time in the negative half-cycle of the waveform, where $V_{gs} > V_{th}$, thereby partially turning ON the shunt device. This will compress the input waveform by shunting some of its energy to ground [31, 32].

In the communication systems, to transmit or receive the information through multiple antennas such as multiple-input and multiple-output (MIMO) systems, it is essential to design a novel RF switch that is capable of operating with multiple antennas and frequencies as well as minimizing signal distortion and power consumption [28–30]. The Si-CMOS for this application allows the higher levels of integration and lower cost as well as improvement in the efficiency. In a switch, the modulated signal is simply transmitted through the switch and makes its way to the antenna for releasing into the space. On the other hand, the modulated signal is received by the antenna and makes its way through the switching path to the receiver. Currently, the CMOS technology is almost capable to take overall functionalities of radio-frequency circuitry.

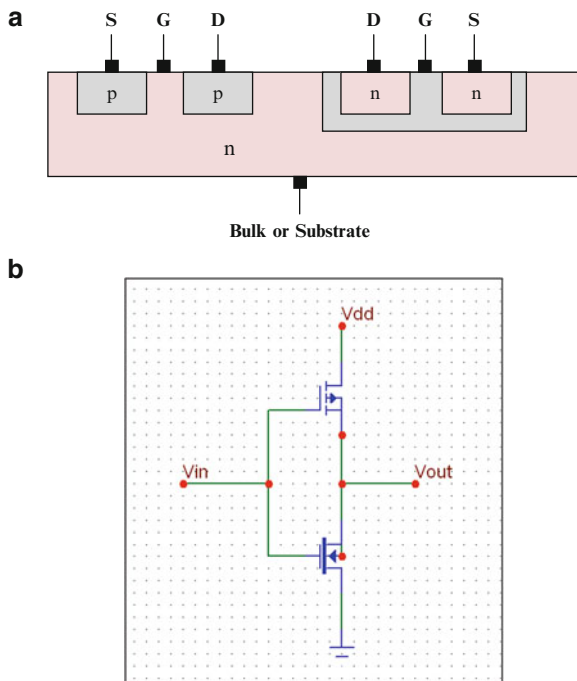
2.5 Design of CMOS Inverter for RF Switch

The CMOS-based technology is the main contributor to reducing significantly the switching time in digital circuits and high-speed performance of the analog electronics. The low-power dissipation and integrability on a single chip made this a demanding technology. Compared to the single-transistor gate logic which consists of n-type MOS transistor with a resistor pull-up and the BJT-based TTL, the CMOS established a new paradigm for low power consumption and high operating speed. The new advances in MOSFET technologies such as double-gate, gate-all-around, and FinFET are the most promising configurations. In this book we have discussed about the double-gate MOSFET and a new proposed design of cylindrical surrounding double-gate MOSFET.

The reason for the success of Silicon MOSFET technology is the development of CMOS logic, because this technology provides both n-channel and p-channel MOSFET. The basic MOSFET has four terminals:

- a. Source
- b. Drain

Fig. 2.3 Schematic of the CMOS (a) internal structure and (b) inverter circuit [31]



- c. Gate
- d. Bulk

Figure 2.3 shows the cross-sectional view of a typical CMOS process. In the n-type MOS transistor, if the voltage on the gate increases, the majority carriers (holes) will be pushed away towards substrate and have been depleted as gate voltage continues to increase. Eventually, generations of carriers will exceed the recombination. The generated hole–electron pairs are separated by the field, the holes being swept into the bulk and the electrons moving to the oxide–silicon interface, where they are held, because of the energy barrier between the conduction band in the silicon and that in the oxide. When a drain-to-source voltage is imposed, the current will flow in the channel. As the drain-to-source voltage (V_{ds}) increases, the current also increases. However, beyond a certain drain-to-source voltage, the current will saturate.

The p-channel MOSFET relies on n-type substrate. As commonly p-type wafers are used for processing, an additional n-type well implant is necessary. In this well, which is a deep region of n-type doping, the p-channel MOSFET is placed. As the p-substrate and the n-well junction are reverse biased, therefore no significant current flows between these regions and the two transistors are isolated as shown in Fig. 2.3a. The output current of the p-channel MOSFET is typically much lower

than the current of an n-channel MOSFET with similar dimensions and doping. This is due to the lower carrier mobility of holes compared to electrons. As the characteristics of the complementary transistors should be as equal as possible, the width of the p-channel MOSFET is typically made larger to compensate the difference. We have taken the geometry factor (ratio of p-type MOSFET to n-type MOSFET) equal to 3.5 to obtain the equal drain currents for equal gate biases of the device [31].

In the stationary case as in Fig. 2.3b, the circuit does not consume any power when assuming perfect devices without leakage current. It can be seen that the gates are at the same bias V_{in} which means that they are always in a complementary state. When V_{in} is high, $V_{in} \approx V_{dd}$, the voltage between gate and substrate of the n-type MOS transistor is also approximately V_{dd} and the transistor is in ON-state. The gate–substrate bias at the p-type MOS transistor on the other side is nearly zero and the transistor is turned OFF. The output voltage V_{out} is pulled to ground, which is the low state. When V_{in} is low $V_{in} \approx 0$, the complementary situation occurs and the p-MOSFET is turned ON, while the n-type MOSFET is turned OFF. The output voltage is, therefore, pulled to V_{dd} which is the high state. It is important to note that in both states, high and low, no static current flows through the inverter. This is valid when assuming ideal devices with zero OFF-current and leakage current [27, 32]. Considering the negative bias temperature instability, the worst stress conditions are imposed on the p-channel MOSFET at $V_{in} = V_{low}$. At this bias condition the p-type MOSFET is turned ON, with approximately the same potential at the source and the drain $V_{gs} = V_{gd} = V_{dd}$ and negative gate-to-substrate voltage $V_{gsub} = -V_{dd}$.

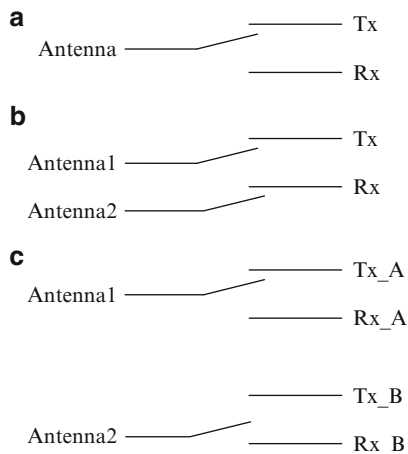
2.6 Configuration of Switches

The RF switch is one of the key functional building blocks. There is a new trend to employ the CMOS technique to control the conducting path between transmitter/receiver circuit and antenna. By this way, it will be helpful to the integration of RF switch with CMOS transceiver circuit, reducing the overall cost of the chipset [33, 34]. There are several types of RF switches, which have been classified as follows.

2.6.1 Single-Pole Single-Throw Switch

The single-pole single-throw (SPST) switch plays an important role in communication and radar systems. It can be used as an individual component or an integral element in subsystems or systems, for example, in RF pulse transmitters [2]. For high data rate short-range communication and some high-resolution radar systems, the SPST switches used for the transmitters pulse formation with fast switching time and high isolation including low insertion loss. Among these characteristics,

Fig. 2.4 Schematic of the (a) SPDT, (b) DPDT, and (c) DP4T



the high isolation is especially a crucial in order to reduce or prevent RF leakage [24, 26, 27]. However, the undesired RF leakage not only causes external effects, such as harm to other coexisting systems, but also internal effects such as reduced dynamic range.

2.6.2 Single-Pole Double-Throw Switch

The single-pole double-throw (SPDT) switch is the fundamental switch that links between one antenna and the transmitter/receiver as shown in Fig. 2.4a. In time division duplexing (TDD) communication systems, transmitter/receiver switch plays an important role to change the RF signal flow to the transmitter or receiver. Further, to increase the integration level, the SPDT switch has to be integrated in the transceiver. The advantages of silicon CMOS technology for RF and microwave control functions over GaAs are its low cost and the integration potential with RF and silicon MOS-based mixed-signal circuitry [27].

Due to the limitations of the CMOS process and circuit topology, the frequencies of most reported CMOS RF switches are lower than 5.8 GHz [28]. The conventional topology for CMOS switch is series shunt, which is only suitable for narrow band design. It demonstrates the power performance of a CMOS switch, but the LC-tuned substrate bias network limits the frequency response. For broadband frequency response, a switch using 0.13- μm CMOS process based on traveling wave concept is reported [35]. The switch consist of the OFF-state shunt transistors and series micro-strip lines to form an artificial transmission line with 50 Ω characteristic impedance and achieve wide bandwidth.

Recently, Quemerais et al. [36] have proposed a fully integrated SPDT transceiver switch, which has been implemented on a standard 45-nm CMOS process.

This circuit is dedicated to fully integrated CMOS front-end modules operating at GHz range. Dinc et al. [37] have proposed an SPDT transceiver switch for X-band on-chip radar applications. These methodologies include the optimization of transistor widths for significantly lower insertion loss, while preserving high isolation and using a parallel resonance technique to improve the isolation. Also, the techniques such as applying DC bias to the source and the drain, using on-chip impedance transformation networks and the body floating are used to improve the power handling capability of the switch. Lei et al. [38] have designed an SPDT switch in a partially depleted (PD) SOI CMOS process for 2.4 GHz wireless communication applications. However, based on the advantage of PD SOI device structure, the presented switch demonstrates the high performance on insertion loss and isolation. Maisurah et al. [39] have designed SPDT transceiver switch for 900 MHz frequency applications with a 0.18- μm CMOS process. Mekanand et al. [29] have proposed a transceiver CMOS switch for 2.4 GHz with low insertion loss and excellent control voltage [40, 41]. These simulation results of CMOS switch design demonstrate an insertion loss of 1.102 dB for receiving mode and 1.085 dB for transmitting mode. However, both the modes can operate using a control voltage of only 1.2 V.

2.6.3 Double-Pole Double-Throw Switch

The SPDT is the fundamental switch that links between antenna and the analog front-end section but due to the single operating frequency. This type of switch has a limited data transfer rate. Therefore, a double-pole double-throw (DPDT) switch is developed to solve the aforementioned problem as shown in Fig. 2.4b. The preferred DPDT switch is the back-to-back structure, which combines the common ports of conventional SPDT switches because it has only one device between four ports. Hence this reduces the insertion loss by half as compared to the SPDT that has two devices in each signal path. In the wireless communication systems, the demand for $n \times m$ switch matrices is increasing significantly for the antenna diversity. The general switching matrix has the disadvantage of the need for large number of switching devices and complicated control logic. These DPDT switches has dual antenna and dual ports, one for transmitting and another for receiving, which is not sufficient for MIMO systems [42]. Hence, we have designed a double-pole four-throw (DP4T) switch to enhance the switch performance for MIMO communication applications.

2.6.4 Double-Pole Four-Throw Switch

This double-pole four-throw (DP4T) switch can send or receive two parallel data streams simultaneously as shown in Fig. 2.4c [5]. The switch with the CMOS inverter technology is shown in Fig. 2.5 to design a novel DP4T switch and then

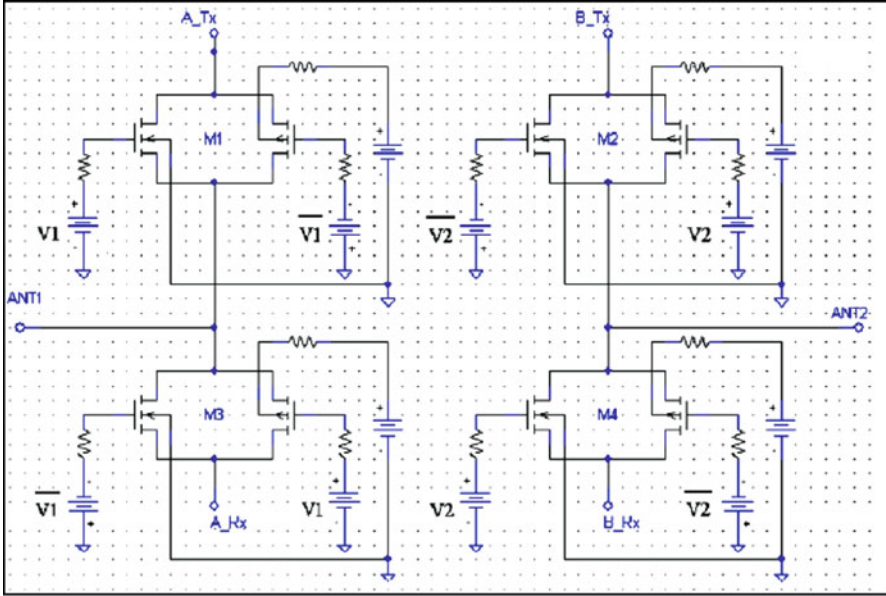


Fig. 2.5 DP4T CMOS transceivers switch with single-gate transistor

design this DP4T switch using the double-gate (DG) MOSFET in the following chapters. Its performances, such as insertion loss, control power, and signal distortion, are compared with a traditional n-type MOSFET DP4T switch in terms of single-gate and double-gate [27, 40, 41].

2.7 Design of DP4T RF Switch Based on Single-Gate MOSFET

Already existing designs of the DP4T switches use the single-gate n-type MOSFET [29] and require a high control voltage from 3.0 to 5.0 V to operate, and a large internal/contact resistance and capacitances are produced for this design at the receivers, transmitters, and antennas for detecting the data signal as shown in Fig. 2.5. This high value of control voltage is not suitable for modern low power portable devices which require smaller power consumption of about 0.5–2.1 V. Therefore, we have proposed a novel DP4T switch using DG CMOS technology for the purpose of RF application [42, 43].

The objective of the proposed design of a switch is to operate at 2.4 and 5.0 GHz for MIMO systems. This switch mitigates the attenuation of the passing signals and exhibits high isolation to avoid interruption of the simultaneously received signals [29]. Since in Fig. 2.5, four transistors are used for first antenna, the working process

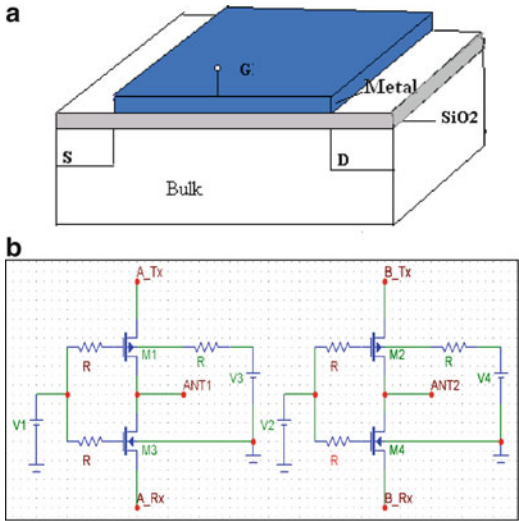


Fig. 2.6 Schematic of the (a) basic SG MOSFET and (b) DP4T SG RF CMOS switch

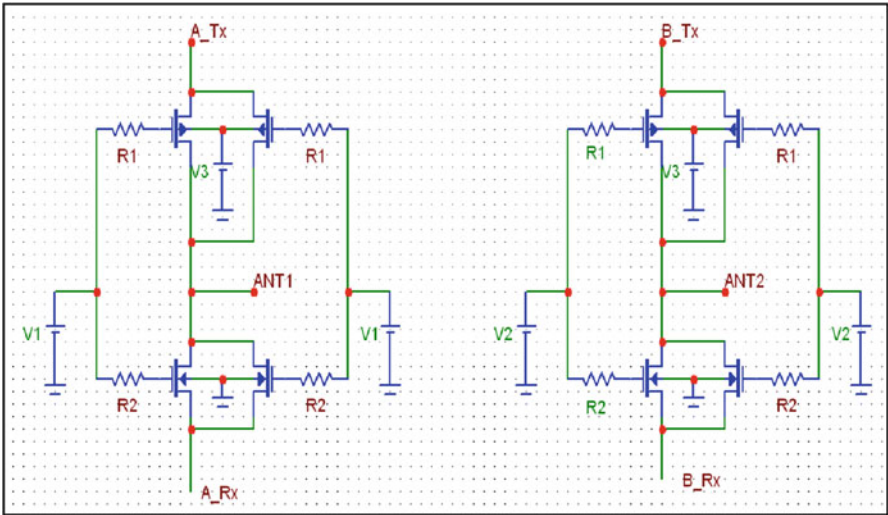


Fig. 2.7 Proposed DP4T switch with two transistors

at a time any one of transistor M_1 or transistor M_3 will operate and in the same fashion any one of transistor M_2 or transistor M_4 will operate. Similar working function is observed in the proposed DP4T CMOS switch as in Figs. 2.6b and 2.7.

A double-pole four-throw double-gate radio-frequency complementary metal-oxide-semiconductor (DP4T DG RF CMOS) switch has the properties as fixed-tuned matching networks, low quality factor, high output power, power gain, or

power amplification, noise figure or amount of noise added during normal operation, and high-power dissipation (total power consumption). Some bipolar RF CMOS transistors are suitable for automotive, commercial, or general industrial applications [43, 44]. To design the DP4T switch based on the DG MOSFET, first we design the DP4T switch in the present chapter with the two parallel transistor technique and then designed the DG MOSFET as in Chap. 3 and at last combine the both technology to design the proposed model of DP4T DG RF CMOS switch in Chap. 4.

The choice of RF CMOS switch requires an analysis of the performance parameters such as maximum drain saturation current, operating frequency, cut-off frequency, threshold voltage of n-type MOSFET and p-type MOSFET, control voltage, output power, and forward transconductance [45]. It also controls the increase or decrease of channel lengths for the devices which operates in depletion region. The DP4T switch is a fundamental switch for the application of multiple-input, multiple-output data transfer. So, the parallel data streams can be transmitted or received simultaneously using the multiple antennas.

2.8 Operational Characteristics of DP4T CMOS Switch

Figure 2.5 shows the existing DP4T CMOS transceiver switch with single-gate (SG) transistor [29]. Here two antennas and four ports are taken into account. Figure 2.6a shows the SG MOSFET structure. In Fig. 2.6b, the transmitted signal from power amplifier is sent to transmitter “A” named as “A_{Tx}” port and travel to the ANT₁ node while the received signal will travel from the ANT₂ node to the receiver “B” named as “B_{Rx}” port and pass on to the low-noise amplifier (LNA) or any other application as required for transceiver systems. The proposed switch contains CMOS in its architecture and needs only two control lines (V_1 , V_2) of 1.2 or 2.1 V to control the signal congestion between two antennas and four ports; therefore, it improves the port isolation performance two times as compared to the DPDT switch and reducing signal distortion. Since connecting an n-type MOSFET in series with a p-type MOSFET allows signals to pass in either direction as shown in the Fig. 2.7. Whether the n-type or p-type device carries more signals current depends on the ratio of input to output voltage because the switch has no preferred direction for the current flow, so it has no preferred input or output terminals.

When the low voltage (approximately zero volts) is applied at the input of Fig. 2.3b, the top transistor (p-type) is conducting (switch closed) while the bottom transistor behaves like an open circuit. Therefore, the supply voltage (5 V) appears at the output. Conversely, when a high voltage (5 V) is applied at the input, the bottom transistor (n-type) is conducting (switch closed) while the top transistor behaves like an open circuit. Hence, the output voltage is low (0 V). It is important to note that always one of the transistors will be an open circuit and no current flows from the supply voltage to the ground [46, 47]. The voltage transfer characteristic gives the response of the DP4T inverter switch circuit with the antennas (ANT₁ and ANT₂)

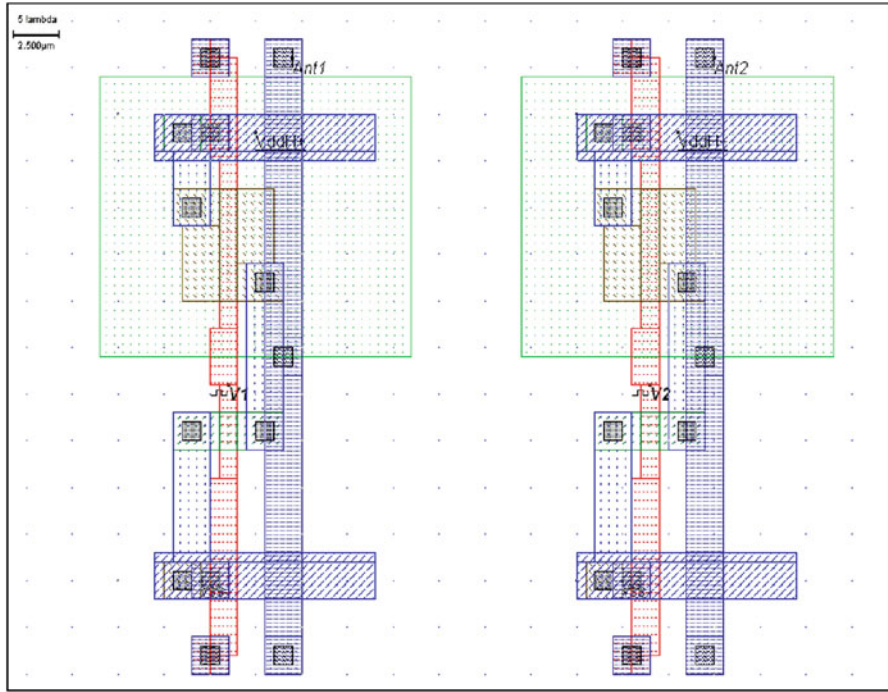


Fig. 2.8 Proposed DP4T switch layout with two transistors

and the specific input voltages V_1 and V_2 . The gate-to-source voltage V_{gs} of the n-type MOSFET is equal to V_{in} , while the gate-to-source voltage of the p-type MOSFET is $V_{gs}^p = V_{in} - V_{dd}$, and the drain-to-source voltage of the p-type MOSFET is $V_{ds}^p = V_{ds}^n - V_{dd}$. From the output characteristics of the two transistors, the resulting drain currents in inverter circuit must be equal for each V_{in} and considering that the drain currents I_d of both the transistors must be equal, the voltage transfer characteristic is extracted from the layout of DP4T CMOS switch, as shown in Fig. 2.8. From this layout, it is obvious that when p-type MOSFET is ON, then ANT₁ and ANT₂ are connected to the A_T_x and B_T_x, respectively, which are shown here with the 5 V or V_{dd} . Similarly when the n-type MOSFET is ON, then ANT₁ and ANT₂ are connected to the A_R_x and B_R_x, respectively.

2.9 RF Switch Performance Parameters

The switches turn RF power ON and OFF, or perform high-frequency signal routing. The electrical parameters which have been measured and observed in this chapter exhibited by a switch are as follows.

2.9.1 Insertion Loss

The insertion loss is the loss of signal energy and power due to the insertion of a device in the transmission line (it may be optical fiber or LAN). The insertion loss of RF switch is the RF loss dissipated in the device and it is measured by S_{21} (in two-port device) between the input and output of the switch in its switch ON-state, which is the closed state for a series switch [48]. It may also be expressed as the reciprocal of the ratio of the signal power delivered to that part of the line following the device to the signal power delivered to that same part before insertion. The main contributing factors include resistive loss of the signal lines, contact at low to medium frequencies, and loss due to the skin depth effect where skin depth stands for the depth at which the electric current flows, measured from the surface of conductor.

2.9.2 Return Loss

The return loss is the loss of signal energy/power resulting from the reflection caused at a discontinuity in the transmission line (it may be optical fiber or LAN). This discontinuity can be a mismatch with the terminating load or with a device inserted in the line. The return loss of RF switch refers to the RF loss reflected back by the device means that portion of a signal that cannot be absorbed by the switch, or cannot cross an impedance mismatching due to the switch. This component of the signal is reflected from the impedance mismatching and returns back from that point and it is measured by S_{11} at the input of the switch in its switch ON-state. The main contributing factors include the mismatch of the switch's total characteristic impedance [48].

2.9.3 Isolation

The isolation of RF switch refers to the RF isolation between the input and output and it is measured by S_{21} of the switch in its blocking state, which is the OFF-state for a series switch. The main contributing factors include capacitive coupling and surface leakage [32].

2.9.4 RF Power Handling

This is a measure of how much and how well a switch passes the RF signal. To quantify RF power handling, the 1 dB compression point is commonly specified. That point is a measure of the deviation from the linearity of the 1 dB output power

with respect to the input power. Alternatively, in pulsed power operation conditions, the peak pulsed power, the repetition rate, and the duty cycle are specified. In the switches containing P–N junctions, power handling is a function of frequency [8].

2.9.5 Linearity

If the ratio of a switch's output power to input power is a function of the input power level, then the switch is said to behave as a nonlinear device [9]. When signals of various frequencies are passed through the switch at a time, then in addition to the input frequencies, the switch's output will also contain frequencies related to the sum and difference of the harmonics of the various input frequencies. It is defined as input third-order intercept point (IIP_3) and output third-order intercept point (OIP_3).

2.9.6 Transition Time

Transition time is basically the time required for RF voltage to increase from 10 to 90 % (sometimes 0–100 %) for ON-state or decrease from 90 to 10 % (sometimes 100 to 0 %) for OFF-state.

2.9.7 Switching Speed

Switching speed is the time required for the switch to respond at the output upon applying of input voltage or changes in input voltage level. Switching speed includes drive propagation delay as well as transition time and is measured from the 50 % point on control voltage to 90 % for ON-state or 10 % for OFF-state of the RF voltage.

2.10 Topologies for DP4T Switches

At the high frequencies signal degradation occurs due to power dissipation in the line and power loss due to reflections in the transmission line. In a typical RF system, the switch network consists of multiple modules and cables. These networks may be constructed in various arrangements with modules of varying topologies. This topology is one of the most important features to consider when selecting an RF switch. Selecting a switch with the wrong topology can cause considerable effects on

switching speed, propagation delay, insertion loss, and voltage standing wave ratio (VSWR).

With the growing degree of integration in the wireless communication systems, the test of RF front-end circuit is becoming more difficult. The high cost of test equipment and complexity of test procedure are becoming problems to be considered carefully by designers. In order to improve these problems, the idea of design for testability is introduced. In this case, the built-in self-test technology is implemented with an additional circuitry to the front-end chip. With this technology, the complete chip can be tested without external equipment. To test the switch circuit, two main types of topologies available for RF are multiplexers and SPDT relays [43].

- a. A multiplexer is a switching system that sequentially routes various inputs to one output or vice versa. It is an ideal for reducing the channel count of RF devices such as analyzers and generators [47]. An application of multiplexer would be on the production floor to test the functionality of a mass produced RF device such as an integrated circuits or cell phones. In a case of batch of 1,000 device test, it would be cost prohibitive to dedicate an RF analyzer for the testing of each individual cell phone as this would require 1,000 RF instruments which increase the losses interns of power (energy) and delay in analyzing. Another way to conduct this test would be to manually route all 1,000 devices, one at a time, to a single RF instrument. This route would be more affordable than having multiple RF instruments. It reduces the test time significantly. The better test for this particular process would be to build an automated RF test system that uses a $1,000 \times 1$ multiplexer to route 1,000 devices to the RF analyzer which takes a measurement.
- b. An SPDT relay is a basic form of multiplexer. This relay can route two inputs to one output or vice versa. General-purpose RF relay modules are usually made up of SPDT relays and are used to route a signal between two places [49]. For example, if a signal needs to be analyzed using an RF analyzer and then broadcasted to two locations through an antenna [50, 51], it can be routed to both locations using an SPDT relay.

The proposed DP4T switch can route four inputs to two outputs at a time or vice versa. So it is twice effective as compared to the existing SPDT switches as shown in Fig. 2.7.

2.11 Conclusions

The DP4T switch is designed with low insertion loss and low control voltage. The advantage of this switch is its minimum distortion and negligible voltage fluctuation, and it does not require large resistance at the receiving end. The proposed DP4T switches can be easily implemented into MIMO systems to increase the diversity and system capacity due to the multiple antenna usage. For the low-power

circuits, a favorable condition can be achieved when both transistor gates are on the same potential contribution, even a reduced amount of leakage current. The proposed DP4T RF switch design with two parallel MOSFET modifies a conventional analog switch circuit design to operate with digital signals to achieve isolation buffering for bidirectional signals and high-density packing of multiple buffer switches operating under single enable control in a single package. However, certain modifications to a conventional analog switch design that facilitate the use of present switch in high-speed digital switching applications provide rapid switching times between ON-state and OFF-state, a low ON-resistance of less than $25\ \Omega$, high-density configuration of multiple switches, and the ability to control the switches with standard logic level signals.

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MOSFET Technologies for Double-Pole Four-Throw

Radio-Frequency Switch

Srivastava, V.M.; Singh, G.

2014, XV, 199 p. 55 illus., 45 illus. in color., Hardcover

ISBN: 978-3-319-01164-6