

Chapter 2

An I/O Line Configuration and Organization of DRAM

2.1 DRAM Core Access Speed

For state-of-the-art DRAM, the core operating speed is around 200 Mb/s. However, data is transferred by 7 Gb/s/pin for GDDR5 [1–3]. This is possible because pre-fetch scheme is employed. In this session, we explain the pre-fetch scheme and global IO configuration for understanding speed limits restricted by DRAM core operation.

2.1.1 DDR1

Figure 2.1 shows a gapless read operation in DDR1 [4]. Burst length of DDR1 is two. It means two data bits are sequentially output from the memory for one read operation. CAS to CAS delay of DDR1 is one clock period. This means the minimum gap between CAS to CAS commands is one clock period. Therefore, DDR1 outputs two data bits in one clock read operation. As mentioned earlier, DRAM core has a speed limitation due to the various capacitive loads and sensing operation of bit line sense amplifier. So, to get around this problem, DDR1 reads two data bits at the same time. The two data bits that are read out from cell array simultaneously is called ‘pre-fetched data’. As a result, the number of GIO (Global I/O) can be calculated by the required burst length multiplied by the number of DQ. As explained earlier, the number of GIO channels is the number of pre-fetch bits multiplied by the number of DQ as shown in Fig. 2.2. And the core operation speed is half of the output data rate for DDR1. For example, if the output data rate is 400 Mb/s, the internal data rate is 200 Mb/s.

2.1.2 DDR2

This timing diagram of Fig. 2.3 shows a gapless read operation in DDR2 [5]. The burst length of DDR2 is four. It means four consecutive data bits are output from the memory for one read operation. CAS to CAS delay of DDR2 is two clock cycles. The tCCD is doubled compared with DDR1 in terms of clock cycles. But DDR2

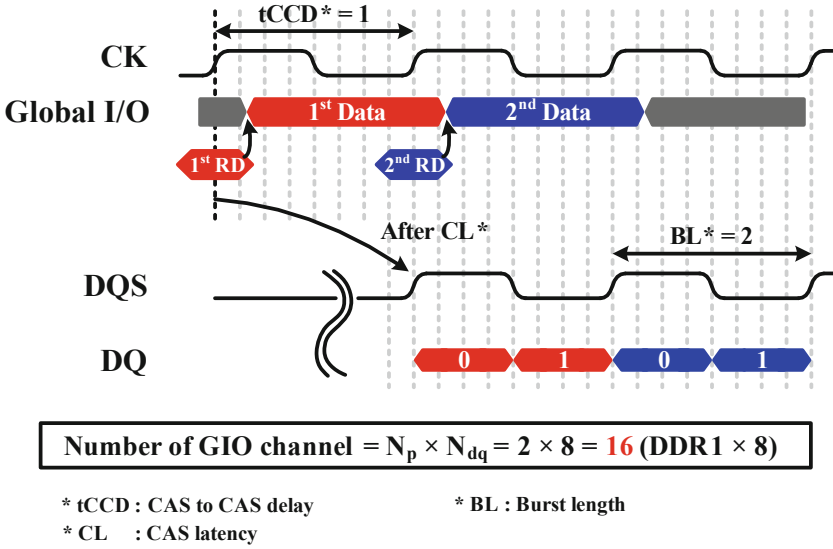
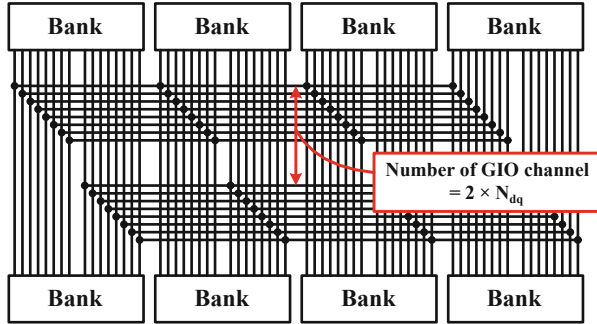


Fig. 2.1 Timing diagram of read operation for DDR1

Fig. 2.2 Configuration of pre-fetch and GIOs connection for DDR1



clock speed is twice as fast as DDR1. DDR2 reads four data bits from cell array at the same time. As a result, the number of GIO is the necessary burst length multiplied by the number of DQ. DDR2 needs four data reading at the same time. So DDR2 needs four GIO channels for each DQ. And the core operation speed is quarter of the output data rate. So if the output data rate is 800 Mbps, the internal data rate is 200 Mbps. The internal data rate of DDR2 is the same as DDR1. The configuration of pre-fetch and GIOs connections for DDR2 is shown in Fig. 2.4.

2.1.3 DDR3

This timing diagram of Fig. 2.5 represents a gapless read operation in DDR3 [6]. The burst length of DDR3 is eight. That means eight consecutive data bits come

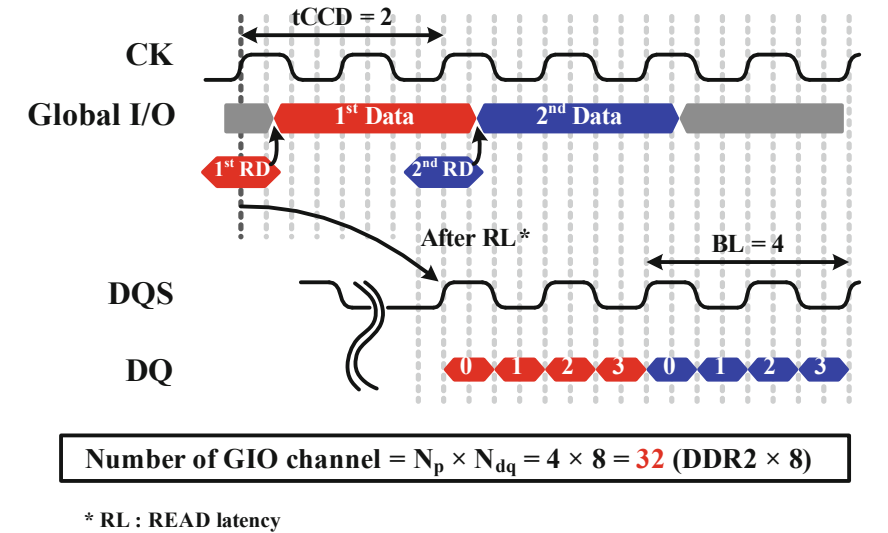
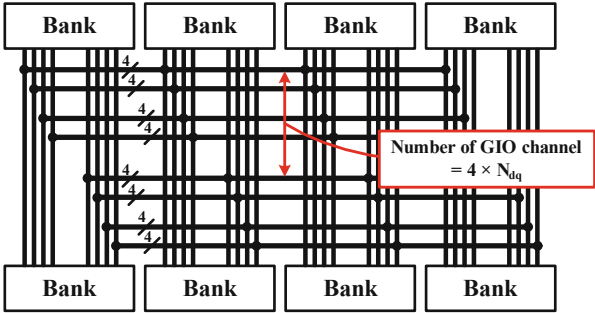


Fig. 2.3 Timing diagram of read operation for DDR2

Fig. 2.4 Configuration of pre-fetch and GIOs connection for DDR2



from the memory for one read operation. CAS to CAS delay of DDR3 is four clock cycles. The t_{CCD} is doubled compared to DDR2 in terms of clock cycles. DDR3 clock speed is twice as fast as DDR2. Even though the eight bits consecutive data are not required, DDR3 reads eight data at the same time. In order to chop the burst data, DDR3 supports the burst chop function. So, you can clearly see the trend. To increase the data rate, the number of pre-fetched bits is increased. The configuration of pre-fetch and GIOs connections for DDR3 is shown in Fig. 2.6.

Unfortunately, the number of GIO channels is increased by the same factor as well. This increase in GIO channels causes the channel area to increase. It is a major disadvantage of the pre-fetched scheme.

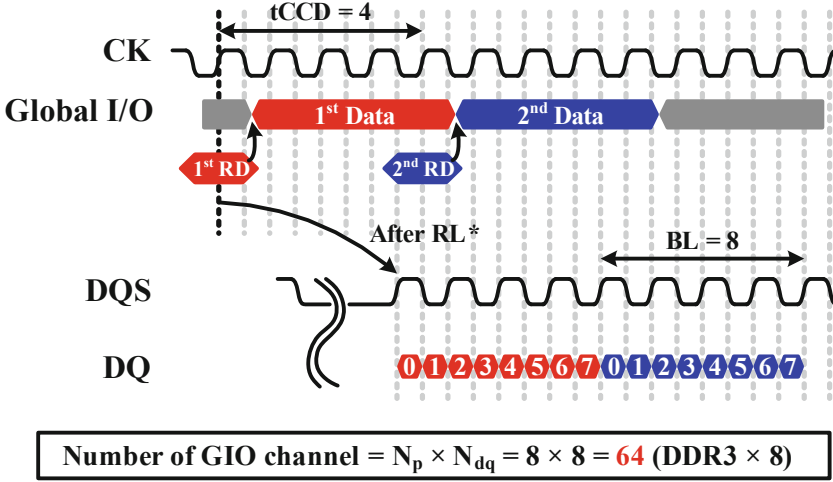
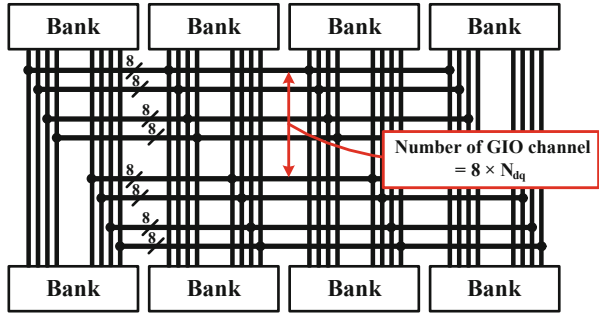


Fig. 2.5 Timing diagram of read operation for DDR3

Fig. 2.6 Configuration of pre-fetch and GIOs connection for DDR3



2.1.4 DDR4

Finally, Fig. 2.7 illustrates a gapless read operation in DDR4 [7–8]. If we follow the previous trend in burst length, the burst length of DDR4 should be 16. But too large of a burst length is inefficient for data processing. So, the burst length is fixed to eight, the same as DDR3. Due to the core speed limitation, you can see a one clock period gap between gapless read operations when t_{CCD} of DDR4 is five. To get rid of this wasted time, a bank group architecture is adopted in DDR4 [9]. The bank group architecture is a very simple idea. The banks that are in the same bank group share the GIO channel. If the interleaving read is applied and each access bank is not in the same bank group, the output data can be transferred to each GIO channel in time. So the output data bits do not collide and the gap of interleaving read can be reduced so that t_{CCD} is four. This bank group interleaving access helps to get rid of wasted time. Therefore, DDR4 has two different CAS to CAS delays, t_{CCD_S} (t_{CCD} Short) and t_{CCD_L} (t_{CCD} Long). t_{CCD_S} is the gap of interleaving read command from different bank groups. t_{CCD_L} is the gap of interleaving read command from the

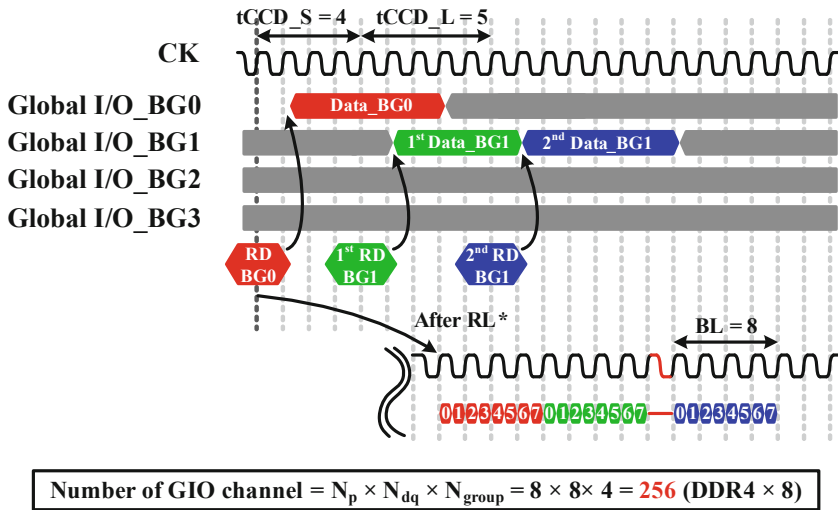


Fig. 2.7 Timing diagram of read operation for DDR4

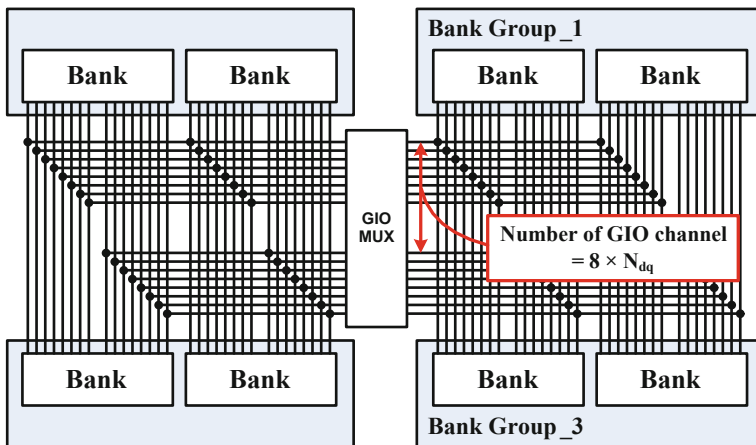


Fig. 2.8 Configuration of pre-fetch and GIOs connection for DDR4

same bank group. Figure 2.8 is a pre-fetch and bank grouping diagram of DDR4. There are no rules as far as how to group the banks. Each channel of a bank group is connected to GIO_MUX, and the GIO_MUX selects the suitable channel.

2.2 Organization of DRAM

In general, it is possible to categorize the DRAM based on their types and applications. DRAM has different features for different applications. We briefly look into their unique features according to their types.

Table 2.1 Differences of DDRx, GDDRx, and LPDDRx

	GDDRx	DDRx	LPDDRx																				
Architecture	<table><tr><td>Bank</td><td>Bank</td></tr><tr><td colspan="2">PAD</td></tr><tr><td>Bank</td><td>Bank</td></tr></table>	Bank	Bank	PAD		Bank	Bank	<table><tr><td>Bank</td><td>Bank</td></tr><tr><td colspan="2">PAD</td></tr><tr><td>Bank</td><td>Bank</td></tr></table>	Bank	Bank	PAD		Bank	Bank	<table><tr><td colspan="2">PAD</td></tr><tr><td>Bank</td><td>Bank</td></tr><tr><td>Bank</td><td>Bank</td></tr><tr><td colspan="2">PAD</td></tr></table>	PAD		Bank	Bank	Bank	Bank	PAD	
Bank	Bank																						
PAD																							
Bank	Bank																						
Bank	Bank																						
PAD																							
Bank	Bank																						
PAD																							
Bank	Bank																						
Bank	Bank																						
PAD																							
Socket	On board	DIMM	MCP*/PoP*/SiP*																				
IO	×16 / ×32	×4 / ×8	×16 / ×32																				
Application	Graphic card	PC/Server	Phone/Consume																				
Application	<ul style="list-style-type: none">• Single uni -directional WDQS , RDQS• VDDQ termination• CRC , DBI• ABI		<ul style="list-style-type: none">• No DLL• DPD *• PASR *• TCSR *																				

* MCP: Multi chip package

* PoP : Package on package

* SiP : System in package

* DPD : Deep power down

* PASR: Partial array self refresh

* TCSR: Temperature compensated self refresh

2.2.1 Differences of DRAM Type

Table 2.1 shows the differences in the three types of DDR. The pad locations of DDR and GDDR are in the center of the chip. On the other hand, LPDDR has pads at edge of the chip due to the different package type. It is good to make multi chip package. LPDDR is normally not packaged alone. So it has an edge pad layout for multi-chip package. Each type of memory has unique features. GDDR is optimized for high speed and large bandwidth. So GDDR has x16 or x32 IO and cyclic redundancy check (CRC) feature. LPDDR is optimized for low power consumption. So LPDDR does not use DLL and supports various functions for lower power consumption such as deep power down mode, partial self-refresh and temperature compensated self-refresh. Recently developed DDR4 has gear down mode, CRC and DBI features for high-speed operation and TCSR for low power. Hence, the differences among DDR, GDDR and LPDDR are becoming less and less. DDR4 borrow some features of GDDR5 such as VDDQ termination, DBI and so on.

2.2.2 Comparison of Conventional DRAM

Table 2.2 shows the differences in DDR1, DDR2, DDR3, and DDR4. Supply voltage is scaled down for low power consumption. Starting from DDR2, OCD and ODT are utilized. OCD is off-chip driver impedance adjustment for the voltage output level for DQ and DQS. So it helps to maximize the valid data window amplitude. ODT is on-die termination to reduce the signal reflection. Starting from DDR3, dynamic ODT,

Table 2.2 DDR comparison

	DDR1	DDR2	DDR3	DDR4
VDD [V]	2.5	1.8	1.5	1.2
Data rate [bps/pin]	200 ~ 400 M	400 ~ 800 M	800 M ~ 2.1 G	1.6 ~ 3.2 G
STROBE	Single DQS	Differential DQS, DQSB		
Pre-fetch	2 bit	4 bit	8 bit	8 bit
Interface	SSTL_2	SSTL_2	SSTL_15	POD-12
New feature		ODT	Write levelling	CA parity
		OCD calibration	Dynamic ODT	Bank grouping
			ZQ calibration	Gear down
				DBI, CRC
				CAL
				PDA
				FGREF
				TCAR

DBI Data bus inversion, *CAL* Command address latency, *FGREF* Fine granularity, *CRC* Cyclic redundancy check, *PDA* Per DRAM addressability, *TCAR* Temperature controlled array refresh

ZQ calibration and write leveling are applied. Dynamic ODT mode is for changing the termination strength of the memory without issuing an MRS command. MRS stands for mode register set and is used as a command set to control the memory mode. The dynamic ODT mode supplies two RTT values which are RTT_Nom and RTT_WR. ZQ calibration is used to calibrate DRAM Ron and ODT values. DDR3 memory module adopted a fly-by topology for better signal integrity. Fly-by topology has the benefits of reducing the number of stubs and their lengths, but it creates flight time skew between the clock and DQS at each DRAM. Therefore, DDR3 supports write leveling to reduce this skew of DQ. DDR4 has dual error detection schemes. The first one is cyclic redundancy check for DQ pins. And the other is command address parity for command and address pins. The CRC scheme is used with data-bus inversion scheme. Data bus inversion reduces the number of switching at DQs to reduce the I/O current. This also improves signal integrity because it reduces the simultaneous switching output (SSO) noise.

2.2.3 Comparison of Graphics DRAM

Now let us examine the graphics memories from Table 2.3. GDDR5 has many new features. For example, it has a double data rate address scheme. At the rising edge of CK, command and half of the address are issued. At the rising edge of CKB (which is the falling edge of CK), remaining half of the address are issued. GDDR5 has differential data clock inputs, called WCK and WCKB. These are called write clocks. Write data are referenced to both edges of a free-running differential forwarded clock (WCK, WCKB) which replaces the pulsed strobes used in conventional graphic memories such as GDDR3 as it called WDQS. It also includes address bus inversion logic and ABI (Address bit inversion) pin. This means that the number of pull down switching pins is reduced to less than four or five out of nine to lower the power

Table 2.3 GDDR comparison

	GDDR1	GDDR2	GDDR3	GDDR4	GDDR5
VDD [V]	2.5	1.8	1.5	1.5	1.5/1.35
Data rate [bps/pin]	300 ~ 900 M	800 M ~ 1 G	700 M ~ 2.6 G	2.0 ~ 3.0 G	3.6 ~ 7.0 G
STROBE	Single DQS	Differential Bi-directional DQS, DQSB	Single unidirectional WDQS, RDQS		
Pre-fetch	2 bit	4 bit	4 bit	8 bit	8 bit
Interface	SSTL_2	SSTL_2	POD-18	POD-15	POD-15
New feature		ODT OCD calibration	ZQ	DBI Parity (opt)	Bank grouping No DLL PLL (option) RDQS (option) WCK, WCKB CRC ABI

DQS DQ strobe signal, *DQ* is data I/O pin, *ODT* on die termination, *OCD* Off chip driver, *ABI* address bus inversion

consumption. If the ABI pin is high, command and address pins are not inverted. If the ABI pin is low, command and address pins are inverted. Bank grouping is a solution for securing the core timing margin for high-speed operation. POD (Pseudo Open Drain) is employed in GDDR memory. VDDQ termination is adopted. Only the low data consumes the energy from the channel. The interface scheme is illustrated in Fig. 2.9. In SSTL, VREF is $0.5 \times VDDQ$. Therefore, the signal center point is a half of VDDQ. In order to transfer data via the channel, HIGH and LOW data consume power. Otherwise, the VDDQ termination type of GDDR5 only consumes power to drive LOW data to the channel. HIGH data stays in VDDQ. GDDR3, 4, 5 and DDR4 employ a POD (Pseudo Open Drain) type, which is good at high-speed operation with low power. If the DBI function is enabled, the energy consumption is more reduced. Because LOW data only consumes energy, if the number of LOW data is larger than HIGH data, then data polarity is inverted and signal DBI is activated.

2.2.4 Comparison of Mobile DRAM

In Table 2.4, we compare low power DRAMs. Data rate of LPDDR3 can reach up to 1.6 Gb/s/pin. The supply voltage of LPDDR2 and 3 are reduced to 1.2 V from 1.8 V. Here, DQS_T and DQS_C represent a pair of data strobes. DQS_C is the complement of DQS_T. Data strobe of LPDDR3 is bi-directional and differential. DQS_T is edge-aligned to read data and centered with write data. The differential DQS and ODT is happened in mobile DRAM even though they require additional power consumption to increase the operating speed. However, the ODT is not welcome to system engineers due to the high power consumption even though the speed performance is increased with the help of the ODT. The DLL is not used in LPDDR

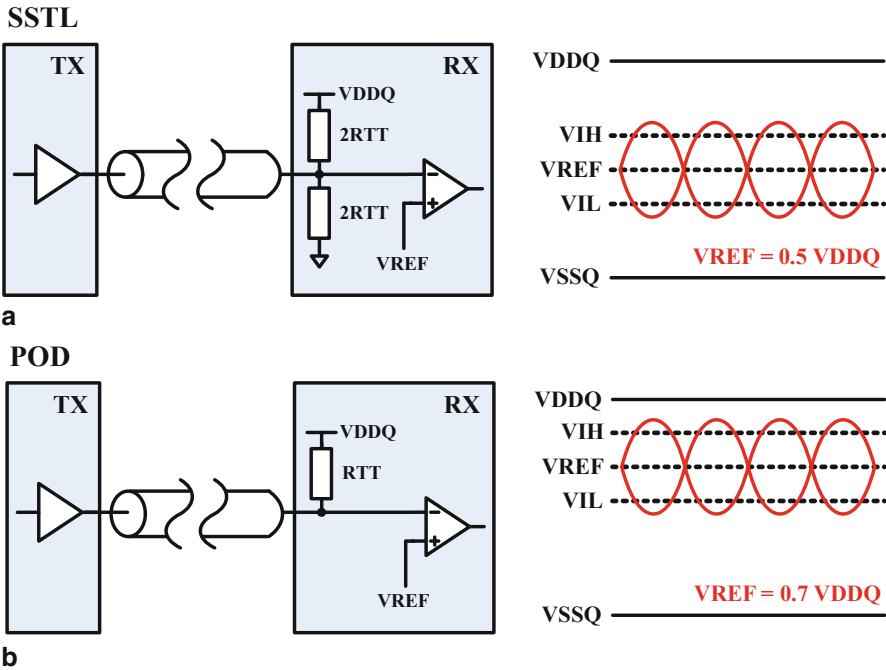


Fig. 2.9 Interface comparison between a SSTL for DDR2/3 and b POD for GDDRx

Table 2.4 LPDDR comparison

	LPDDR1	LPDDR2	LPDDR3
VDD [V]	1.8	1.2	1.2
Data rate[bps/pin]	200~400M	200 M~1.066 G	333 M~1.6 G
STROBE	DQS	DQS_T, DQS_C	DQS_T, DQS_C
Pre-Fetch	2 bit	4 bit	8 bit
Interface	SSTL_18	HSUL_12	HSUL_12
New feature	No DLL	No DLL CA pin	No DLL ODT (high tapped termination)

SSTL Stub series terminated logic, HSUL High speed un-terminated logic

memory in order to reduce the power consumption. The typical features of low-power DRAM are as follows:

- Low voltage (additional PAD for VPP)
- Low I/O capacitance
- Un-terminated I/Os (HSUL)
- Typically X16 or X32 data width per die
- Usually contained in multi-die packages
- Fast low-power entry and exit
- Very low standby (self-fresh) power (with long refresh rate)

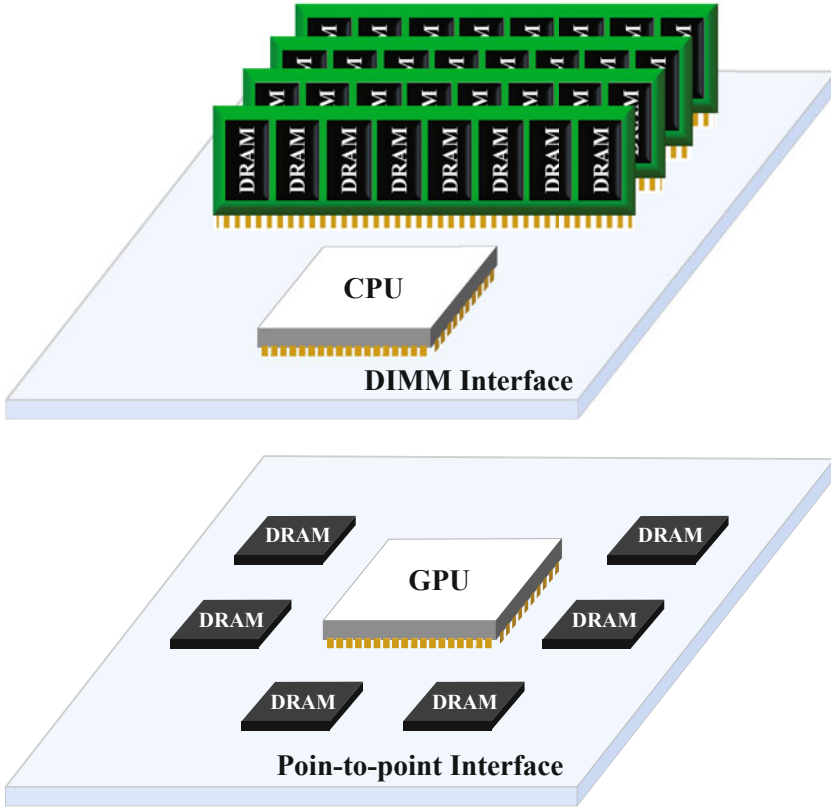


Fig. 2.10 Memory interface of PC and graphics memory

Temperature compensated self-refresh mode/ Partial array self-refresh
 Deep power down mode
 No DLL/ Low speed (up to LPDDR2, but high speed requirements increase)

2.3 Application

As shown in Fig. 2.10 DRAM has many single-ended data channels. A DDR memory module consists of multi rank and multi DIMM. This causes impedance discontinuities due to many stubs, connectors, vias and so on. Therefore, the data channel of DRAM is vulnerable to noise coupling and inter symbol interference, ISI. DQ drivers or receivers usually operate all at the same time. So simultaneous switching output noise (SSON) is a problem for high quality SI (Signal integrity). Otherwise, graphics DRAMs are configured with point-to-point connection. Therefore SI is better than the one of DIMM channel. Therefore, it is harder to increase the operating speed for DIMM channel than a graphics point-to-point channel. The last issue of

High-Bandwidth Memory Interface

Kim, C.; Lee, H.-W.; Song, J.

2014, VIII, 88 p. 91 illus., 41 illus. in color., Softcover

ISBN: 978-3-319-02380-9