

Preface

These days most people use at least one personal computing device, like a pc, a tablet or a smartphone. DRAM is one of the data storage components in these devices, and memory bandwidth has increased significantly over the last 10 years. Main memories like DDR2, DDR3 and DDR4 are used in PCs and servers. DDR4 is a higher-bandwidth successor to DDR2 and DDR3 to support high-speed applications. Graphic DDR (GDDR) is used in graphic cards and game consoles. GDDR series provide higher-bandwidth than main memories to process large image and video data such as frame data buffering and life-like 3D image rendering.

Many high-speed wireline interface techniques for other applications have been adopted in SDRAM to increase the bandwidth. However, there are several key differences between memory interface and other wireline applications, which cause difficulties for synchronous DRAM (SDRAM) design. First, SDRAM cannot utilize differential signaling due to inherently large number of data pins. Second, a DDR memory module consists of multi rank and multi DIMM which causes impedance discontinuities due to many stubs, connectors, vias and so on. Therefore, the data channel of DRAM is more vulnerable to noise coupling and inter symbol interference. Third, simultaneous switching output noise is a problem because DQ drivers or receivers usually operate all at the same time. The last major difference of high-bandwidth DRAM design is that the transistor performance of DRAM process is very poor compared to that of logic process.

There are many technologies to enhance the memory interface such as TSV interface, high-speed serial interface including equalization, ODT, pre-emphasis, wide I/O interface including crosstalk, skew cancellation, and clock generation and distribution. This book provides overviews of recent advances in memory interface design both in architecture and at circuit levels. Subtopics will include signal integrity and testing. Future trends for further bandwidth enhancement will be covered as well. This book is developed mainly from the research outputs on memory interface by the Advanced Integrated System Lab of Korea University and a number of notable research papers from other groups. This book provides readers with crucial resources to develop their studies about high bandwidth memory systems.

Chapter 1 investigates the basic DRAM characteristics including cell array access control, read and write operation, and an example of DDR3 configuration. Power

dissipation is a big concern in this mobile era. The important considerations for active and stand-by power consumptions are described. Chapter 2 deals with I/O configuration for DDR SDRAM. It provides the readers with an understanding for speed limitation of cell access. Several important DRAM organizations are compared to differentiate and to help understand the various types of DRAM. Chapter 3 focuses on the design of clock generation and distribution. Because DLL (Delay Locked Loop) is widely used in DDR SDRAM, in-depth investigation and analysis of DLL is provided. To improve the data valid window for high-speed DRAM, DCC (Duty Cycle Corrector) should be employed. This chapter also includes the issues and requirements of DCC. Twenty papers about DLL are categorized according to their research area. In Chap. 4, general transceiver design techniques for the DRAM interface are introduced. The design issues in the transceiver arise from the imperfections in the channel characteristics. Therefore, the effects of channel are discussed, and the solutions from previous works are introduced. Also, several design techniques which are not widely adopted in other interfaces are introduced. The general concepts of the transceiver and advanced design techniques help to understand the high-bandwidth DRAM interface. Chapter 5 investigates the TSV (Thru Silicon Via) interface. TSV is a good solution to increase the bandwidth of DRAM with low power consumption. It is helpful to understand the basic configurations, architecture and issues of TSV based DRAM. One method for removing data confliction is investigated.

In the near future, further bandwidth increase is highly demanding. Therefore many readers are interested in design techniques for high-speed memory interface. This book will guide those engineers.

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