

## Chapter 2

# System Level Test Methods

In [Chap. 1](#) the major trend toward SoC and SoP integration with system level pins was emphasized. This trend results in the design paradigm shift toward integration of the system level ESD protection capability on-chip. By providing the second stage ESD current capability the on-chip ESD protection can be both used for the IC-system co-design with the PCB components ([Chap. 5](#)) or provide a complete system level compliant pin protection.

To support this trend a significant gap between component and system level test methods and standards is bridged. The system level standards, for example IEC 61000-4-2, have been developed to support ESD and EMI compliance qualification of the systems rather than to validate the passing level of IC components. The accomplished system design in general significantly impacts the ESD test results and pulse waveforms. However not only the system blocks, but also the PCB design are usually not finalized or communicated to the IC developers and included in the initial specification of the component product.

Needless to point out that the ESD clamp solution development prior to the IC design itself creates a challenge on the predictive experimental validation. Thus both from technical realization perspective and from overall methodological point of view, the on-chip system level ESD design requires at least a good understanding of the test standards, procedures and their adaptation for the component level and on-wafer verification. The aspects of such understanding include the measurements of the quasi-static I-V characteristics, transient ESD pulse current and voltage waveforms, and the establishing of the correlation factors between particular device types, ESD protection capability and different pulse types.

This Chapter describes the physical aspects of the key test methodologies and their applications for the on-chip ESD system level design at each development stage. The focus is made on the explanation of the ESD gun test on board level, followed by the package and wafer level test methods towards an approach for a more effective on-chip design rather than just make a citation of the standard documents or to provide a reference guide.

The first section focuses on system level tests like the commonly used IEC 61000-4-2 and ISO 10605 standards. This material is followed by the key methodological approach of Human Metal Model (HMM) testing as the first

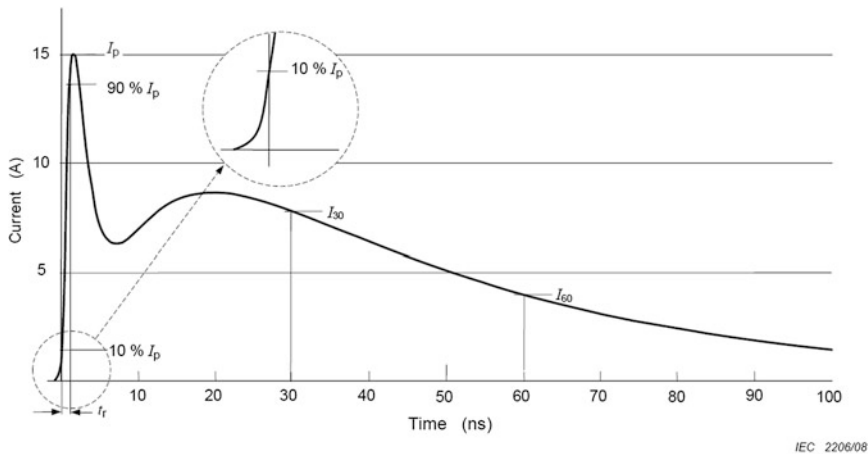
component-level emulation of system level ESD stress. The following section presents the transmission line pulse methodology as a very common tool for the on-chip design. The next section introduces the ESD waveform capturing as an essential approach for analysis and verification of the transient device and circuit characteristic. A discussion of the correlation factors for different pulses, devices and test conditions concludes this chapter.

## **2.1 Board Level Test Methodology**

The purpose of ESD testing in the laboratory environment is both to emulate the real life ESD event and to verify the protection capability of a component or a system in order to comply with the corresponding IEC and ISO standards. In case of on-chip system level design the differentiation can be made between the printed circuit board (PCB) level test and the stand-alone component-level IC tests. The further expansion of the methodology is the on-wafer validation of either an IC or even standalone ESD structures from a test chip. As discussed in [Chap. 1](#), the application of the component level standard pulses (HBM, MM and CDM) even with elevated pulse amplitude is not an adequate experimental and qualification approach to verify the system level ESD robustness. This is mainly due to the different ESD pulse waveforms, absence of power-on conditions and in general different ESD current paths through the IC. The component-level HBM, MM and CDM tests are performed to ensure the robustness of an integrated circuit or discrete component during IC and system manufacturing in the ESD protected environment. This is done under expectation that future designed systems or system blocks reliability will not be impacted during assembly and manufacturing rather than to add an ability to pass the system level ESD tests. Therefore system-level ESD qualification to obtain the certification is carried out at least for an equivalent of a system to ensure the functionality during operation, handling and maintenance.

### ***2.1.1 General Electrical Equipment IEC 61000-4-2 Standard and Test Methodology***

IEC 61000-4-2 [21] is the most commonly used standard released by the International Electrotechnical Commission (IEC). It defines electromagnetic compatibility (EMC) for test and measurement techniques for the electrostatic discharge immunity test. The document defines the corresponding system level ESD pulse waveform parameters, that should be delivered by ESD tester, and outlines the corresponding test methodologies. Since the standard is originally defined for system tests, it brings no straight forward understanding on how to apply it for the



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**Fig. 2.1** IEC 61000-4-2 Ideal contact discharge current waveform at 4 kV with defined parameters:  $I_p$  3.75 A/kV  $\pm$  15 %,  $I_{30ns}$  2 A/kV  $\pm$  30 %,  $I_{60ns}$  1 A/kV  $\pm$  30 %,  $t_r$  rise time of 0.7 ns  $\pm$  25 %

verification of the protection capability of IC pins with system level ESD requirements. It is even more undefined how to apply the test for standalone on-chip ESD protection clamps.

The major difference between the component and system ESD pulse waveforms and the energy of the pulses was already compared in Chap. 1. The waveform of the ESD current supported by this standard (Fig. 2.1) physically represents an event of a discharge of a conductive object through a system port. The double-peak waveform (Fig. 2.1) represents the physical discharge produced by a conductive distributed object suddenly connected or approached to the discharge point. The first short peak corresponds to the discharge of the conductive peripheral region of the object in the immediate vicinity connected to the port. The second peak represents the discharge of the remaining body of the object. Assuming a constant object resistance, the periphery is quickly discharged with a short rise time and low resistance forming the first high amplitude peak. The remaining discharge of the object body has a bigger pulse propagation delay and higher current path impedance thus forming a longer, but smaller amplitude second peak.

The ratio between peak amplitudes and duration is defined by the standard itself. In the IEC 61000-4-2 short circuit contact discharge current waveform the amplitude of the first peak  $I_p$  is defined at  $\sim 3.75$  A/kV  $\pm$  15 % with rise time of 0.7 ns  $\pm$  25 %, while the current levels after 30 ns and 60 ns from the beginning of the pulse  $I_{30ns} \sim 2$  A/kV  $\pm$  30 % and  $I_{60ns} \sim 1$  A/kV  $\pm$  30 %, respectively. Thus in general according to the standard the pulse waveform has significant margins to be varied in different test setups.

The real life system level stress in uncontrolled environments has much higher energy than an ESD event in an ESD protected areas (EPA). However, the overall difference between the system and the component level standards are not only based in the much larger stress current level and the corresponding higher energy (Fig. 1.5). Another major differentiating factor for the system standard in comparison with the component level standards is that the tests are accomplished both under power-on and power-off conditions. This is done to reflect the real life applications where the system can experience an ESD event both under power-on and power-off conditions. Thus when a component is subjected to ESD stress the stress may result in a failure which causes irreversible changes in the device and interconnects.

Four possible system states are classified by IEC 61000-4-2 standard as a result of system-level ESD stress:

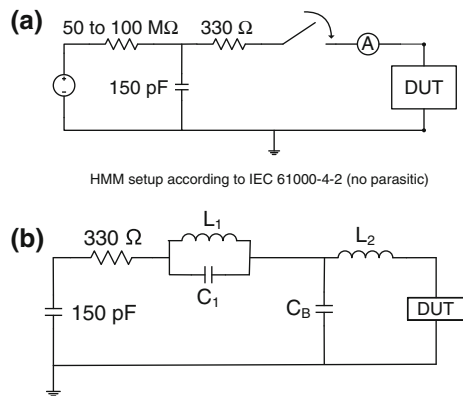
- A normal performance within given limits;
- B temporary loss of function or degradation of performance which ceases after the disturbance ceases, and from which the equipment under test recovers its normal performance, without operator intervention;
- C temporary loss of function or degradation of performance, the correction of which requires operator intervention;
- D loss of function or degradation of performance, no recovery possible.

The goal for most of the system designs is to pass the qualification test with the system state class A. Classes B and C represent so-called soft failures that are either self-restored or require a system reset. The classes B and C bring another major differentiation to component-level testing which correlates only the failure classes A and D.

Since the waveform is defined by the Standard, a number of testers have been manufactured by ESD equipment vendors to enable the test in laboratory or even in a field environment. In the standard the simplified discharge circuit uses a 150 pF capacitor and a resistance of 330  $\Omega$  to create the system-level ESD stress pulse (Fig. 2.2). Although the standard proposes the equivalent circuit (Fig. 2.2a) for the test setup, it is obvious that this simplified circuit cannot support double-peak standard waveform. The exact tester schematic is usually more complex to fit to the pulse waveforms. However the circuit (Fig. 2.2b) provides a relatively good waveform to meet the standard with the component parameters for example:  $L_I = 4.5 \mu\text{H}$ ;  $C_I = \text{pF}$ ;  $C_B = 20 \text{ pF}$  and  $L_I = 200 \text{ nH}$ .

The results of stand-alone IC test or packaged ESD component verification unlikely can be extrapolated to predict an arbitrary system passing level. Perhaps, a more realistic goal can be set to understand the aspects of the “worst case scenario”, the impact of the test conditions and the test methodology. This is an important part of the IC-System co-design approach presented in Chap. 5. The critical step toward this goal is to build an understanding of the contact and air discharge methods in case of the bench test setup specific for the IEC 61000-4-2 standard with the test methodology.

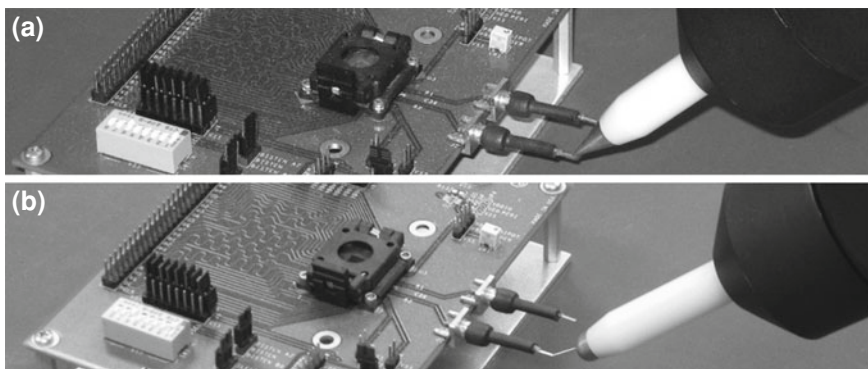
**Fig. 2.2** Simplified (a) and real tester (b) schematic of an IEC 61000-4-2 compatible discharge circuit, the L-C parasitic may vary in a real tester discharge circuit



The ESD pulse current waveform as defined in the standard (Fig. 2.1) is mostly reproduced only during tester calibration with a dedicated target tool. In the majority of other test conditions the waveform shape is dependent on the ESD protection components used in the object under test, system or PCB design.

A significant deviation of the ideal standard waveform is observed for the air-gap test. Originally, both contact and air gap discharges are defined as a requirement when testing for IEC 61000-4-2 specifications with the preference of the contact discharge. However, typically by manufacturers the requirement for IC pins to pass a given level during both the contact and air discharges are specified. Air discharge is usually defined at a higher level than contact discharge. A common requirement for the level 4 of IEC 61000-4-2 specification is the passing of 8 kV contact and 15 kV air gap discharge. Thus to avoid “surprises” with inadequate performance at the system-level an IC with system level pins must be verified by a methodology that would adequately predict this performance or at least cover the worst case scenario.

Contact discharge is applied to conductive surfaces (e.g. connectors) and air discharge to insulating surfaces (e.g. housing) of system blocks. In case of air discharge, the current level and rise time are less reproducible and more related to environmental conditions (humidity, speed of the tip approach, etc.). For the air discharge test the round ESD gun tip is used (Fig. 2.3a). When the test voltage is set the ESD gun is moved towards the discharge point until a spark appears and then further until the ESD gun tip touches the discharge point on the system surface. This action is usually repeated with positive and negative polarities depending on the applied test procedures, for example,  $\sim 10$  times. Touching the systems surface is important for the removal of the residual induced charges from the system since only some guns have an integrated charge remover. To remove the residual charge the system must be grounded, brushed, etc. The gun must touch the object because it is intended to model the event when the user, after the first air-gap discharge, will or can eventually touch the apparatus.



**Fig. 2.3** Examples of the contact (a) and air-gap (b) discharge gun testing on PCB

At the contact discharge test the sharp ESD gun tip (Fig 2.3b) is used to obtain a good electrical contact with the conductive system surface. Similarly to the air-gap test about 10 discharges are typically applied with positive and negative polarities.

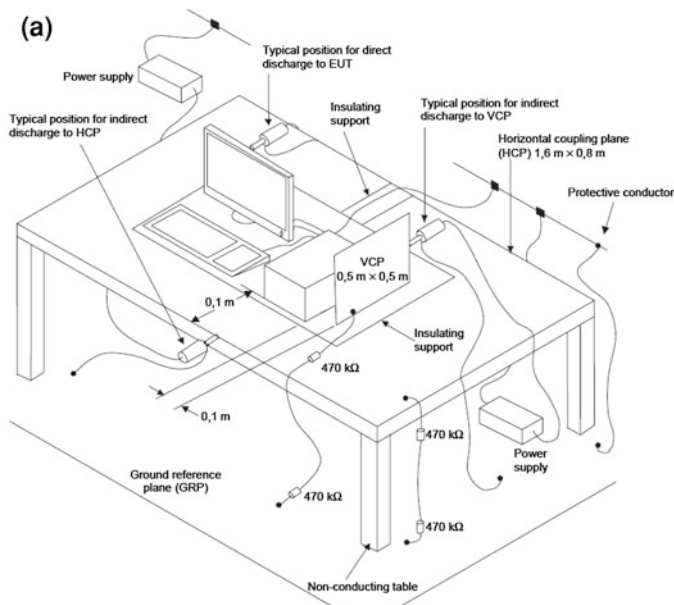
The test setup for the system level ESD verification is recommended in the standard (Fig 2.4a). These main components critically impact the current pulse waveforms. If inappropriately used, they may significantly change the outcome of the test. In the standard, two different types of tests are distinguished: tests performed in laboratories and post installation tests performed on equipment in its final installed conditions.

When the system is not grounded, for example in case of battery powered systems, there is no self-discharge like in grounded equipment. If the charge is not removed before the next ESD pulse is applied, it is possible that the EUT or part(s) of the EUT are stressed significantly lower than the intended test voltage level or higher if the polarity of the stress pulse is reversed. To avoid the charging of EUT to an unrealistically high charge the test setup is modified (Fig. 2.4b). The possible additional charges are removed prior to each applied ESD test pulse by increasing the time interval between successive discharges or by sweeping away the charges from the EUT through a grounded carbon fiber brush, or with bleeder resistors (for example,  $2 \times 470 \text{ k}\Omega$ ) in the grounding cable.

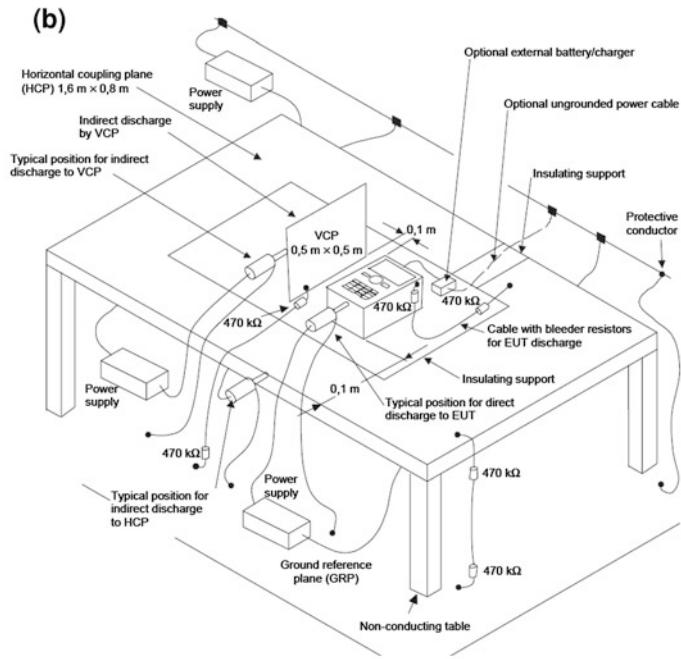
In general the components form a very large scale capacitor  $C_T \sim 56 \text{ pF}$  between the ground reference metal plate and the upper metal plate, mounted on the table with a specified height. Also there is a capacitance  $C_B$  between the upper metal plate and the board. The distance between the corresponding upper plate and board is determined by the dielectric mat defined by the standard.

The value of capacitance  $C_T$  is practically fixed by the design of the setup. The value of the board capacitor  $C_B$  is limited by the mat parameters, but otherwise variable depending on the board size and coupling with the upper metal plate.

The pulse waveforms are sensitive to the ground connection of the plates, tested boards and the gun. In the IEC 61000-4-2 standard the ground connection has very

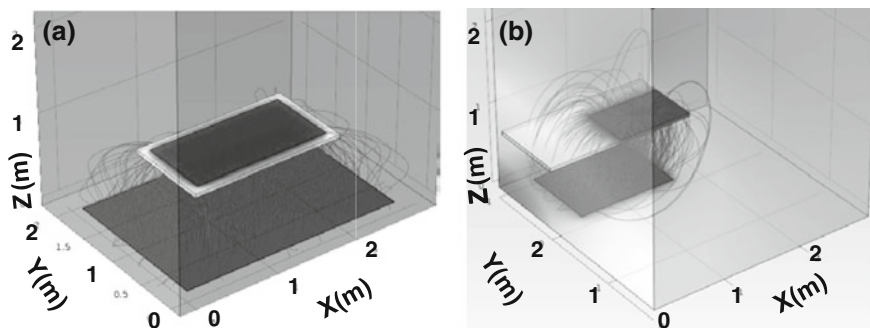


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**Fig. 2.4** Example of IEC 61000-4-2 standard test setup for floor-standing equipment laboratory tests (a) and for ungrounded table-top equipment (b)



**Fig. 2.5** 3D FEM electrostatic simulations for electric potential carried out for IEC standard setup with the upper plate positioned in the middle of the table (a) resulting in with calculated capacitance  $\sim 56$  pF (b) and an incorrect custom setup with upper plate shifted to the corner of the table calculated capacitance  $\sim 25$  pF (courtesy of Augusto Tazzoli)

high impedance through two 470 k $\Omega$  charge bleeding resistors and additional inductive wire impedance. These bleeding resistors are only capable to remove the residual charge from the system during the long time between the stress events. Therefore the major ESD current path is provided by low impedance of the capacitors formed by the test setup. This impedance is only a few Ohms for the first current peak. The major difference in the ground connection for the power-on test is translated from the power supply source implementation that can be battery or power grid based.

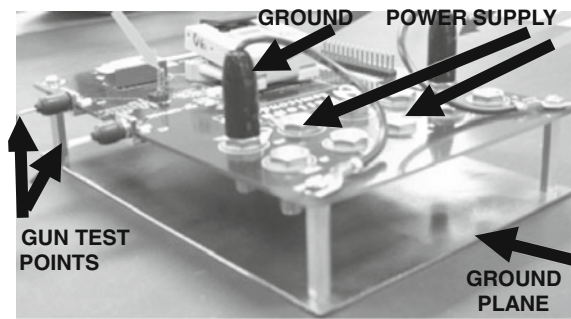
The stress waveform depends on the current path during the discharge. In case of no direct ground connection to the upper plate and to the board, the bleeding resistors cannot conduct any large system level current. Thus the discharge path is realized through the two serial capacitors  $C_T$  and  $C_B$ . In this case, the position of the metal plates and the dimension is directly impacting the discharge capacitance which changes the waveform of the ESD current pulse. A simple electro-magnetic simulation of the equivalent capacitance of the table and the ground reference plate demonstrates a significant variation of the test setup capacitance depending on the upper plate—Horizontal Coupling Plate (HCP) size and position (Fig. 2.5).

An important part of the system level test is the test board design. The devices for customer systems that require either IEC 61000-4-2 or ISO 10605 are expected to be tested in conditions that more or less accurately emulate the system in the final application. Thus at least the board level stress is an approach to meet a more ideal expectation for robust ESD design without redesigning the final system.

Initially the test boards can be either demo boards or actual customer boards (Fig. 2.6). To enable the gun test in case of present standard connectors, a port pin extenders is introduced. However it is ideal to understand the customer board environment and to clarify how the case/housing is grounded. The following question should be answered before the design:



**Fig. 2.6** Example of the industrial evaluation board design with the ground plane and extended connectors



- (i) *Does demo board need a ground plane?*
- (ii) *Is the case floating?*
- (iii) *Are cables being connected?*
- (iv) *Are there any other specific requirements?*

Through evaluation of the current waveforms the capacitor  $C_B$ , which is formed by the board ground plane with the upper metal plate, is now well understood in the industry. This understanding has been translated into the supported practice to mount all custom boards on an additional ground metal plane. In addition, metal pins extended from the board surface are spaced apart about  $\sim 10$  mm. Additional pins of  $\sim 5$  mm are introduced to guarantee the discharge of the current pulse through the tested pins rather than through non-dedicated PCB components.

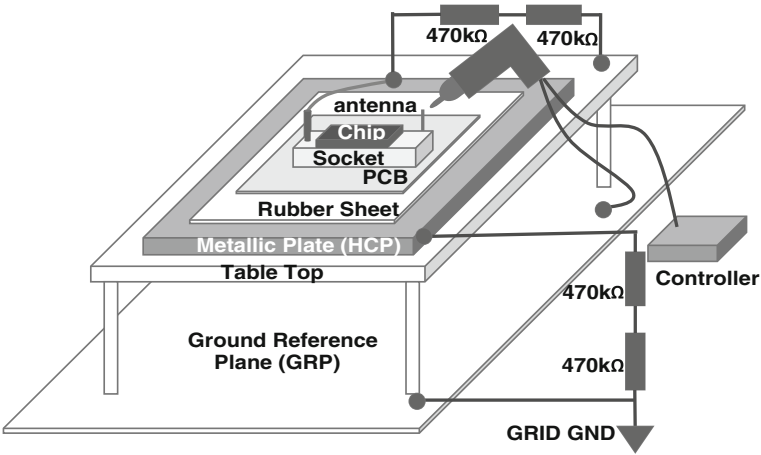
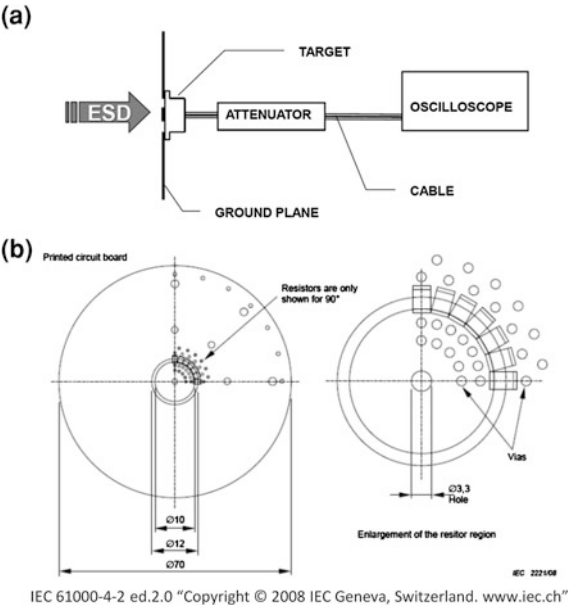
Gun verification techniques, practical aspects and recommendations are described by the gun manufacturers [22]. They cover the parameters which must be measured. Those parameters are the tip voltage, the contact discharge current waveform which is defined for its peak, rise time and the currents after 30 and 60 ns, and in case of air discharge the rise time and time constant.

For stress waveform verification a low impedance shunt ( $<2.1 \Omega$ ) is used. It represents a discharge into a large metallic object rather than just a piece of wire (Fig. 2.7). A new calibration target design with a frequency response flatness of up to 4 and a 2 GHz oscilloscope was introduced in IEC 61000-4-2:2008. Environmental factors also affect the calibration results. Therefore no air discharge verification procedure was included due to too high variability of the approaching speed, humidity, and the arc and ionization length.

A few simple experiments can be used to demonstrate the impact of the test setup grounding on the air gap test current waveforms. In the setup for the packaged component test on PCB with no external ground (Fig. 2.8) the current often can be a source of miscorrelation between the contact and the air discharge. It largely depends on both the PCB ground plate dimension (Fig. 2.9a) and the bleeder resistor value (Fig. 2.9b).

Certainly the presence of the high value bleeder resistor is negligible for the alternative current path. A significant change in the pulse waveform results in formation of the negative current peaks that may result in a damage of the device

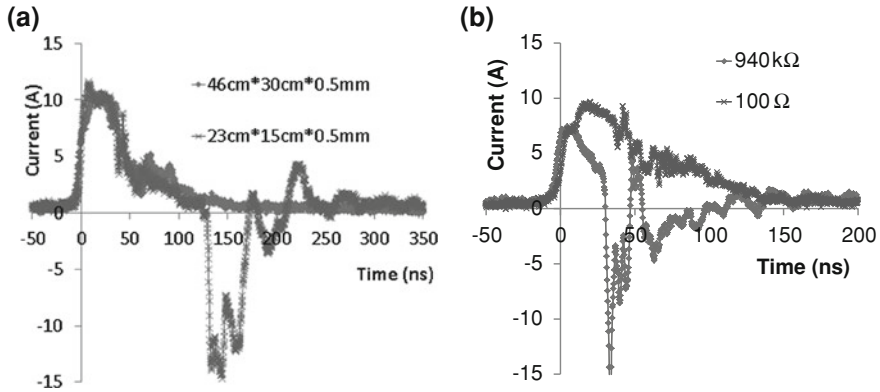
**Fig. 2.7** ESD simulator verification setup (a) and the verification target (b)



**Fig. 2.8** Setup for system level test with the bleeding resistors connected to the upper metal plate only

in rather unexpected conditions. For example a blocking junction of a dual-direction protection design can be destroyed during a positive air discharge rather than negative, as it would be originally expected.

An ideal air discharge waveform for different load conditions is not defined even by the standard. It is realized only when the gun ground is connected directly



**Fig. 2.9** Current waveforms for 8 kV air gap discharge realized in the set up (Fig. 2.8) for the conditions of different PCB plate size (a) and the resistors values (b) (courtesy of Yunfeng Xi)

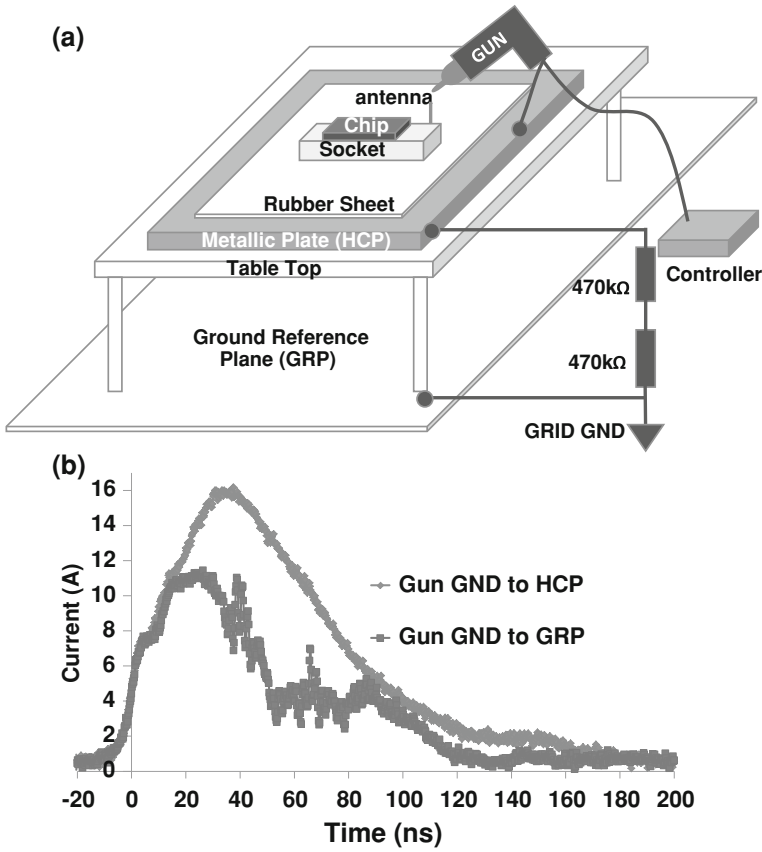
to horizontal coupling plane (HCP, Fig. 2.10). In this case the waveform with a good accuracy can be assumed similar to the standard pulse (Fig. 2.1) with simply eliminated first peak. In this conditions according to the experimental waveforms the only peak has the slow rise time until the maximum current of  $\sim 20\text{--}40$  ns with the same current levels after 30 and 60 ns from the beginning of the pulse  $I_{30ns} \sim 2 \text{ A/kV} \pm 30\%$  and  $I_{60ns} \sim 1 \text{ A/kV} \pm 30\%$ , respectively. To reproduce this waveform in simulation namely the circuit (Fig. 2.2a) can be used, rather than (Fig. 2.2b). The additional parasitic components and circuit parameters can be adjusted to form the single peak pulse.

### 2.1.2 Automotive Standard ISO 10605

Another widely used common standard for system-level ESD test was released by ISO (the International Organization for Standardization) as a major guidance in the automotive industry. This ISO 10605 standard [23] defines the road vehicles test methods for electrical disturbances from electrostatic discharge.

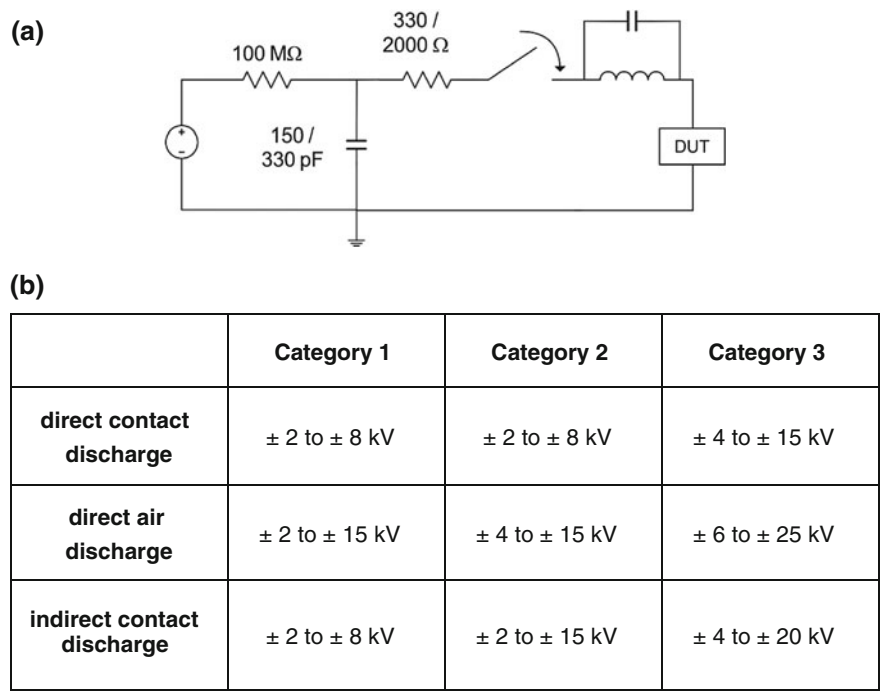
While IEC 61000-4-2 is created to establish a common and reproducible basis for evaluating the performance of electrical equipment subjected to ESD, the ISO 10605 Standard is created to specify ESD test methods necessary to evaluate electronic modules intended for vehicle use based on IEC 61000-4-2.

This Standard has many similarities with IEC 61000-4-2 especially if it is compared to the packaged level component tests (HBM, MM, CDM). However there are a number of differentiating aspects. First of all the ESD stress level that is usually required to be passed in the automotive industry is much higher. A passing level of 30 kV is often requested.



**Fig. 2.10** The non-standard setup with the IEC gun ground connected directly to the HCP (a) and the 8 kV air gap discharge current waveforms if the gun ground is connected to HCP and GRP (b) (courtesy of Yunfeng Xi)

The equivalent circuits for this test setup (Fig. 2.11a) include four discharge networks composed of a 150 or 330 pF charging capacitor and a 330 or a 2000  $\Omega$  discharge resistor. These are the only two combinations required by the standard in spite of that some gun manufacturers offer the option of 330 pF charging capacitor with 330  $\Omega$  resistor. Physically 150 pF–330  $\Omega$  combination represents the discharge of a human body through a metallic part to the system port, while 330 pF–2 k $\Omega$  combination represents a discharge of a human body directly through the skin.

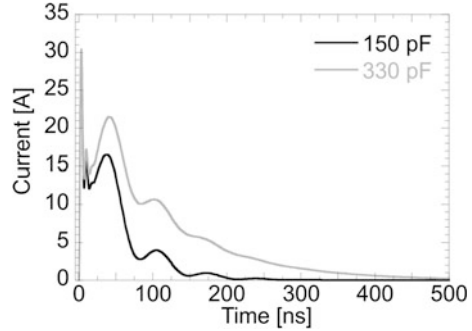


**Fig. 2.11** Principle schematic of an ISO 10605 discharge circuit, (a) the L-C parasitic may vary in a real discharge circuit, and (b) defined stress level [23]

Unlike in the IEC 61000-4-2, in the ISO 10605 the upper table plane (HCP) is directly connected to the gun ground. Another differentiation aspect of this standard from IEC 61000-4-2 is the preferred test levels. Although in addition to the 4 main levels IEC 61000-4-2 defines any arbitrary level x, many IEC test guns and ESD stress generators had 16 kV pre-charge limit. ISO 10605 clearly states test severity levels (Fig. 2.11b). The test severity levels are differentiated for the direct and indirect discharge.

Among more detailed vs. IEC 61000-4-2 definitions in ISO 10605 the speed of the gun tip approach speed should be between 0.1–0.5 m/s for any test. Because the approach speed is not trivial to measure, in practice the ESD generator should approach the DUT as quickly as possible until the discharge occurs or the discharge tip touches the discharge point without causing damage to the DUT or generator.

**Fig. 2.12** ISO 10605 current waveforms into short load, discharge network: 150/330 pF and 150  $\Omega$ , stress level: 8 kV



Similarly the charge removal measures are defined as the charge build-up can be eliminated by briefly connecting a bleeder wire with high resistance (1 M $\Omega$ ) in the following sequence: (i) between the discharge location and ground, and (ii) between the ground point of the DUT and ground. If there is evidence that the wire does not have any impact on the test result, it can remain connected to the DUT.

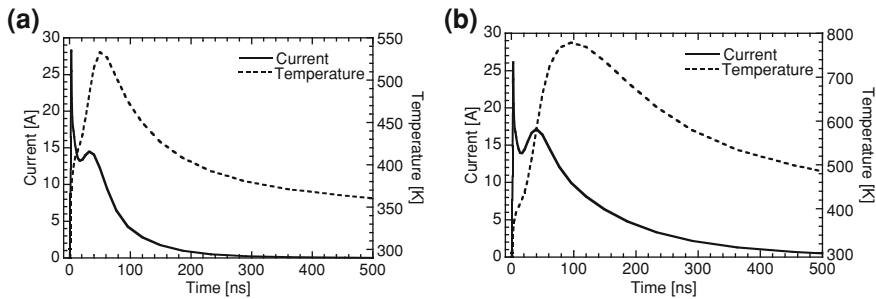
The evaluation test results are similar to IEC 61000-4-2, but according to Section C of the standard reports in detail on “function performance status classification (FPSC)”.

Two waveforms into a short circuit load (Fig. 2.12) have much longer discharge duration in comparison with the IEC 61000-4-2 stress when using the larger pre-charged capacitor. The ISO 10605 standard is not directly intended to be used in component-level testing, but it is a requirement of many automotive manufacturers to their suppliers.

The longer stress durations of some of the ISO 10605 discharge currents directly impacts the design of on-chip ESD protection structures. Figure 2.13 shows the current and the maximum temperature in an ESD diode during IEC 61000-4-2 and ISO 10605 discharge. The latter is created with a 330 pF/330  $\Omega$  network. Because of the longer stress duration the device self-heating is significant higher for ISO 10605 discharge stress conditions and needs to be taken into account during the ESD protection design to prevent unexpected failure during ESD qualification. One approach for the on-chip ESD protection design has been used by [24] where long duration TLP testing emulates the longer duration of an ISO 10605 stress.

To summarize the above two sections the comparison of the major specifications of the IEC 61000-4-2 and ISO 10605 standards is compiled in Table 2.1. The specific characteristic of IEC 61000-4-2 is that the ungrounded DUT cannot discharge itself like grounded equipment. Therefore the charge shall be removed prior to each applied ESD test pulse either by waiting a sufficient time between zaps through  $2 \times 470$  k $\Omega$  bleeding resistors or by a carbon fiber brush. During Air-discharge test methods, the gun should approach the DUT as fast as possible and touch it after the discharge occurred.

In ISO 10605 the speed of approach should be between 0.1–0.5 m/s for any test. Charge build-up can be eliminated by briefly connecting a bleeder wire with high



**Fig. 2.13** Current and temperature in an ESD clamp during system-level ESD stress: **a** IEC 61000-4-2 and **b** ISO 10605 with 330 pF/330  $\Omega$  discharge network, stress level: 8 kV

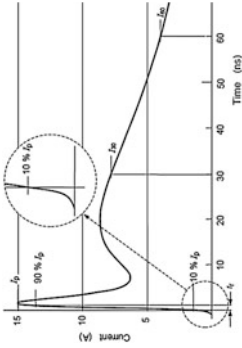
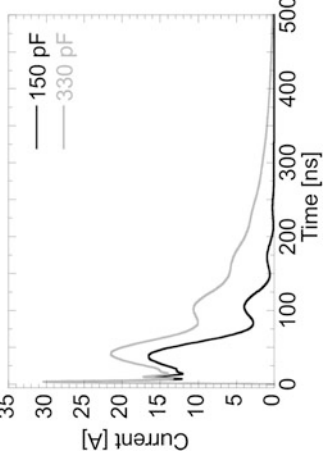
resistance (1 M $\Omega$ ) in the following sequence: (1) between the discharge location and ground, and (2) between the ground point of the DUT and ground. If there is evidence that the wire does not have any impact on the test result, it can remain connected to the DUT.

### 2.1.3 The Surge Standard IEC 61000-4-5

Similar to the ESD pulses the trend to propagate system level requirements for on-chip solutions has involved the specification of the surge requirements. The surge pulse specification is captured in the standard Electromagnetic compatibility (EMC) standard IEC 61000-4-5 *Part 4-5* [25]. The standard formalizes the testing and measurement techniques for the surge immunity test.

In real life the surge events are represented by systems switching transients or lightning strike events. The power system switching transients are associated with major power system switching disturbances, such as capacitor bank switching; minor local switching activity or load changes in the power distribution system; resonating circuits associated with switching devices, such as thyristors; various system faults, such as short circuits and arcing faults to the grounding system of the installation [25]. The major mechanisms of lightning surge include direct lightning strikes to an external (outdoor) circuit injecting high currents producing voltages by either flowing through the ground resistance or the impedance of the external circuitry; an indirect remote lightning strike which produces electromagnetic impulses that induce voltages/currents on the conductors outside and/or inside a building; lightning ground current flow resulting from nearby direct-to-earth discharges coupling into the common ground paths of the grounding system of an installation. The rapid change of voltage and flow of current which can also occur as a result of the operation of a lightning protection device can induce electromagnetic disturbances into adjacent equipment [25].

**Table 2.1** Comparison of the essential features of IEC 61000-4-2 and ISO 10605 standards

Standard	IEC 61000-4-2	ISO 10605
Target	General electrical equipment	Electronic modules for vehicle
Preferred test RC network	Contact discharge method 150 pF 330 Ω	Air discharge method Direct ESD, powered DUT 150/330 pF 330 Ω 150/330 pF 2 kΩ
Connection of ESD gun ground	To ground reference plane (GRP) through 2 × 470 kΩ charge bleeding resistors	Direct powered DUT: HCP and DUT GND Indirect powered DUT HCP or GRP
Preferred stress levels (kV)	Contact: 2, 4, 6, 8 Air: 2, 4, 8, 15	Contact: 2-8; 4-15 Air: 2-15; 4-15; 6-25 Indirect: 2-8; 2-15; 4-20
Number of discharges	At least 10 single discharges in the most sensitive polarity	Direct, <i>unpowered</i> or <i>Vehicle test method</i> at least 3 discharges are applied to all direct discharge test points for each specified test voltage and polarity Indirect 50 discharges are applied to all indirect discharge test points for each specified test voltage and polarity
Short circuit contact discharge waveform		



Similar to other standards the simulation of the transients in the laboratory environment is defined in the standard for the test generator to simulate the above-mentioned phenomena as close as possible to real physical conditions. This requires a corresponding surge generator in comparison with ESD pulse generators.

Respectively to the direct and indirect physical events, mentioned above, the surge testers simulate surge events to target both the direct and the indirect coupling conditions. During direct coupling the source of interference is in the same circuit, for example in the power supply network. Inductive spikes or load dumps can be another source. In those cases the generator simulates a low impedance source at the ports of the equipment under test. In case of an indirect coupling the source of interference is not in the same circuit as the victim equipment. In such case the generator simulates a higher impedance source.

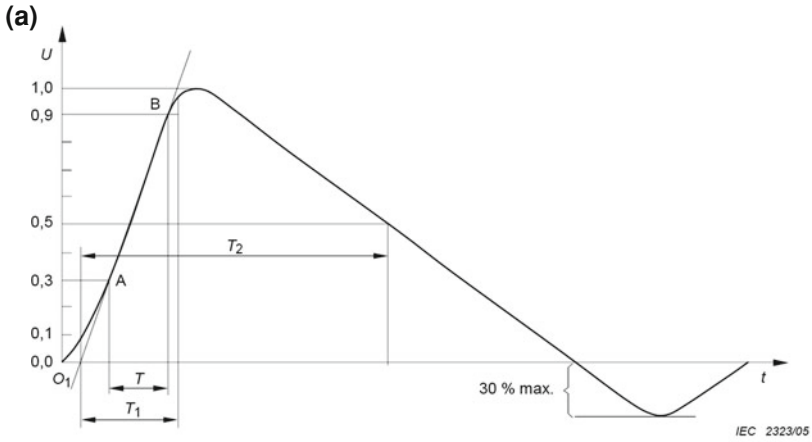
Unlike system and component level ESD pulses, the surge tests standard waveforms are specified both as open-circuit voltage and short-circuit current. Similarly to the system level ESD guns the waveforms for surge tester are verified without the equipment under test (EUT) connected. The output can be also specified for the cases of AC or DC powered products.

The surge generator is intended to generate a surge having an open-circuit voltage front time of  $1.2\text{ }\mu\text{s}$ ; an open-circuit voltage time to half value of  $50\text{ }\mu\text{s}$  (Fig. 2.14a); short-circuit current front time of  $8\text{ }\mu\text{s}$ ; and a short-circuit current time to half value of  $20\text{ }\mu\text{s}$  (Fig. 2.14b).

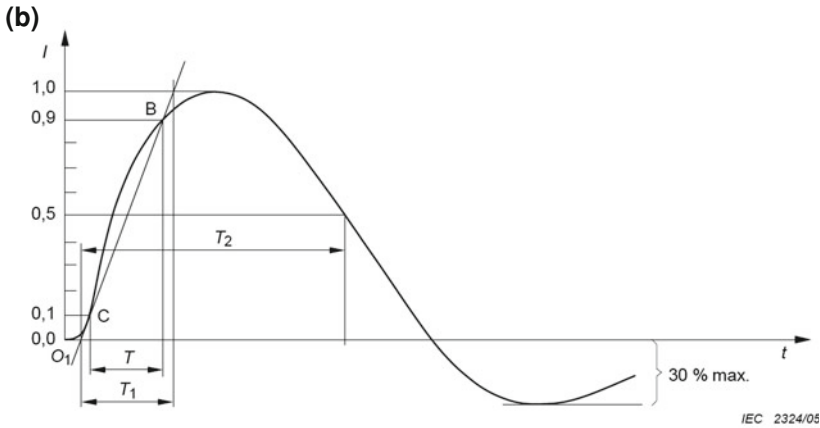
A simplified circuit diagram of a generator as provided by the standard is presented in (Fig. 2.15) with the high voltage source  $U$ , the charging resistor  $R_C$ , the energy storage capacitor  $C_C$ , the pulse duration shaping resistors  $R_{S\#}$ , the impedance matching resistor  $R_m$ , and the rise time shaping inductor  $L_r$ . The values for the generator components are selected so that the generator delivers the corresponding standard pulses for the  $1.2/50\text{ }\mu\text{s}$  voltage surge at the open-circuit and a  $8/20\text{ }\mu\text{s}$  current surge into the short circuit conditions. Most surge pulse generators produce pulses with peak currents in the range from  $250\text{ A}$  to  $2\text{ kA}$ .

For convenience, the ratio of peak open-circuit output voltage to peak short-circuit current of a combination wave generator may be considered as the effective output impedance. For this generator, the ratio defines an effective output impedance of  $2\text{ }\Omega$ . The resulting waveform of the voltage and current is a function of the EUT input impedance. This impedance may change during surges to equipment due to either proper operation of the installed protection devices, or due to flash over or component breakdown if the protection devices are absent or inoperative. Therefore, the  $1.2/50\text{ }\mu\text{s}$  voltage and the  $8/20\text{ }\mu\text{s}$  current waves have to be available from the same generator output as required by the load.

The circuit simulation for the surge tester in a Spectre simulator environment has been done in [25] for a circuit (Fig. 2.16a) with the components value  $C_C = 6.038\text{ }\mu\text{F}$ ,  $L_T = 10.37\text{ }\mu\text{H}$ ,  $R_{s1} = 25.105\text{ }\Omega$ ,  $R_{s2} = 19.8\text{ }\Omega$ ,  $R_m = 0.941\text{ }\Omega$  and  $U = 1082\text{ V}$ , demonstrating adequate short and open circuit waveforms (Fig. 2.16a).



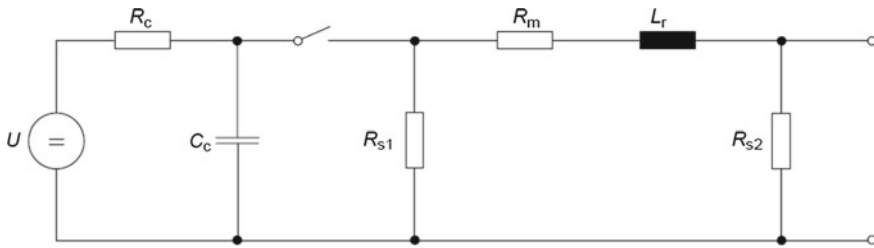
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**Fig. 2.14** Waveform of open-circuit voltage ( $1.2/50 \mu\text{s}$ ) at the output of the combination wave generator with no Coupling-Decoupling Network (CDN) connected (waveform definition according to IEC 60060-1) (a), waveform of short-circuit current ( $8/20 \mu\text{s}$ ) at the output of the generator with no CDN connected (waveform definition according to IEC 60060-1) (b)

The waveforms into a short circuit load (Fig. 2.16) have much longer discharge duration in comparison to the IEC 61000-4-2 stress. ESD pulses surge tests create the stress in a different time domain where not only adiabatic electrical phenomena



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**Fig. 2.15** Simplified circuit diagram of the combination wave surge generator

are responsible for the passing level but also the electro thermal phenomena are dominating. In general, ESD protection devices originally designed to withstand the electrical, rather than thermo-electrical current can only provide the ESD protection. In experimental results the typical correlation for SCR type of ESD protection devices results in a 10 times lower passing current.

According to [25] the selection of the source impedance of the combination wave generator depends on the type of cable, conductor or line. The differentiation is done for a.c or d.c. power supply networks, interconnections, the length of the cable lines, indoor/outdoor conditions, and the application of the test voltage for either line-to-line or lines-to-ground.

As for the Coupling Decoupling Network (CDN), the impedance of  $2\ \Omega$  represents the source impedance of the low voltage power supply network. Therefore in the equivalent cases the generator with its initial internal effective output impedance of  $2\ \Omega$  is used directly. The impedance of  $12\ \Omega$  with additional  $10\ \Omega$  serial resistor represents the entire low voltage power supply and ground network. The effective impedance of  $42\ \Omega$  is provided by an additional  $40\ \Omega$  resistor that represents the source impedance between all other lines and ground (Fig. 2.17).

Although the current of a surge can be lower, the total energy is much higher. Highly specialized ESD protection schemes can be ineffective against such slow transient, low voltage, but high current stresses. Stressing devices using relatively low level (up to 10–20 A) surge stresses can be also based on the IEC 61000-4-5 specification. Specialized surge protection may need to be added. A number of Transient Voltage Suppressors (TVS) have been characterized using the IEC surge stress for years. Their performance during an IEC surge stress is frequently found in TVS datasheets.

For the on-chip standalone devices surge-IEC correlation study TESEQ surge tester (NSG3040) was used with  $1\ \text{k}\Omega$  resistor in series with tested device to limit the current down to reasonable level of indirect surge scenario. The majority of SCR devices passed at least 3 kV stress with corresponding current  $\sim 3\ \text{A}$  demonstrating  $\sim 10$  times pulsed current reduction in comparison with the ESD current level. Failures from surge were open, while the typical failure signature from ESD

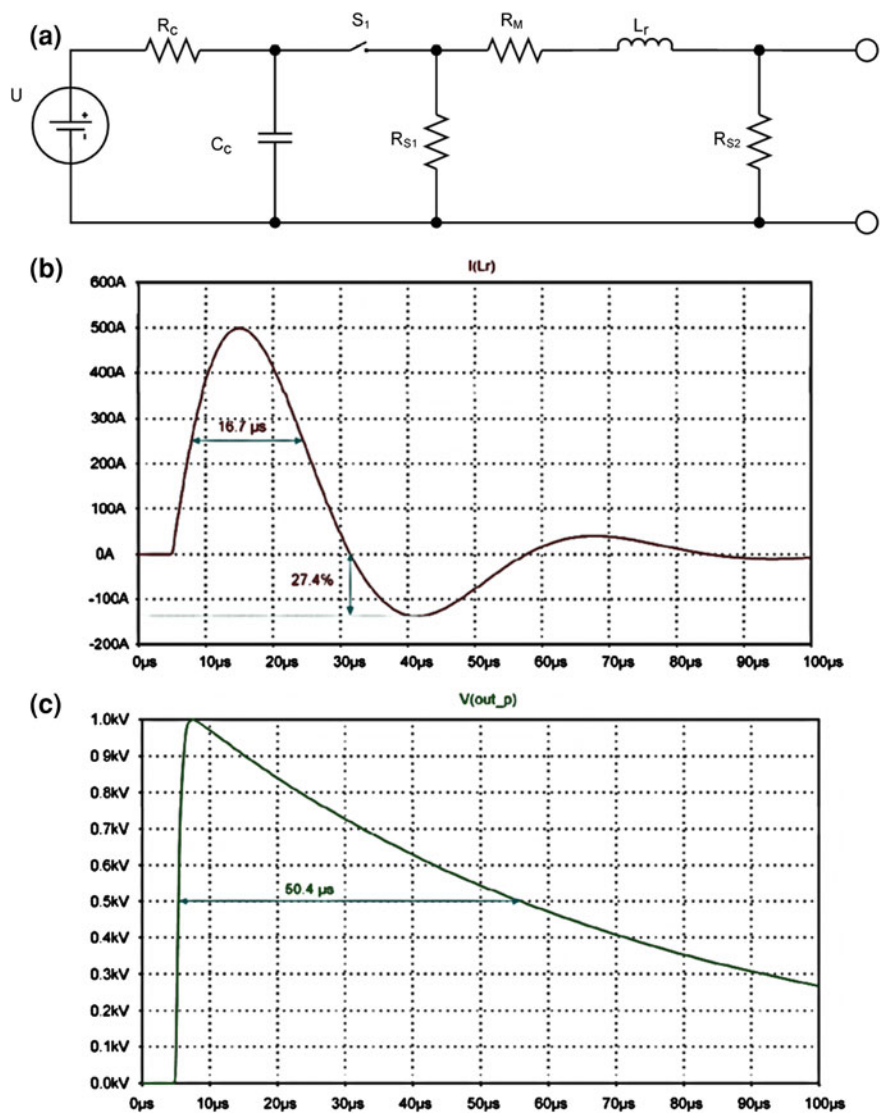


Fig. 2.16 Spectre simulation circuit for the combination wave generator (a) and the simulated waveforms for short circuit current (b) and open circuit voltage (c) [26]

stress is short circuit or elevated leakage (Table 2.2). In snapback mode the correlation factor between the surge current and standard component level test currents was  $\sim 0.1$ . In forward mode the backend limitations were dominant during the surge test.

A similar  $\sim 10$  times correlation factor between ESD and surge pulse peak current was measured for the snapback NMOS (SNMOS). The increasing of the



silicide block (SB) length in the drain ballasting region provided practically no improvement of the surge pulse passing level in spite of the significant effect on standard component and even HMM test results (Table 2.3). The description of the SNMOS and SCR ESD devices is presented in Chap. 3.

## 2.2 HMM Testing

A significant progress for the on-chip system level IC protection design was achieved by implementing the component and on-wafer test methods. These methods simulate the system level ESD discharge pulse waveforms with a margin which is acceptable for initial design steps. In particular, an understanding of the IEC 61000-4-2 standard requirements led to the development of a component-level test method using the same stress waveform.

The system-level ESD test standards do not guide directly how to apply system-level ESD stress on the IC component level. Nevertheless, there was a critical need of characterizing components and on-chip ESD clamps with a system-level equivalent stress. Thus, a new measurement method—the Human Metal Model (HMM), has been proposed. While the system level IEC and ISO standards for the contact discharge define the tests for the system ports, the HMM methodology is on the contrary primarily targeting the evaluation of the IC pin robustness. It was also successfully used for the evaluation of the standalone ESD solutions placed on test chips.

The methodology is done under the assumption that, if the HMM pulse waveform repeats the system level waveform, a certain passing level correlation can be expected. Several studies demonstrated that in many cases there is a correlation between standard system level gun test and HMM stress [51]. In spite of a number of reported miscorrelations, today HMM represents the most useful approach for the on-chip system-level design. This triggered the release of many industrial HMM laboratory tools [28, 29] now offered by variety of vendors. The details of the setup and associated issues are described in the following sections.

A complementary angle of view on the HMM practice is related to the propagation of the system level stress across the PCB. This results in a possible current overstress at the IC pins directly interfacing with the system port under stress. It is logical to expect that the ability to withstand this system level test is not automatically guaranteed just by the passing the standard component level stress (HBM, MM, CDM). Instead, such capability should be added by the dedicated on-chip design, discussed in Chaps. 3 and 4.

HMM tester applies stress waveforms with similar characteristics to the IEC 61000-4-2 standard waveforms. Perhaps the only parallel in physical understanding between the HMM test and the standard component level tests can be roughly drawn by a physical representation of HMM current pulse waveform as a superposition of the component-level CDM pulse, representing the first peak, and HBM pulse, representing the second peak, after both scaled in a right proportion. Although certain attempts can be made to find the correlation factors between

HMM pulse and these two component pulses unlikely this approach can provide a replacement for HMM. This is mainly because the current paths of the single pin stress CDM are not in general the same to the path during HMM stress. Also the duration of an HBM event is much larger than the duration of *e.g.* the second peak current during an HMM event.

### 2.2.1 HMM Setups with ESD Gun

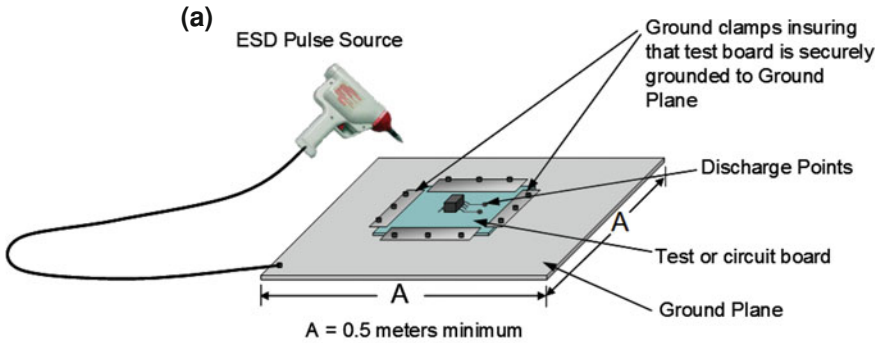
The HMM standard practice document [30] describes three different measurement setups to apply the stress waveform to a component. The setups are using both gun type and  $50\ \Omega$  pulse generators. The gun based setups include an IEC 61000-4-2 compliant ESD gun as a stress source. The packaged DUT is placed on a PCB which is mounted on a larger ground plane. The ground plane of the PCB and ground plane of the test setup thereby form a continuing ground plane (Fig. 2.18a). When stress is applied to the DUT, the ground wire of the ESD gun is connected to the ground plane of the measurement setup. A variation of the setup uses a vertical ground plane (Fig. 2.18b) which allows the shielding of the measurement equipment from the electromagnetic fields send out by the ESD gun during discharge.

Both setups allow the application of HMM stress when the DUT is powered up. In this case the supply pins of the DUT should be equipped with a by-pass capacitor to ground to decouple the supply line.

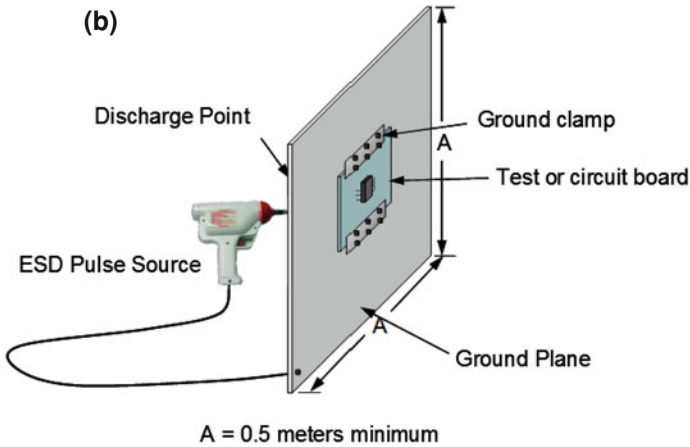
Several miscorrelation cases between different ESD gun models have been reported [31–33]. A common reason for most of the miscorrelation is related to the rather flexible tolerance range of the waveform parameters defined in the standard. For example the amplitude and rise time of the IEC 61000-4-2 stress current are defined with rather big tolerance of 30 % for the currents after 30 and 60 ns. Combined with the 25 % acceptable range for the rise time of the initial current peak it is logical to assume that different model ESD gun pulses might impact the passing level at the same equal conditions [33, 34]. In addition the electro-magnetic field around the discharge point depends strongly on the shape of the ESD gun discharge tip. Thus the gun based HMM measurement setups partially include some of the limitations related to the flexibility of the IEC 61000-4-2 compliant ESD guns.

### 2.2.2 50 Ohm HMM Setup

The alternative third HMM setup uses a  $50\ \Omega$  ESD pulse source (Fig. 2.19). The stress is applied with coaxial lines to a test board with the DUT mounted on. This setup has been originally proposed in order to improve repeatability of the applied stress pulses [35], to remove the ESD gun issues and to enable a reliable measurement of voltage and current during the HMM stress. Similar to the other HMM setups a DUT can be tested when powered up. In this case the supply pins of the DUT are equipped with a by-pass capacitor to ground to decouple the supply line.



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**Fig. 2.18** HMM measurement setup with ESD gun and horizontal coupling plane (a) and with ESD gun and vertical coupling plane (b) [30]

The impact of reflections in  $50 \Omega$  HMM setups is an important issue. The source impedance of the  $50 \Omega$  HMM tester is much lower than for ESD guns. The difference in source impedance impacts the test results in  $50 \Omega$  HMM setups. The on-state of ESD protection devices typically results in a low impedance of a few Ohms. This causes an impedance mismatch between the turned-on device and the tester source impedance.

The HMM stress current is partially reflected back to the pulse generator which causes a disturbance of the pulse generator circuit (Fig. 2.20). This results in an appearance of a negative current after the decay of the HMM stress current. The current waveforms with and without matching DUT resistance become different (Fig. 2.21). Those reflections can impact the device failure level. Thus, there are miscorrelations in comparison to testing with an IEC 61000-4-2 discharge circuit



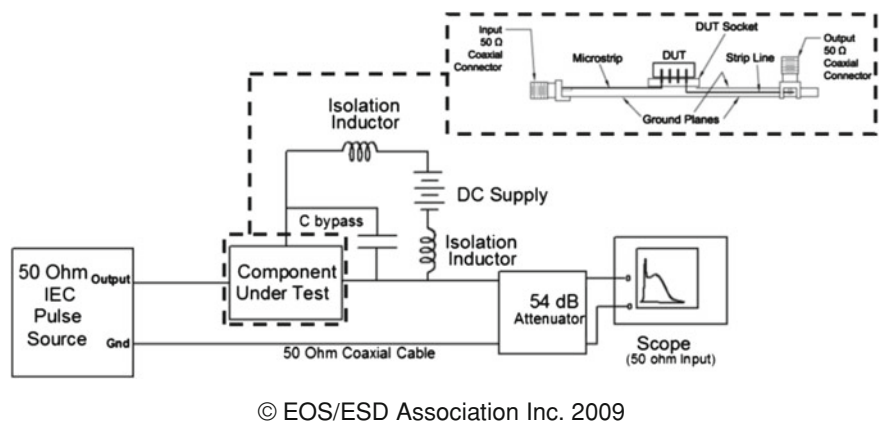


Fig. 2.19 50 Ω HMM setup [30]

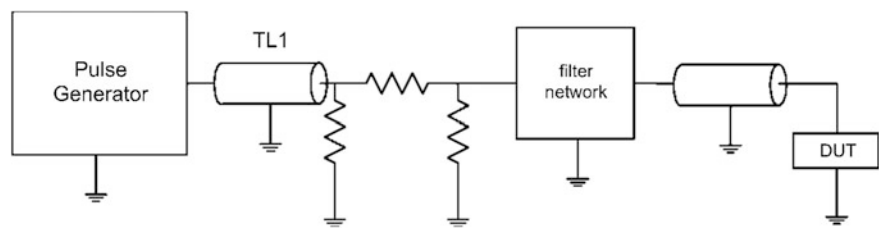


Fig. 2.20 Principle schematic of a 50 Ω HMM setup; TLI one transmission line for pulse shaping

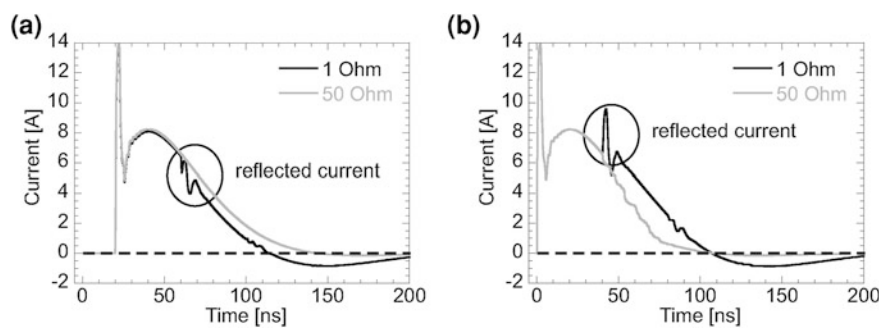
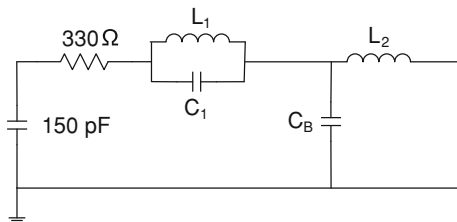


Fig. 2.21 Simulation of the impact of the DUT impedance on reflections in 50 Ω HMM testers: current through DUT (*left*) and current through TL1 (*right*); DUT represented with 1 and 50 Ω resistance

as HMM stress source. If a matched 50 Ω impedance is connected as DUT, then these disturbances do not occur. A detailed analysis of this phenomenon is provided later in this chapter.

**Fig. 2.22** Equivalent schematic of a  $330\ \Omega$  HMM discharge circuit



The HMM setup with an IEC 61000-4-2 discharge circuit (Fig. 2.22) has an impedance of  $330\ \Omega$  which is similar to ESD guns. Hence type of reflections as observed in  $50\ \Omega$  HMM setups cannot occur. The main advantage of this HMM tester over any ESD gun is the compact form factor of its discharge module. It can be conveniently mounted into wafer-level measurement setups. This enables HMM characterization in a very early stage during the ESD protection design. Additionally the design of the module limits the radiation of electromagnetic fields during the HMM test. Alternatively, the discharge can be applied via connectors to application boards. The stress current complies with the IEC 61000-4-2 standard and the HMM standard practice.

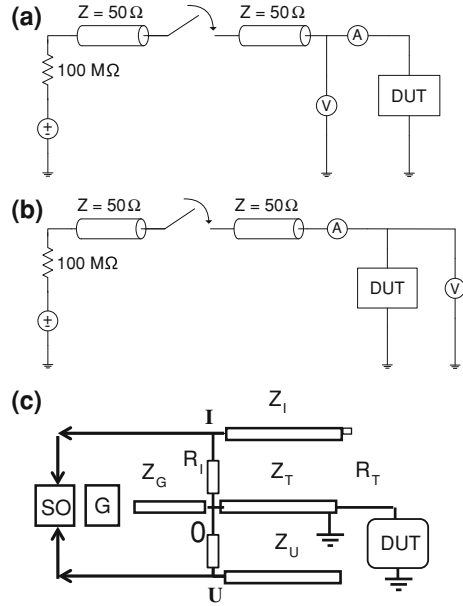
## 2.3 Transmission Line Pulsed Characterization

Passing ESD qualification level for devices and systems under test is a primary goal of any ESD design. However it would be rather difficult to rely only on the passing level during the development of ESD solutions and ESD case studies. Neither capturing of the current and voltage waveforms is always simple nor an easy way to run comparative and conclusive evaluation of ESD solutions and the internal circuit response. Therefore Transmission Line Pulsing (TLP) I-V characterization becomes one of the major steps in the on-chip development process. After more than two decades of evolution the TLP methods have significantly improved. Many tools have been released by test equipment vendors and are now widely applied both on the component and system level evaluation. The TLP I-V characteristics measurement methodology including challenges and pitfalls related to the on-wafer measurement techniques are addressed in this section.

### 2.3.1 TLP Test Method

TLP testing has been introduced for the first time in [36]. Today, commercial TLP testers are available from several vendors and provide a variety of user friendly features and GUIs. The original motivation for introducing TLP was to have a measurement setup which allows the device characterization and the capturing of voltage and current in the HBM time domain. Since then, it became the most

**Fig. 2.23** Simplified diagram of two typical TLP experimental setups: Time Domain Reflected (TDR) TLP (a) and Time Domain Transmission (TDT) TLP (b) and simplified diagram for the voltage and current measurements by summation of the reflected pulses (c)



important component-level ESD characterization tool for obtaining the device parameters which are required for the design of on-chip and off-chip ESD protection circuits.

One typical TLP setup is the Time-Domain Reflected (TDR) TLP measurement setup (Fig. 2.23a). Certainly the voltage measurements include the probes with substantial attenuation. A transmission line of a certain length is charged by a high-voltage source. The length of the transmission line defines the width of TLP pulse. When the switch is closed the transmission line is discharged to the DUT. The incident and reflected voltage and current in time are measured with an oscilloscope. Typically the delay between incident and reflected waveform is not long enough. Therefore incident and reflected waveforms can be seen “overlaid” on the screen of the connected oscilloscope. The current and voltage at the DUT are obtained by adding incident and reflected data. This is done either in the control software of the TLP tester and/or during processing of the obtained waveform data.

The second typical setup is the Time-Domain Transmission (TDT) TLP measurement setup (Fig. 2.23b). Like before a transmission line is discharged to a DUT. The incident and reflected current in time are measured with an oscilloscope. The voltage, however, is measured directly at the device under test. The TDT setup can be also compared to a Kelvin type of measurement setup as the voltage is not measured through the same wire where the stress current is flowing.

The principle of the voltage and current measurement with only 2-pin DUT connection is illustrated in Fig. 2.23c. The main pulse from the generator G is propagating in the line  $Z_G$ . In the point “0” two small fractions are split out from the

main pulse that is continuing to travel in the line  $Z_T$  toward DUT. These two small fractions are routed into the coaxial lines  $Z_I$  and  $Z_U$ . The attenuated pulses are obtained using 1/200 dividers formed by the corresponding resistors  $R_I$  and  $R_U$  into. All three coaxial lines  $Z_I$ ,  $Z_U$  and  $Z_T$  are matched to the same length thus introducing the same propagation delay time. The line  $Z_I$  has with the opposite end shorted to the ground, while the coaxial delay line  $Z_U$  with the open circuit (Fig. 2.23c).

After corresponding propagation line delay time each split pulse reflected from opposite ends of the lines  $Z_I$  and  $Z_U$  arrive at the points  $I$  and  $U$ , respectively meeting with the new two fraction of the main pulse reflected from the DUT. Summation of the DUT pulse with the pulses in the reflected pulses in the lines with shorted and open circuit ends form the signal proportional to the current and voltage through the DUT, respectively. This signal are brought to the two channels of the oscilloscope SO.

In case of low voltage devices at high current the voltage signal at DUT at high current is the result of subtraction of rather big values of the reflected signals. This significantly impacts the accuracy of voltage measurements. To improve the accuracy a direct voltage probe with corresponding transmission line delay can be used as an alternative (Fig. 2.23b).

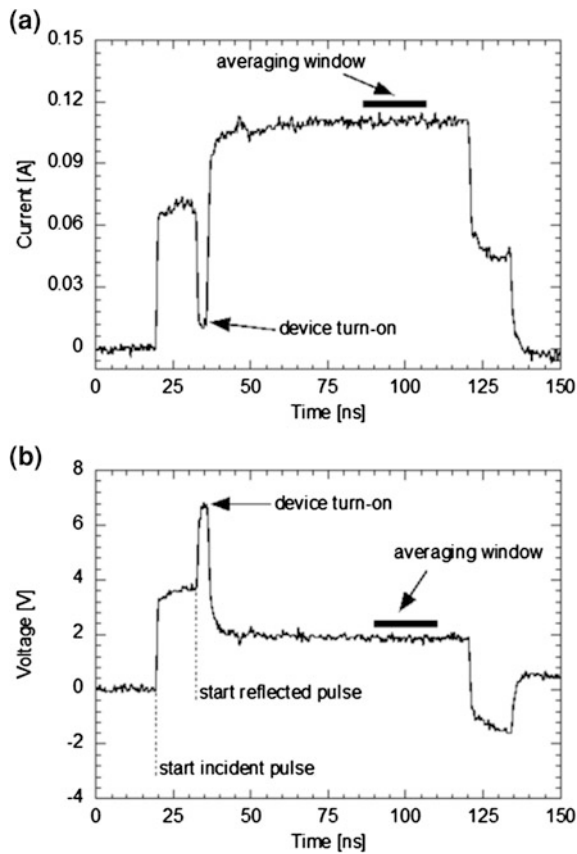
The typical current and voltage waveforms of the TLP discharge pulse are rectangular with a user-defined rise time and pulse width. TLP pulses are usually 100 ns wide and rise within 200 ps to 10 ns which is partly equivalent to the rise times of the HBM current (Fig. 2.24).

To obtain the quasi-static DUT response the TLP pulses are analyzed for each stress level only in a selected time window that is usually selected between 70 and 90 % of the TLP pulse width. In this time window voltage and current are averaged (Fig. 2.25, left plots). By plotting each averaged voltage and current value the TLP I-V curve of a DUT is obtained after the corresponding multiple zap steps (Fig. 2.25, right).

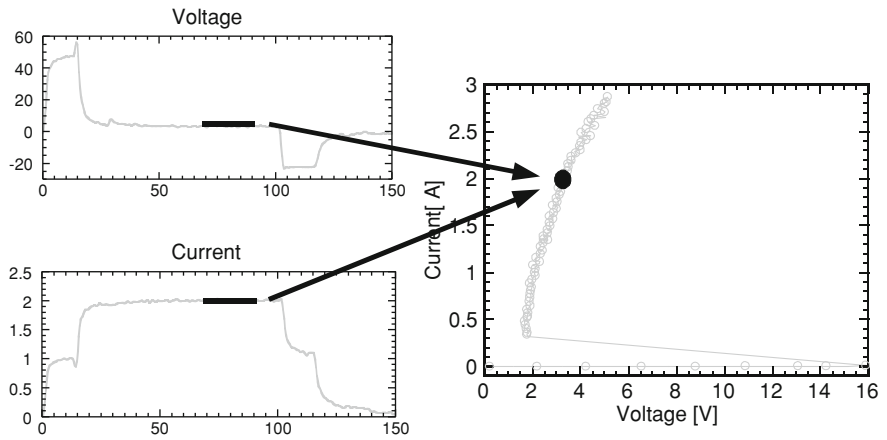
TLP evaluation is used not only for the confirmation of the maximum current level provided by the clamp but also to deliver insights on the quasi-static characteristics of the ESD device. This is achieved by extracting several figures of merit from the TLP I-V characteristics. In industrial testers the TLP test is combined both with the functional leakage test and with the automatic bias conditions used for example for pulsed SOA measurements of the standard devices [37]. The leakage current is measured between each pulse (Fig. 2.26) under power down condition of the controlled pins prior to the measurement.

From a physical point of view, the ESD device in snapback mode operates similarly to a voltage-controlled switch with a resistive load. The first pair of parameters, the triggering voltage  $V_{TI}$  and triggering current  $I_{TI}$ , is used as figures of merit for the turn-on of the device into snapback. These parameters are important when defining the device turn-on within a so-called *ESD Protection Window* and to guarantee that during normal circuit operation the device does not accidentally turn-on thereby having the risk for transient induced latch-up.

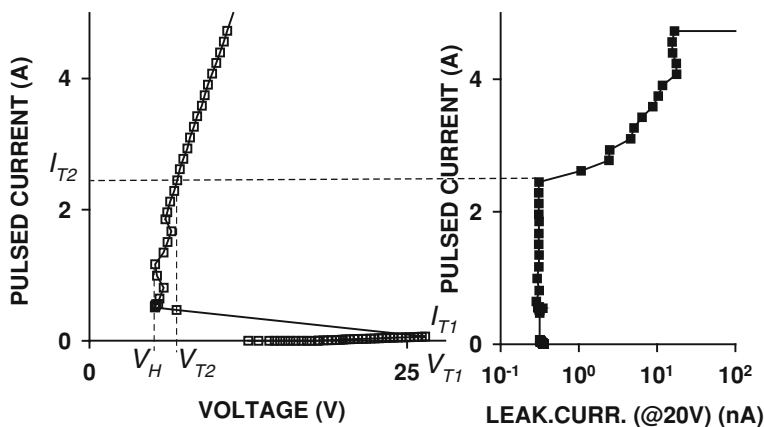
The next important figure of merit parameter is the holding voltage  $V_H$ . This parameter depends on the load impedance of the TLP tester and the snapback



**Fig. 2.24** 100 ns TDR TLP waveforms: **a** voltage and **b** current; captured during TLP stress on a low-voltage-triggered SCR



**Fig. 2.25** Measuring TLP I-V curve: TLP waveforms (*left*) and extracted TLP I-V curve (*right*)



**Fig. 2.26** Typical double plot for TLP snapback characteristics with major figures of merit indicated

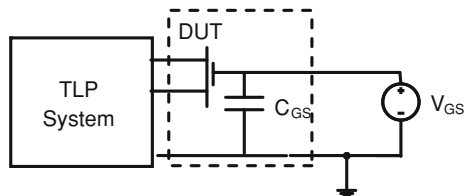
voltage of the device. Thus, for example, when using a  $50\ \Omega$  TLP system, the measured holding voltage generally is higher than the real device holding voltage which can be obtained by characterizing it with a waveform HBM system or a DC measurement.

After turn-on into the high current state, the device provides a certain on-state resistance due the internal positive feedback and a saturation region that determines the voltage waveform in the ESD pulse domain at a high current level. Usually, this parameter is an important practical criterion. For standard package level specifications it can be defined, for example for 1.33A (2 kV HBM). Finally, at a certain stress level, the physical limitation of the device results in irreversible changes to the devices structure. This equivalent TLP I–V curve point is usually referred to as  $I_{T2}$  and  $V_{T2}$  (Fig. 2.26)

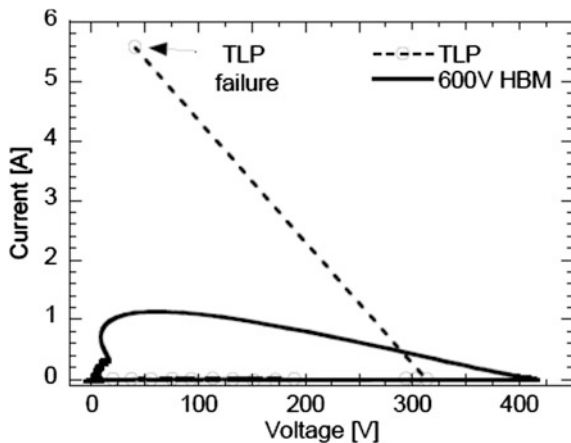
In general the parameters  $I_{T2}$  and  $V_{T2}$  cannot be seen from the pulsed I–V characteristic alone. Even after irreversible changes the TLP I–V curve still may show the same trend. A separate functional test is usually required to establish the detection of device failure. In most TLP systems, this functional test is usually implemented by a simple leakage current measurement at a given voltage level with a defined parametric failure criterion, for example, a leakage deviation of one order of magnitude from the original level. For example, in the case of data for the 20 V snapback device presented in Fig. 2.26, the left plot for pulsed I–V shows no peculiarity associated with the irreversible failure that is already observed in the leakage current obtained with the functional test at an  $I_{T2}$  current level of  $\sim 2.5\text{A}$ .

TLP characteristics are very convenient for comparative analysis. They are widely used across this book both to represent the device parameters, pulsed SOA, and for the debugging of the analog circuit product pin characteristics. Pulsed SOA in the ESD time domain (further as ESD SOA) is a SOA measured for specific pulse conditions. In principle, this SOA depends on the specific pulse waveform.

**Fig. 2.27** Circuit diagram for setup for pulsed SOA evaluation using TLP measurements



**Fig. 2.28** Overlay of TLP I–V and HBM I–V curves taken from the same device for the stress level 0.6 kV

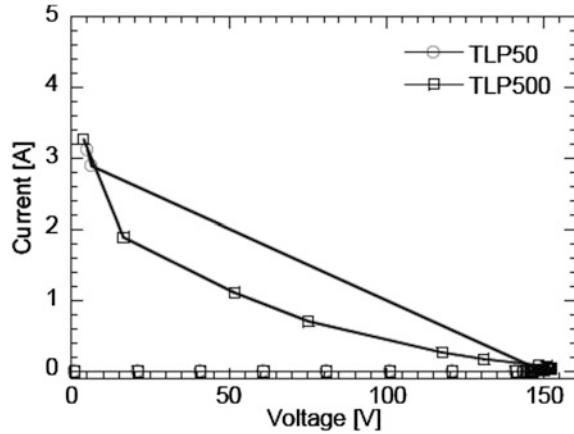


Known miscorrelation expected a different SOA for HBM, MM, and CDM, as well as for IEC and CDE system level test pulses. The most common characterization technique for ESD SOA evaluation combines TLP measurements with constant gate bias (Fig. 2.27). This technique applies TLP pulses to a DUT, for example, NMOS devices under constant gate bias on the gate electrode (Fig. 2.27). The setup includes a constant voltage source to provide gate-source bias, base-emitter bias, or current. TLP stress is applied under different bias conditions to obtain the DUTs SOA.

The impact of the TLP tester impedance on the failure level cannot always be neglected. One example is the so-called very high voltage (VHV) switching devices which can operate at voltages of several hundreds of volts up to more than one kilovolt. *E.g.* triggering a 600 V SCR device into the snapback mode in a 50  $\Omega$  TLP setup can result in a current level above 10 A. This may be much higher than the current capability of the device. An example of a device that passes 2 kV HBM stress (1.33 A), but fails the 50  $\Omega$  TLP stress is presented in Fig. 2.28. Another important issue for the high-voltage devices is the precise measurement of the holding voltage that is usually hidden by the load line of the 50  $\Omega$  TLP tester.

An experimental methodology to overcome this issue is either to increase the source impedance of the TLP tester [38] or to use a multi-level TLP tester [39]. The 100 ns TLP I–V curves of a HV nLDMOS-SCR were obtained with a 50 and a 500  $\Omega$  TLP tester (Fig. 2.29). The device snaps back to a higher current value

**Fig. 2.29** 100 ns TLP I–V curves obtained with different TLP tester impedances for a high-voltage nLDMOS-SCR



when using the 50  $\Omega$  tester. Due to the different load line the current after snapback is lower when using the 500  $\Omega$  tester. When using the 500  $\Omega$  system even points between the device turn-on around 150 V and the completed snapback around 3 V can be captured.

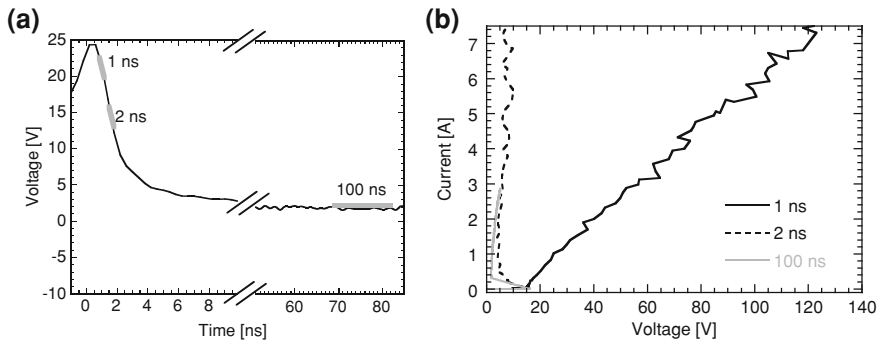
### 2.3.2 Very Fast TLP Test Method

The very fast TLP (vfTLP) test methodology has been proposed for the first time in [40]. The motivation for the vfTLP testing is to enable the device pulsed characterization and voltage/current measurement in the CDM time domain. In the standard practice document [41] vfTLP is defined as a TLP stress with less than 10 ns pulse width and 100–500 ps rise time. The fast rise time and short pulse duration allows the measurement of transient device behavior in the nanosecond time domain.

The TLP and vfTLP I–V characteristics of the same device are different due to the pulse length. Conventional 100 ns TLP measurements represent a quasi-static state of a device. The vfTLP I–V curves represent a more dynamic device behavior which is related *e.g.* to the DUT triggering delay (Fig. 2.30).

The quasi-static characteristics of the device are accessed by means of TLP I–V characteristics analysis. TLP waveform analysis enables the study of the transient device behavior during ESD stress. Because of the transient nature of the TLP pulses calibrating TLP and vfTLP measurements is an important step to obtain accurate testing results. For example in on-wafer TDR TLP setups the parasitic elements of the connection cannot be neglected due to distortion of the measurement results. The probe needles contain the main contributing parasitic elements. They are represented by their resistance  $R_S < 1 \Omega$  and their inductance  $L_S \sim 10\text{--}20 \text{ nH}$  (Fig. 2.31) [42, 43].





**Fig. 2.30** Illustration of different averaging windows during extraction of vfTLP and TLP I-V curves: **a** location of averaging windows and **b** I-V curves based on the different averaging windows

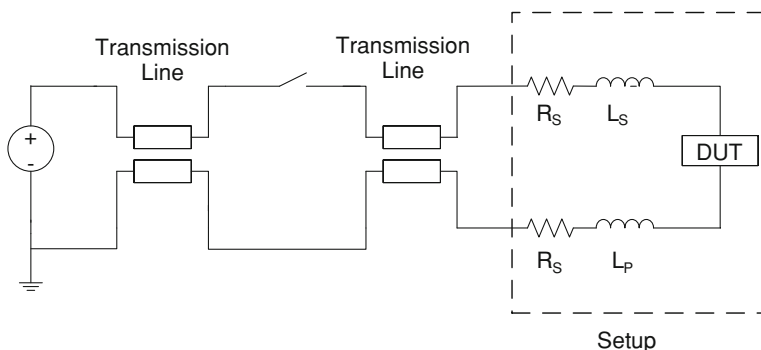
In the high current region of a TLP I-V characteristics the parasitic resistance of the probe needles causes a significant parasitic voltage drop due to the needle resistance  $R_S$ . The additional voltage drop brings inaccuracy to the TLP waveform analysis. The impact of the parasitic elements must be calibrated out from the measurement data. To take into account the additional voltage introduced by the needle resistance the TLP tester can be connected to a short circuit element. The I-V characteristic is measured as an initial step of the calibration procedure. The slope of the obtained I-V curve equals to the serial resistance of the probe needles. By introducing the corresponding correction to the measurement data the real I-V characteristics at the DUT can be obtained.

A more complex calibration routine for vfTLP testing setups is related to the significantly faster rise time and shorter pulse duration. The corresponding measurement setup with high bandwidth current and voltage probes results in a need for high cost RF probes. Their main disadvantage in case of on-wafer vfTLP measurements is the non-flexible probe pitch. The layout of the on-wafer test structures has to be designed for available RF probe pitches.

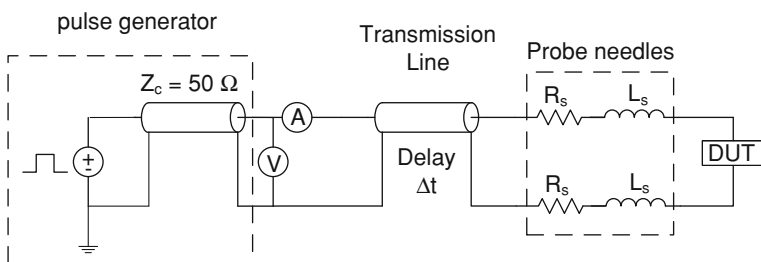
A practical alternative with standard tungsten probe needles requires (Fig. 2.32) a de-embedding of the parasitic from each measured voltage and current waveform using a dedicated calibration/de-embedding methodology [44]. The method is independent of the pulse shape generated by the tester. The vfTLP pulse can feature different durations and rise and fall times.

The de-embedding/calibration methodology uses three loads to characterize the full vfTLP setup: an open circuit, a short and a  $50\ \Omega$  resistor. Voltage and current are captured from those loads. With the data, a model for the needle parasitic and the loss in transmission line are extracted.

The voltage and current for a short load measured by the oscilloscope were calibrated. The needle inductance causes a voltage overshoot of 23 V (Fig. 2.33a). After calibration this voltage overshoot is completely removed. As a result the



**Fig. 2.31** Circuit diagram for on-wafer TLP measurement setup with device under test connection with parasitic resistance  $R_s$  and parasitic inductance  $L_s$  of the probe needle

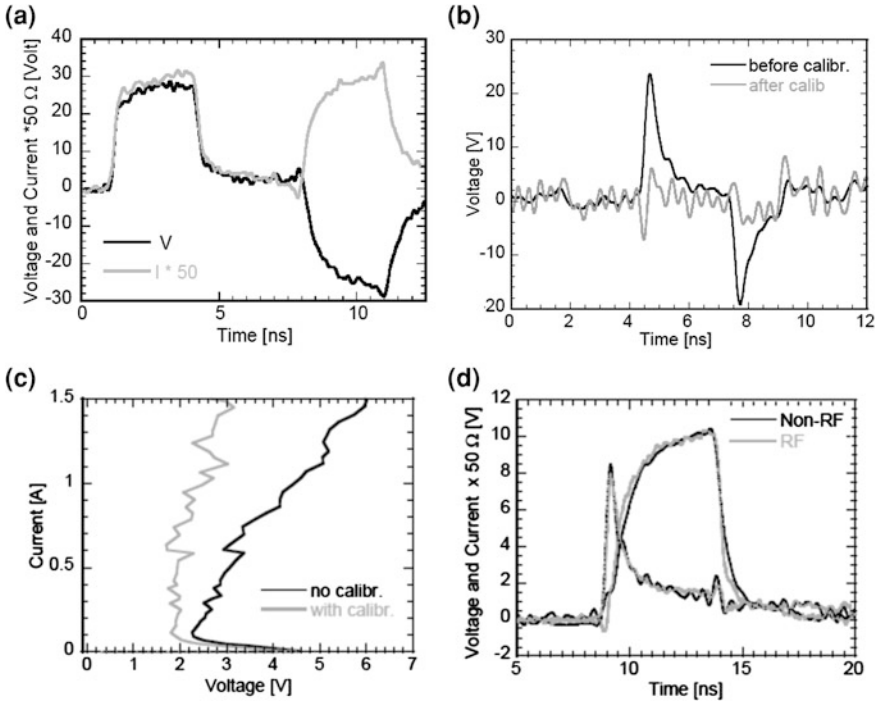


**Fig. 2.32** Circuit diagram for an on-wafer TDR vFTLP measurement setup including loss in transmission line and probe needle parasitic

voltage from a short load has eliminated the voltage overshoot due to the needle parasitic (Fig. 2.33b).

The calibration methodology is applied to vFTLP measurement data, obtained from a diode-triggered SCR (DTSCR). The impact of the test setup parasitic is demonstrated for a diode-triggered SCR (DTSCR) by comparing the vFTLP I-V characteristics before and after the calibration (Fig. 2.33c). Without calibration, both the on-resistance and the holding voltage of the DTSCR are higher. The additional voltage drop due to the parasitic is included in the extracted I-V curve. After calibration, the on-resistance is much lower and a more accurate holding voltage is extracted from the I-V curve. The accuracy of the calibration methodology is validated by comparison of the results with RF probe needles (Fig. 2.33d).

For both TLP and vFTLP testing setups a Kelvin type of setup (TDT) can be used with an additional DUT connection to eliminate the need for a calibration procedure related to the probes parasitic [38]. However due to possible different cable lengths of voltage and current measurement an alignment of the obtained voltage and current waveforms might be required even if a Kelvin setup is used.



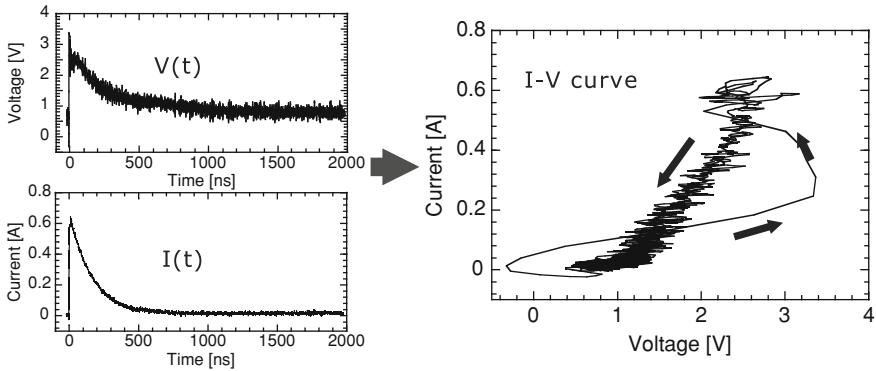
**Fig. 2.33** Application of vTLP calibration routine to measurement data: the voltage and current for a short circuit load (a), comparison of the voltage before and after calibration (b), 3 ns vTLP I–V curve of a diode-triggered SCR (c) and comparison of measured current and voltage waveforms during 5 ns vTLP stress after calibration and when measured with RF probes (d)

## 2.4 Transient Waveforms Characterization for ESD Stress

While TLP characterization and the passing level for ESD pulses are the most used tools for practical design, the analysis of the waveforms for the different transient pulses often can reveal additional useful information and help to debug and optimize different ESD solutions. For example using current and voltage waveform capture techniques for HBM pulses the phase-diagram like HBM I–V characteristic can be reconstructed by plotting instantaneous current  $I(t)$  over  $V(t)$  over the entire HBM time domain (Fig. 2.34).

The analysis of such phase I–V characteristics reveals the region representing the device turn-on, oscillations around the peak current and a stable monotonous part during the remaining 150 ns HBM pulse discharge. The first two regions represent the transient device behavior under ESD stress, whereas the latter represents the quasi-static device pulsed operation.

Similar analysis can be completed to represent the transient characteristics for the system level pulse. To achieve this goal several important aspects must be



**Fig. 2.34** Voltage  $V(t)$  and current  $I(t)$  waveforms captured from a ESD diode at a HBM stress level of 1 kV and plotted phase HBM  $I(t)$ – $V(t)$  characteristics

taken into account. They are related to the required calibration procedures for the waveform capturing, clamp operation specific and the setup itself. These aspects are discussed in this section.

### 2.4.1 Calibration of ESD Waveforms

The example of a calibration procedure is described in this section for the case of HBM tester. The methodology can be also applied to other two-pin component-level tests like MM and HMM.

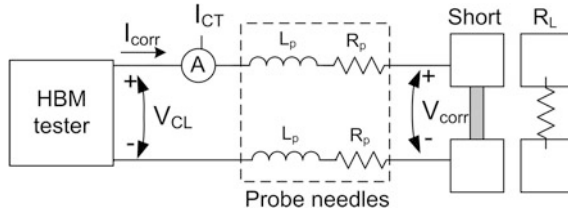
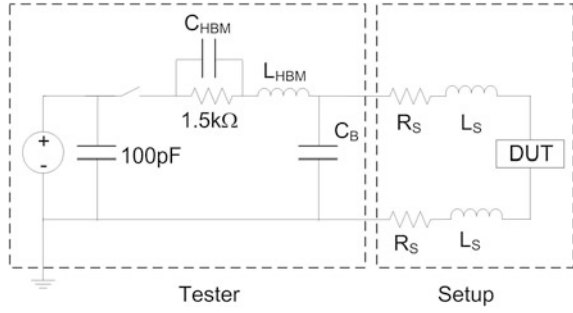
At the standard HBM pulse rise time of  $\sim 2$ – $10$  ns the voltage and current waveform measurement is very sensitive to parasitic elements in the setup (Fig. 2.35). The parasitic elements contributed by the probe needles and test setup cause an additional voltage drop around the current peak and to the linear region of the HBM I–V characteristic. They must be eliminated by an appropriate calibration procedure. The current transformers usually used as current probes have a limited bandwidth, which is between 25 kHz and 2 GHz. This results in distortion of the falling part of the measured current waveform.

To remove this low frequency distortion of the current transformer, the transfer function  $TF$  of the current transformer needs to be determined for the calculation of the real current  $I_{corr}$  out of the measured current  $I_{CT}$  (2.1).

$$I_{corr} = TF \cdot I_{CT} \quad (2.1)$$

This corresponds to a de-convolution problem, where the determination of an unknown input signal is calculated from the measured output signal if the transfer function of the system is known. The methodology allows to extract the transfer function  $TF$ , the needle parasitic resistance  $R_p$  and inductance  $L_p$ . The extracted

**Fig. 2.35** Circuit diagram for an HBM on-wafer test setup with indicated parasitic tester capacitance  $C_{HBM}$ , parasitic tester inductance  $L_{HBM}$ , board capacitance  $C_B$ , probe needle resistance  $R_S$  and probe needle inductance  $L_S$



**Fig. 2.36** Setup for HBM calibration with indicated corrected ‘real’ current  $I_{corr}$ , distorted current measured by current transformer  $I_{CT}$ , measured voltage  $V_{CL}$ , corrected ‘real’ voltage  $V_{corr}$ , parasitic needle inductance  $L_p$ , parasitic needle resistance  $R_p$  and load for calibration  $R_L$

values are calculated from HBM voltage  $V_{cl}$  and current  $I_{ct}$  waveforms captured for given resistive load  $R_L$  and short circuit conditions (Fig. 2.36).

Measured voltage  $V_{cl}$  and current  $I_{CT}$  are aligned in time and transformed to the frequency domain. Two expressions of the transfer function of the current transformer are obtained - one for the load  $R_L$  (2.2) and one for the short (2.3) measurement.

$$TF_{cl}^{load} = \frac{I_{corr}^{load}(\omega)}{I_{CT}^{load}(\omega)} = \frac{V_{cl}^{load}(\omega)}{(R_L + Z_P) \cdot I_{CT}^{load}(\omega)}, \quad (2.2)$$

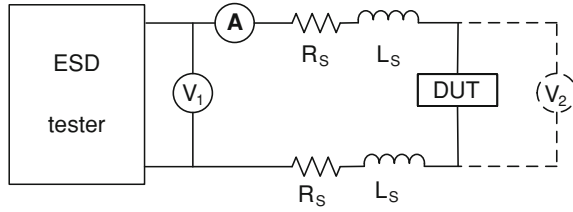
$$TF_{cl}^{short} = \frac{I_{corr}^{short}(\omega)}{I_{CT}^{short}(\omega)} = \frac{V_{cl}^{short}(\omega)}{Z_P \cdot I_{CT}^{short}(\omega)}, \quad (2.3)$$

$$Z_P = 2 \cdot (R_P + j\omega L_P), \quad (2.4)$$

where  $Z_P$  is the impedance of the needles. Both transfer functions are identical as they are obtained with the same current transformer and on the same setup:

$$\frac{V_{cl}^{short}(\omega)}{Z_P \cdot I_{CT}^{short}(\omega)} = \frac{V_{cl}^{load}(\omega)}{(R_L + Z_P) \cdot I_{CT}^{load}(\omega)} = TF. \quad (2.5)$$

From (2.5)  $Z_P$  is obtained as



**Fig. 2.37** Circuit diagram of an ESD on-wafer test setup including parasitic with option Kelvin setup using direct voltage  $V_2$  measurement, where  $R_S$  and  $L_S$  are probe needle resistance and inductance,  $V_1$  tested represents standard voltage measurement

$$Z_P = \frac{V_{cl}^{short}(\omega) \cdot R_L \cdot I_{CT}^{load}(\omega)}{V_{cl}^{load}(\omega) \cdot I_{CT}^{short}(\omega) - V_{CL}^{short}(\omega) \cdot I_{CT}^{load}(\omega)}. \quad (2.6)$$

For a typical on-wafer measurement setup the series resistance  $R_p$  is  $\sim 0.5\text{--}0.8 \, \Omega$  and the inductance  $L_p$  is  $\sim 10\text{--}15 \, \text{nH}$ , extracted per a single needle. Finally,  $TF$  is obtained by substituting (2.6) in (2.2) or (2.3). To obtain the real current through a device under test (DUT), the measured current waveform  $I_{DUTmeas}$  is transformed to the frequency domain and multiplied with the transfer function  $TF$  (2.7). A corrected voltage waveform across the DUT is calculated referring to Eq. (2.8).

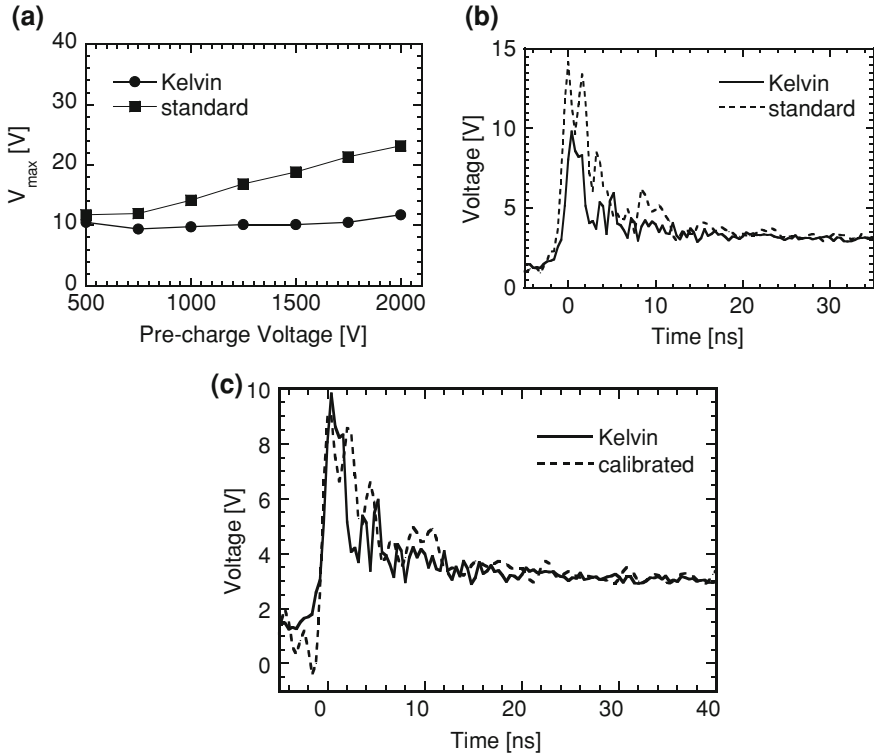
$$I_{corr}^{DUT}(\omega) = TF \cdot I_{meas}^{DUT}(\omega), \quad (2.7)$$

$$V_{corr}^{DUT}(\omega) = V_{meas}^{DUT}(\omega) - Z_P \cdot I_{corr}^{DUT}(\omega). \quad (2.8)$$

Due to limited power of the signal spectrum at high frequencies, the numerator and denominator in Eqs. (2.2) and (2.3) becomes very small. The result is unrealistic values at high frequencies that have to be removed before the IFFT operation. To reduce the noise level additional filtering of the obtained data is required. The corrected current  $I_{corr}^{DUT}(\omega)$  and voltage  $V_{corr}^{DUT}(\omega)$  waveforms are transformed to the time domain. The calibration data is independent of the pre-charge voltage. A calibration needs to be performed only once before a full set of HBM waveform measurements.

The de-embedding of the HBM tester parasitic requires the application of the calibration data to every captured voltage and current waveform. Also the data needs to be filtered to remove the increased noise due to FFT/IFFT operations on the data. As an alternative to the calibration procedure the voltages can be captured in a Kelvin setup [38]. The advantage of the setup (Fig. 2.37) is that the voltage is measured directly at the DUT using a second pair of probes. Since the stress current has a separate path the parasitic voltage drop is not interfering with the voltage measurement thus eliminating the need in calibration.

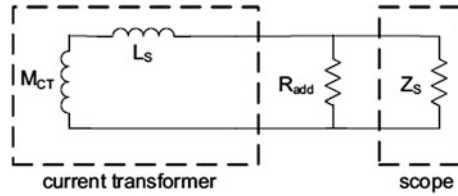
The comparison of the maximum voltage dependence upon the stress level for the peak voltage with and without Kelvin technique is apparent (Fig. 2.38a, b) and less noisy. It can be further used to validate the calibration procedure too (Fig. 2.38c).



**Fig. 2.38** Application of Kelvin methodology for low-voltage-triggered SCR device measurements: maximum voltage versus HBM stress level (a) and voltage waveforms for a 1 kV HBM stress (b) and comparison with the calibration/de-embedding results

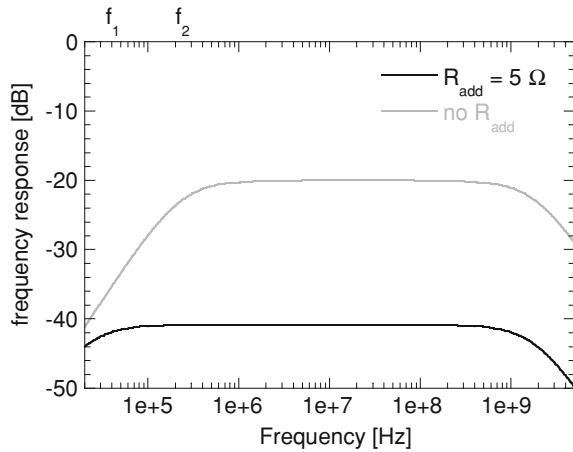
Additionally the frequency response of the current transformer can be modified to improve the bandwidth of the current transformer. Changing the transfer function of the current probe can significantly simplify the calibration procedures. The lower frequency limitation of inductive current probes is changed to a level which is acceptable for the measurements. The equivalent circuit of an inductive current transformer typically used in ESD measurement setups includes the self-inductance and the termination resistance (usually 50  $\Omega$ ) (Fig. 2.39). The formed L–R filter has a lower frequency limit that can be reduced further by adding a low value parallel resistor between the current transformer and the input of the oscilloscope [45].

For example, by adding a resistor of 5  $\Omega$  in parallel to a Tektronix current transformer CT-6, the lower bandwidth limitation is reduced from 250 kHz (datasheet) down to  $\sim 40$  kHz (Fig. 2.40) impacting significantly the measured current waveforms. As a result the negative current part of the current waveform is strongly reduced (Fig. 2.41)



**Fig. 2.39** Equivalent circuit diagram of CT probe with added resistor representing the mutual inductance  $M_{CT}$ , the self-inductance  $L_S$  and added resistor  $R_{add}$  with the input impedance oscilloscope  $Z_S$

**Fig. 2.40** Simulated frequency response of a Tektronix CT-6 current transformer with and without added parallel resistor;  $f_1$  lower frequency limit with added resistor of 5  $\Omega$ ,  $f_2$  lower frequency limit without added resistor



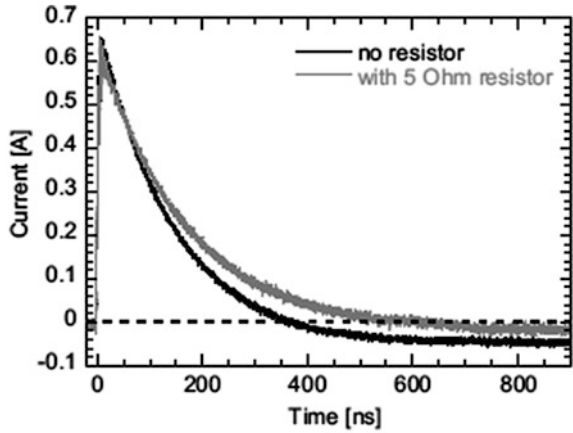
The main advantage of modifying the current probe is the reduced effort during the HBM tester calibration. If a modified current probe is used together with a Kelvin setup no HBM tester calibration is required when measuring voltage and current waveforms during HBM stress. Consequently no FFT is applied to the measurement data and the increase of the noise in the measurement data is prevented.

Once the waveform capture setup is done, the measurements of the transient characteristics can be applied for comparative analysis of the ESD solutions. Such application can be demonstrated on the example of a low-voltage SCR local clamp operation as a function of the driver circuit design. The clamp design includes a diode triggered SCR device. To evaluate the clamp performance an nMOS transistor has been added as a gate monitor device in parallel to the clamp (Fig. 2.42).

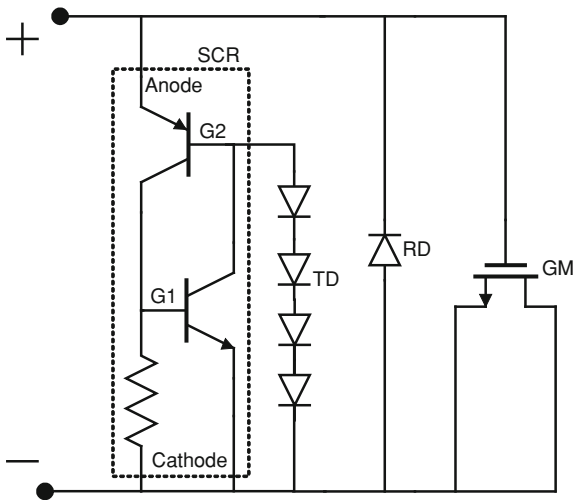
Three different variations A, B and C of the clamp design were used [44] for comparative analysis. The type A was representing the baseline clamp composed from the SCR device and the small width reference diodes. The diode controlled only small local Anode-G2 junction (Fig. 2.42) of the SCR N-base. Thus the diode



**Fig. 2.41** Current waveform into a short load, measured with a current transformer Tektronix CT-6 with and without added 5  $\Omega$  resistor; HBM stress level: 1 kV



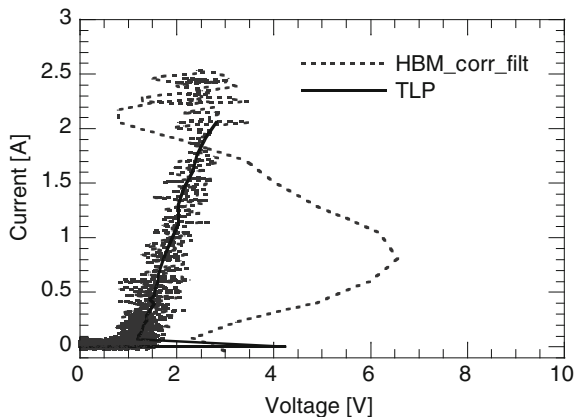
**Fig. 2.42** Schematic of diode triggered silicon-controlled rectifier with gate-monitor in parallel



pull-down circuit was triggering the SCR locally and the delay of the turn-on was expected to provide relatively large clamp voltage overshoot due to the turn-on delay. Type B was representing an improved turn-on speed. This was achieved by wider trigger diodes to control the entire width of the SCR N-base junction connected to the Anode-G2 terminals [47].

Finally the further turn-on speed improvement was implemented in the Type C version, when the conventional shallow-trench-isolation (STI) diodes in the low side reference circuit were replaced by poly-bounded diodes. Due to better on-state performance of the poly-bounded diodes over the STI diodes the SCR triggering speed was expected to be the best among the three types.

**Fig. 2.43** Overlay of 4 kV HBM I-V and 100 ns TLP I-V curves, obtained from device type A



To emphasize the informative value of the waveform capture analysis value the TLP measurements were also performed for all three SCR clamp types with no gate monitor present. As expected, no difference for the three clamp types can be observed in the TLP I-V characteristics. There is a clear matching between the TLP I-V curve and the linear part of the HBM I-V curve. The TLP characteristics of each clamp were similar to the TLP I-V curve of type A (Fig. 2.43). A different result for maximum TLP current was recorded when the gate monitor was connected demonstrating the best performance for clamp type C.

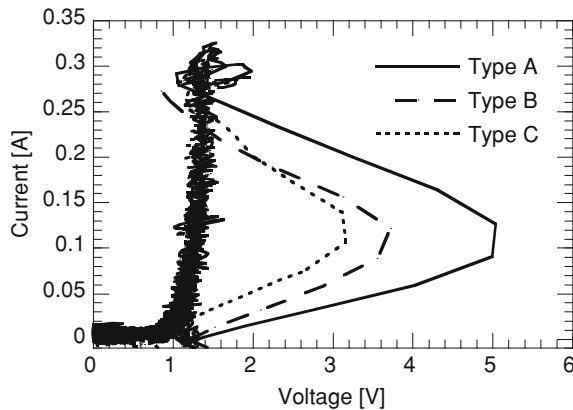
This fact points on a critical role of the voltage overshoot that was damaging the nMOS device gate oxide. The effect can be made visible by an overlay of a calibrated HBM phase I-V characteristics (Fig. 2.43). Unlike in TLP I-V curves the voltage overshoot is visible in a HBM I-V plot.

The comparison of the HBM I-V characteristics for the three clamp design types demonstrated the expected level of voltage overshoot depending on the clamp design (Fig. 2.44). Device type A is the slowest device and provides the highest overshoot voltage. The combination of the DTSCR clamp type A and the gate monitor fails at  $\sim 1.9$  kV HBM.

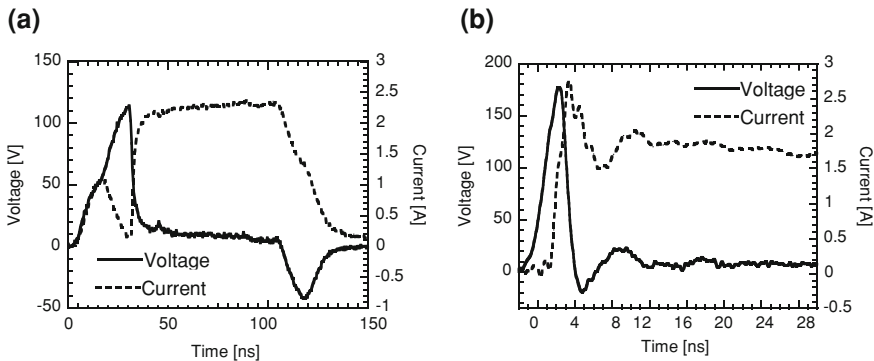
The faster turn-on speed of the type B design results in an increased passing level of 2.6 kV when the gate monitor is connected. Finally the biggest improvement is achieved for clamp type C with poly bounded reference diodes. It generates the lowest overshoot due to fastest turn-on. This leads to an increased HBM robustness in the gate monitor experiment of about 4.6 kV.

### 2.4.2 Transient Characterization of HV Circuits

The high-voltage (HV) ESD devices include longer drift and blocking junction regions in comparison to LV CMOS devices. Therefore a longer carrier transient time from the anode to cathode is involved in the initiation of the conductivity



**Fig. 2.44** HBM I-V curves obtained from the three SCR types for the same HBM stress level of 500 V

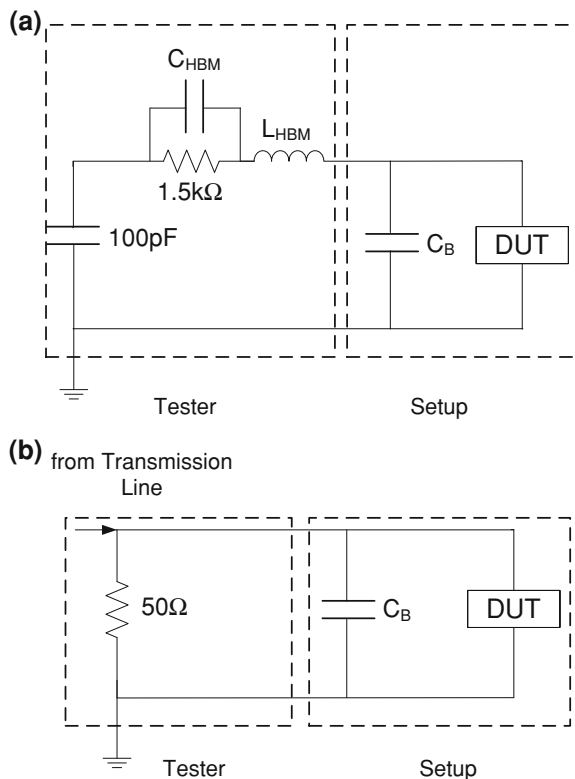


**Fig. 2.45** Calibrated TLP (a) and HBM (b) voltage and current waveform at a stress level of  $\sim 2$  A for 100 V VDMOS-SCR device

modulation process. This results in slower device reaction during ESD (over-) stress, non-uniform triggering, and filamentation [48, 49]. An example of the HV devices realized in a 100 V BCD process technology is discussed below to demonstrate the peculiarities. The voltage and current waveforms were captured using the described calibrated methodologies for TLP and HBM ESD pulses. The DUT was a vertical double-diffused MOS SCR (VDMOS-SCR) device stressed with about 2 A equivalent current (Fig. 2.45).

A comparison of the TLP and HBM waveforms shows that during HBM testing current and voltage overshoots are occurring but not during TLP testing. The TLP trigger voltage is about 120 V (Fig. 2.45a), whereas in HBM an overshoot voltage of about 180 V (Fig. 2.45b) is measured. Additionally, in HBM a delay between voltage and current peak is observed. Through the measured device flows a HBM current with a peak  $\sim 2.7$  A. This is much higher than the nominal expected current

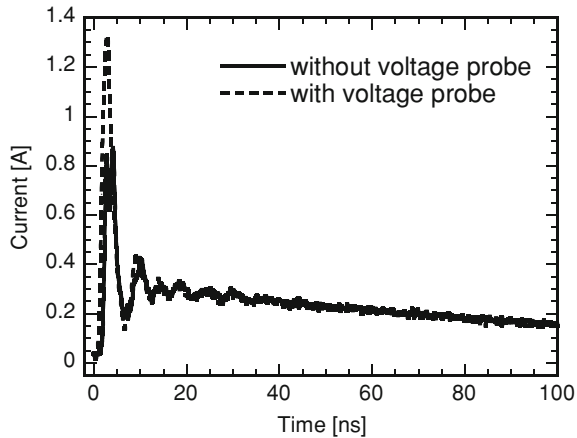
**Fig. 2.46** Equivalent schematic of HBM (a) and TLP (b) setups during device stress:  $C_{HBM}$  parasitic tester capacitance,  $L_{HBM}$  parasitic tester inductance,  $C_B$  test board capacitance



of 2 A for 3 kV pre-charge voltage. What are the underlying reasons for these results? The different testing environment in TLP and HBM influences strongly the transient behavior of the ESD clamp. In a HBM test setup the 100 pF discharge capacitor is in parallel to the board capacitance  $C_B$ . This results in a much larger equivalent capacitance in parallel to the DUT in the HBM testing setup. The much larger equivalent capacitance in the HBM setup interacts with the DUT and causes the described behavior. The equivalent schematics for TLP and HBM measurement setups show different ways how the  $C_B$  capacitor is charged and discharged (Fig. 2.46). In the HBM setup the capacitor is charged to the level of the triggering voltage. During the fast transient triggering of the HV SCR device in high conductivity state, the capacitor  $C_B$  releases the major charge into the SCR device. This generates CDM-like high current peak. The faster rise time of this initial peak is the likely reason for the higher voltage overshoot. In case of TLP stress the  $C_B$  capacitor is driven by the 50 Ω load that limits the current through the capacitor.

It is important to note that the capacitive loading of the voltage probe impacts the measured HBM waveforms. Typically commercially available voltage probes have an input capacitance in the 8–10 pF range. These values in general cannot be neglected. For example in case of the above devices the voltage probe capacitance influences the device triggering and results in a growth of the current amplitude

**Fig. 2.47** HBM current waveforms obtained from the same device with and without connected voltage probe, stress level: 500 V (equivalent to 0.33 A)



from  $\sim 0.8$  A without voltage probe to 1.4 A with connected voltage probe (Fig. 2.47).

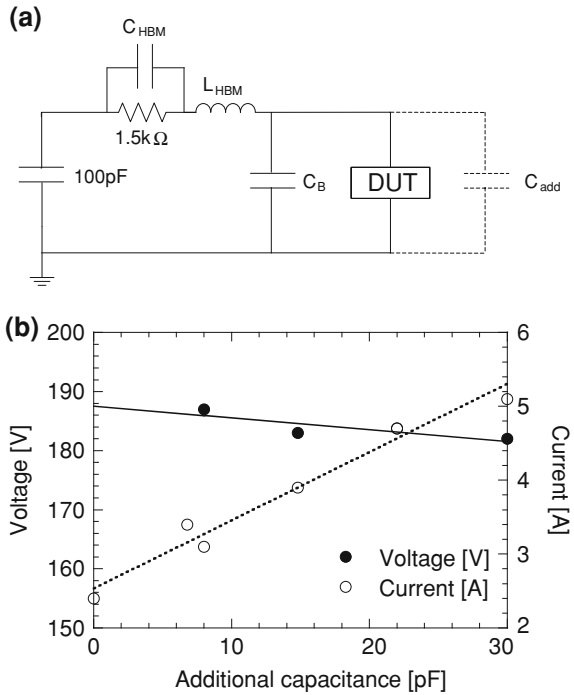
To evaluate the influence of the capacitive load of the voltage probe on the HBM waveform measurements, additional capacitors with different values are placed in parallel to the DUT (Fig. 2.48a). In the described setup for HBM waveform capturing the VDMOS-SCR device peak voltage and current depend on the total capacitance across the device (Fig. 2.48b). The maximum voltage obtained at a HBM pre-charge level of 4 kV remains practically unchanged with increased capacitance, while the increasing capacitive load increases significantly the current overshoot.

### 2.4.3 Transient Characterization with On-Wafer HMM Setups

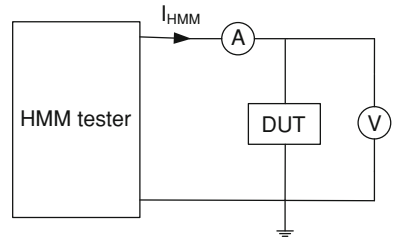
On-wafer HMM testing setups can be used not only to measure the ESD passing level of the components for this pulse. Similar to the HBM methodology, described above, this setup can be also modified to enable the voltage waveform capturing. This enables both the preliminary validation of IC pins during ESD stress and the research and design of ESD devices for system-level ESD protection designs.

Due to the fast rise time of the HMM pulse first peak a more sophisticated setup design is required in comparison to HBM waveform capturing. If the voltage measurement is made across the probe needles a calibration and de-embedding of the test setup parasitic required extracting the real voltage waveforms at the tested device. The much larger voltage amplitudes during HMM stress combined with the faster rise time in general results in much higher voltage overshoots. During voltage capturing the scaling of the oscilloscope is usually set to capture the full

**Fig. 2.48** Simplified circuit diagram for the HBM measurement setup with additional capacitor  $C_{add}$  (a) and peak voltage and current during an HBM stress on a VDMOSSCR device at pre-charge voltage: 4 kV upon the capacitor  $C_{add}$  variation (b)



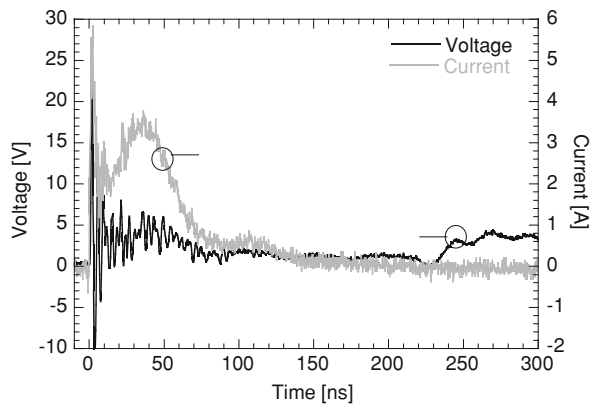
**Fig. 2.49** Simplified circuit diagram for on-wafer HMM setup with voltage measurement in Kelvin configuration



amplitude of the voltage overshoot. This reduces the measurement resolution for the part of the voltage waveform where the device is in the on- or holding state after the first 5–10 ns time domain of the pulse. Hence, the preferable setup for HMM on-wafer measurements is the Kelvin setup (Fig. 2.49). The voltage probe is connected through a second pair of probes to the probe pads of the DUT which decouples it from the HMM current path. This limits or even eliminates the corresponding waveform distortion.

For example, the voltage and current waveforms for on-wafer HMM stress of a nLDMOS-SCR measured in a Kelvin setup provide the realistic values for the triggering voltage of the nLDMOS-SCR, holding voltage and the device turn-off (Fig. 2.50).

**Fig. 2.50** Voltage and current waveforms during on-wafer HMM stress; device: nLDMOS-SCR; 1.5 kV HMM stress level with Kelvin setup voltage measurement

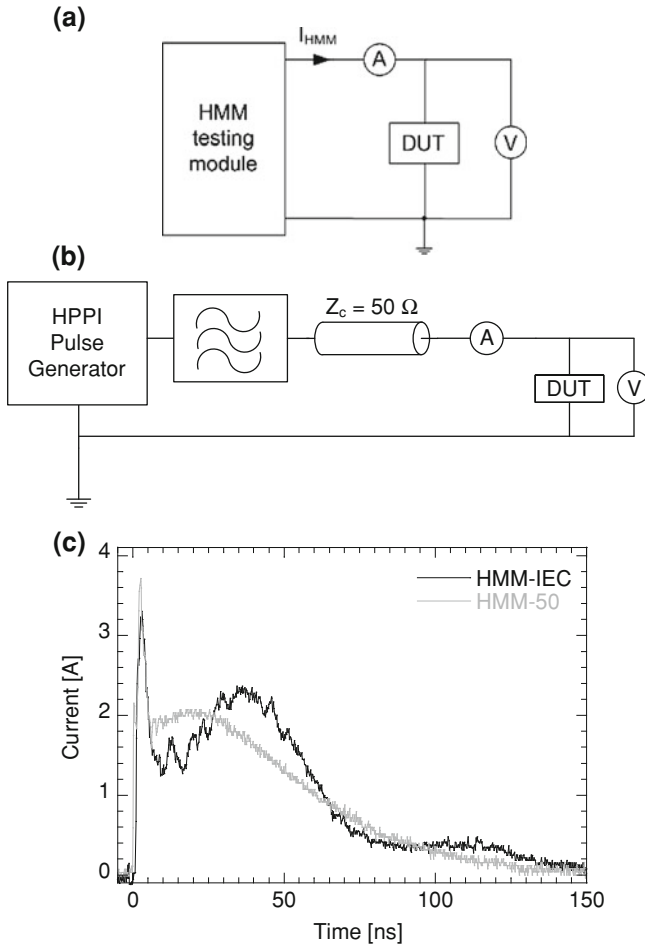


## 2.5 HMM Tester Correlation

The HMM standard practice document [30] outlines methods how system-level ESD stress should be applied to components. “Components” are defined as both single devices and integrated circuits. Two main tester concepts are proposed: HMM testing setup using the IEC 61000-4-2 standard discharge circuit and 50  $\Omega$  HMM pulse generators. The 50  $\Omega$  HMM pulse generators create the stress waveform by shaping a rectangular pulse with transmission lines and filters. In spite of a good correlation reported for 50  $\Omega$  HMM (HMM-50) and ESD gun based testers [50] for standard and advanced LV CMOS technologies, this section demonstrates a miscorrelation case study. The impedance of HMM-50 tester can lead to false results in comparison to testers which use a discharge circuit of the IEC 61000-4-2 type.

### 2.5.1 Test Setup and Device Characterization

The HMM testers used for the comparison are connected to on-wafer test setups. The gun based HMM tester is a HANWA HED-5000 M (HMM-IEC, Fig. 2.51a) tester which uses an IEC 61000-4-2 RC type of discharge circuit to create the stress current [51]. By design, the discharge module of this HMM-IEC tester does not generate the typical electromagnetic fields produced by ESD guns during the discharge. The tester form factor is compatible with on-wafer setup integration which allows a short connection between the discharge module the DUT on the wafer. The second tester is a 50  $\Omega$  HMM tester HPPI 3010C/3011C (HMM-50, Fig. 2.51b) which is based on a modified Transmission Line Pulse tester [52]. The transmission lines and rise time filters are modified in a way that allows the sourcing of a stress current which has a shape within the specifications of the IEC 61000-4-2 standard.



**Fig. 2.51** Block diagrams for HMM-IEC (a) and HMM-50 (b) on-wafer test setups with connected voltage and current probes and comparison of their short circuit current waveforms for 1 kV HMM stress equivalent (c)

In spite of the difference in the output impedance, both testers provide current waveforms into a short circuit load that are compliant to the IEC 61000-4-2 standard. In general the real tester pre-charge voltages cannot be used for the comparison of failure level due to the different methods of creating the ESD stress current. The use of the first peak of the HMM current waveform is neither an adequate figure of merit for the comparison. The amplitude of this first peak strongly depends on the parasitic load of the measurement setup, the DUT impedance and the accuracy of the pulse source. In addition there can be a variation from pulse to pulse when repeating zaps at the same stress level and in the same test setup. For tester comparison, the current after 30 ns is a more reliable



**Table 2.4** Devices under test and process technologies used

Device name	Device type	Technology
LV N-SCR	nLDMOS-SCR	90 nm CMOS
Diode	ESD diode, forward	100 V BCD process
HV N-SCR	nLDMOS-SCR	100 V BCD process
PNP	Lateral PNP	100 V BCD process
NMOS	Grounded-gate NMOS	5 V analog CMOS

**Fig. 2.52** Summary of obtained measurement results; three device groups: *group 1* lower failure level during HMM-IEC testing, *group 2* higher failure level during HMM-IEC testing, *group 3* similar failure level when using HMM-IEC and HMM-50 tester

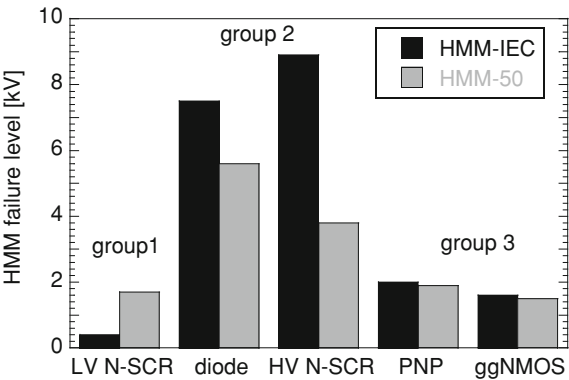


figure of merit. To comply with the standard the current level after 30 ns is expected to be  $\sim 2$  A/kV, although with  $\pm 30$  % variation.

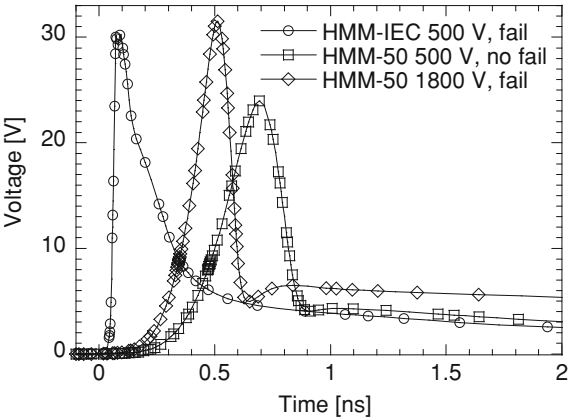
To minimize waveform distortions the voltage waveforms were captured with a Kelvin setup. The selected DUTs are typical ESD protection devices for analog, high-voltage-tolerant and high-voltage/smart power applications (Table 2.4).

The experimental results obtained from all devices can be subdivided in 3 groups based on their correlation between the HMM-IEC and the HMM-50 testing results (Fig. 2.53). The lateral PNP and the NMOS show similar failure level for both testers (group 3). The diode and HV-SCR devices fail at two times lower passing level when using the HMM-50 tester (Group 2, Fig. 2.52). In contrary the LV N-SCR device fails at substantially lower level when using the HMM-IEC tester.

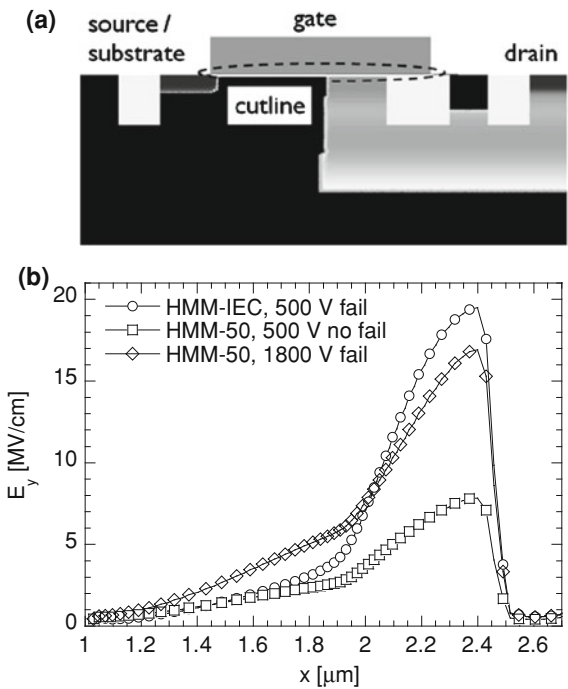
The difference in failure level for the LV N-SCR (0.5 kV vs. 1.8 kV) can be explained by the gate oxide breakdown effects due to a faster rise time of the HMM-IEC tester. To support these conclusions mixed-mode simulations with DECIMM™ [19] are carried out. The models of the two HMM tester are implemented as well as the device TCAD model. The simulated voltage waveforms (Fig. 2.53) for the same equivalent stress level show a smaller voltage amplitude and a slower rise time with the HMM-50 tester suggesting less gate oxide stress.

To compare the impact of the HMM tester on the GOX stress the vertical electrical field across the gate oxide (GOX) was also extracted from the device-

**Fig. 2.53** Simulated voltage waveforms across the low-voltage LV N-SCR during triggering when stressed with different HMM tester; stress level: equivalent stress level

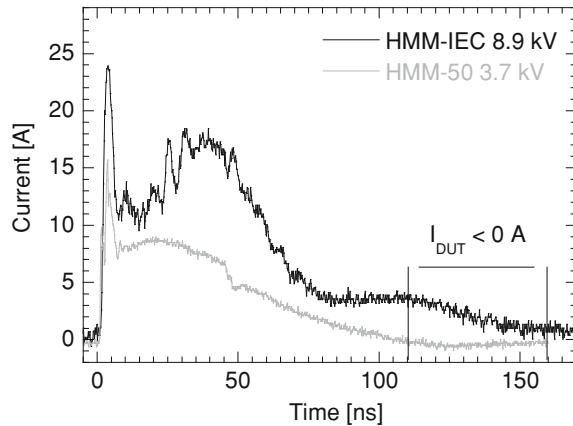


**Fig. 2.54** Simulated cross section of the LV N-SCR (a) and simulated vertical electrical field through GOX for different HMM testers and equivalent stress level (b)



circuit mixed-mode simulations. The simulated cross-section of the LV N-SCR (Fig. 2.54a) was used to extract the maximum vertical electrical field across the GOX at different stress levels. For HMM-IEC tester pulse the electrical field is significantly exceeding the value of the HMM-50 tester for the same stress level. The peak value correlation of the 500 V HMM-IEC is matching the corresponding

**Fig. 2.55** Measured HMM current waveforms at (equivalent) failure level for the high-voltage ESD diode when stressing with both HMM testers

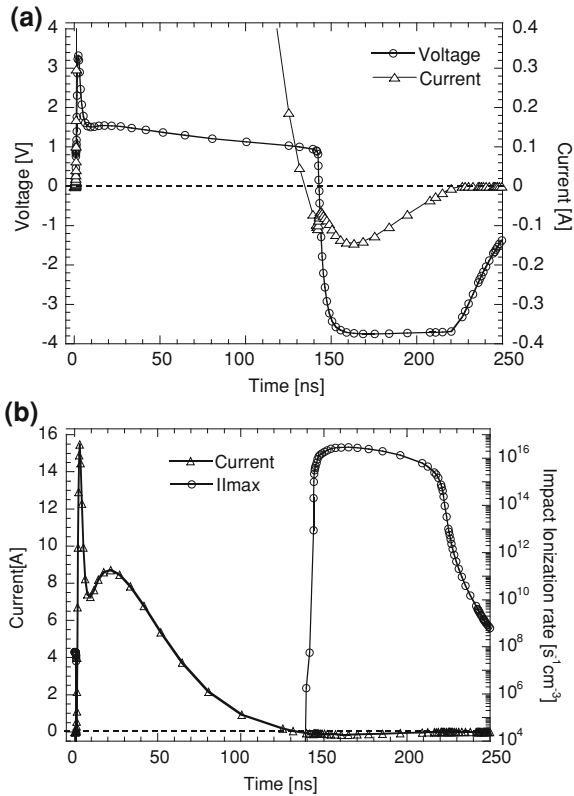


value for 1.8 kV HMM stress which supports the conclusion of the failure cause. GOX breakdown occurs because of the faster rise time of the HMM-IEC tester.

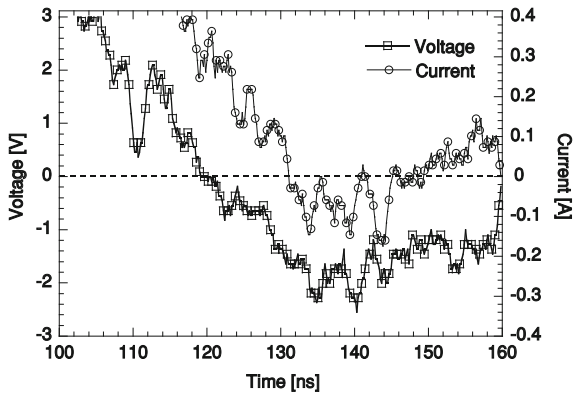
A different reason for the miscorrelation was derived for the HV ESD protection diode for 100 V applications. The device passed 8 kV HMM-IEC tester stress, but failed below  $\sim 3.7$  kV during the HMM-50 tester stress. This unexpected result was explained by examining the current waveform. A negative current through the diode at the end of the pulse was observed as a result of reflections at the  $50\ \Omega$  HMM transmission line. The low on-state resistance of the diode causes an impedance mismatch with the  $50\ \Omega$  source impedance of the tester. Part of the current through the DUT is reflected back into the HMM-50 tester [52]. The observed negative current forces the diode to switch fast from the forward into the reverse biased state. When switching from forward to reverse bias, the excess minority carriers, collected and stored in the diffusion capacitances during forward conduction, need to be discharged. This takes a finite time for the reverse recovery. It is visible in the negative part of the measured current waveform as a constant negative current flow (Fig. 2.55). During this reverse recovery time the diode conducts although the voltage across the device is much lower than the reverse breakdown voltage of 150 V. The amplitude of the reverse recovery current is high enough to cause a failure of the diode since reverse biased diodes can only withstands very small current densities.

Mixed-mode TCAD simulations are done for the same geometrical parameters and doping profiles to understand and visualize the reverse recovery and resulting stress in the device. During reverse recovery, the diode junction is in the transition to the reverse biased state. The external negative voltage enforces the built up of a high electrical field across the junction (Fig. 2.56a), the electrical field stimulates impact ionization Fig. 2.56b) and at certain HMM stress levels the impact ionization leads to avalanche breakdown. The resulting current flow results in a current density which exceeds the limits of the reverse-biased diode and causes device failure.

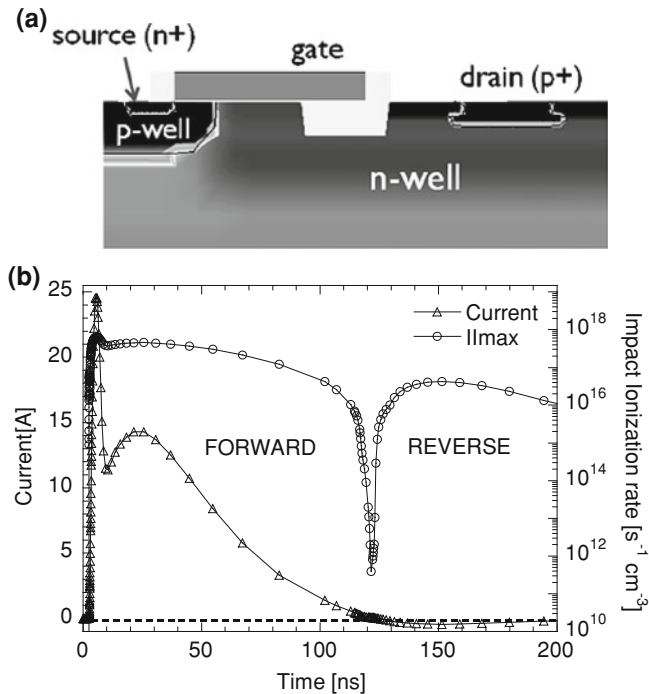
**Fig. 2.56** Mixed-mode simulation of ESD diode during HMM stress applied with the HMM-50 tester for the current and voltage (a) and the current and impact ionization rate (b) at HMM stress level 3.7 kV (equivalent)



**Fig. 2.57** Measured voltages and current through nLDMOS-SCR when stressed with HMM-50 tester, zoom-in on moment of reverse recovery; stress level: 5.6 kV (equivalent)



The 100 V tolerant HV nLDMOS-SCR has failed at 5.6 kV HMM-50 and at 7.5 kV HMM-IEC stresses. Similar to the ESD diode case described above the likely reason of miscorrelation is the negative currents generated by HMM-50 tester (Fig. 2.57) and the corresponding reverse recovery effect.

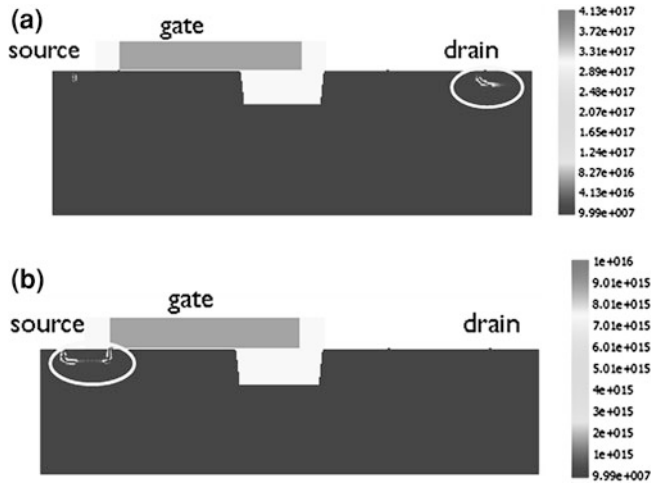


**Fig. 2.58** Simulated cross-section of a nLDMOS-SCR (a) and simulated HMM current and maximum impact ionization rate in the device during 5.6 kV (equivalent) HMM-50 stress (b)

The mixed-mode simulation with the nLDMOS-SCR device cross-section (Fig. 2.58a) in DECIMM<sup>TM</sup> [19] was used to analyze the lower failure level during HMM-50 stress. The simulated HMM current and the impact ionization rate of the nLDMOS-SCR at the failing stress level (Fig. 2.58b) demonstrate the significant increased impact ionization rate at  $t \sim 150$  ns in spite of a full decay of the HMM current. The increased impact ionization rate after the decay indicates reverse recovery in the nLDMOS-SCR device.

The location of the highest impact ionization during HMM stress during forward conduction mode is the drain side of the device (Fig. 2.59a). During reverse recovery, the impact ionization is concentrated mainly at the source side (Fig. 2.59b). The negative external voltage forces the n+-to-p-body junction on the source side of the nLDMOS-SCR into reverse bias thereby building up a strong electrical field. This electrical field stimulates impact ionization along the junction. The impact ionization does not spread uniformly across the junction. Instead there are two hot spots where the impact ionization rate is locally higher (Fig. 2.60). This induces locally a higher carrier and current density.

The impact ionization is also concentrated around the gate oxide of the nLDMOS-SCR. During reverse recovery, some of the free hot carriers move towards the gate. They get trapped when they enter into the gate oxide. With increasing



**Fig. 2.59** Location (*circle*) of impact ionization peaks during HMM-50 stress: **a** after 20 ns (*forward conduction*) and **b** after 150 ns (*reverse recovery*); *stress level 5.6 kV (equivalent)*

HMM stress levels, more carriers are trapped in the gate oxide which results in a degradation of the gate oxide and an increase of the device leakage similar to the hot carrier degradation effect at much longer stress in normal operation conditions.

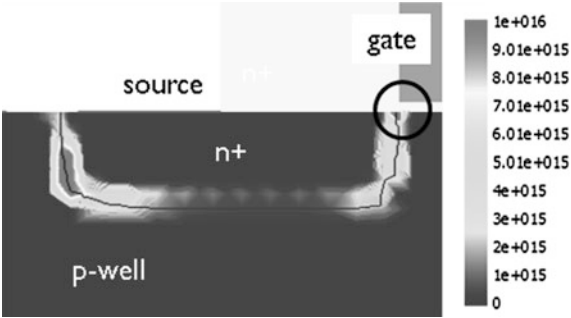
The evolution of the device leakage current during HMM stress on the nLD-MOS-SCR for both the HMM-50 and the HMM-IEC testers is different (Fig. 2.61). On the contrary, an abrupt failure is observed during the HMM-IEC tester stress. This supports the conclusion that different failure modes occur when stressing the HV nLDMOS-SCR with the two different HMM testers. The device fails thermally when using the HMM-IEC tester. Hot carrier stress induced by reverse recovery causes a gate oxide failure during stress with the HMM-50 tester.

### 2.5.2 Impedance Matching and Impact on Failure Level

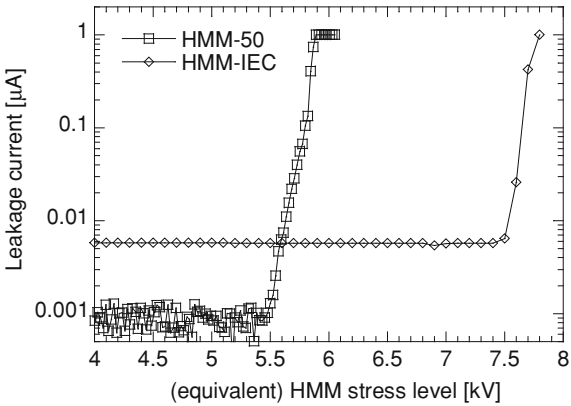
The observed device failures are directly related to the pulse source impedance of the particular HMM-50 tester. The on-state resistance of the tested devices is much lower than  $50\ \Omega$ . This causes mismatching with the source impedance of the HMM tester. If a series  $50\ \Omega$  resistor is added to the HMM setup (Fig. 2.62) the reflections are minimized and failure due to reverse recovery is suppressed.

The repeated HMM-tests with the series  $50\ \Omega$  resistor show different results (Table 2.5). The equivalent failure level when stressing the two devices from group 2 with the HMM-50 tester becomes comparable.

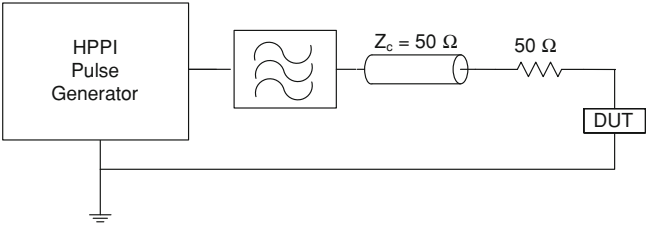
A small negative current is measured when stressing the ESD diode with the  $50\ \Omega$  resistor. This forces the diode into reverse bias and the reverse recovery



**Fig. 2.60** Zoom-in on locations of impact ionization (after 150 ns) in device cross-section, circle: impact ionization hotspot close to gate oxide; *stress level* 5.6 kV (equivalent)



**Fig. 2.61** Device leakage current evolution (at 100 V) of 100 V nLDMOS SCR during HMM testing with HMM-50 tester and HMM-IEC tester

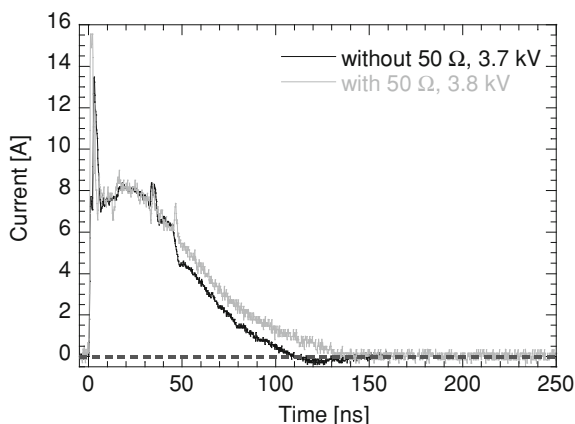


**Fig. 2.62** Modified HMM-50 setup with added  $50 \Omega$  resistor

**Table 2.5** Equivalent failure level of ESD diode and nLDMOS-SCR when stressed with HMM-50 tester: with and without added  $50 \Omega$  series resistor

Device	No resistor	With $50 \Omega$ resistor
ESD diode	3.7 kV	3.8 kV
nLDMOS-SCR	5.6 kV	5.4 kV

**Fig. 2.63** Measured current through ESD diode at failure level when stressed with the HMM-50 tester: with and without 50  $\Omega$  resistor



occurs. Although the amplitude of the negative current is much smaller in comparison to the stress without added resistor the resulting failure level is similar to the case when the resistor is added. This is attributed to a different stress current shape (Fig. 2.63) for the measured HMM current through the ESD diode with and without added series resistor.

This larger forward current charges more the diffusion capacitances of the diode. When the diode goes into reverse recovery, more carriers need to be swept away to get a stable reverse-biased state. The higher amount of free carriers, together with the impact ionization due to reverse recovery creates a similar current density in the diode than without series resistor.

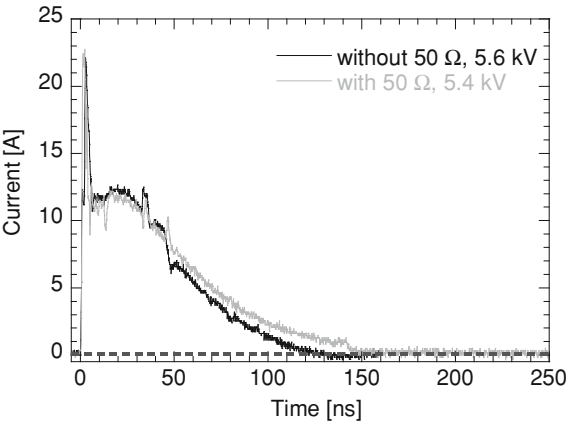
The additional series resistor prevents negative voltages and currents when the nLDMOS-SCR is stressed. Consequently it should prevent reverse recovery in the n<sup>+</sup>-to-p-body junction on the source side of the nLDMOS-SCR. However, small negative voltages and currents are still measured. This indicates that reverse recovery still occurs in the device when stressed with the HMM-50 tester. The measured HMM current through the nLDMOS-SCR with and without added series resistor (Fig. 2.64).

A larger current flows through the device when the resistor is added to the setup. More excess minority carriers are stored in the diffusion capacitances of the device's junctions. Due to the larger amount of minority carriers during forward conduction, a similar number of carriers are trapped in the gate oxide. This results in a similar degradation of the gate oxide in comparison to the case when no resistor is added to the setup (Fig. 2.65).

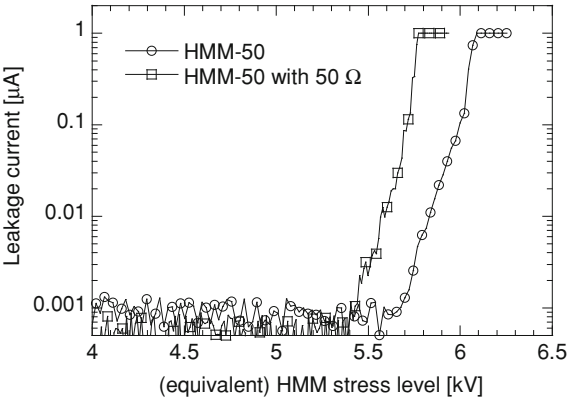
Similar failure level are obtained when stressing the lateral PNP and the ggNMOS with both the HMM-50 and HMM-IEC tester. PNP devices conduct ESD stress with a higher on-resistance. This results in fewer reflections when the stress is applied with the HMM-50 tester. Consequently only a small negative current flows after the decay of the HMM pulse. Furthermore, a PNP device in reverse behaves like in forward operation but with a different I-V curve. It is



**Fig. 2.64** Measured current through nLDMOS-SCR at failure level when stressed with the HMM-50 tester: with and without 50  $\Omega$  resistor; equivalent HMM stress level are given



**Fig. 2.65** Leakage current evolution of 100 V nLDMOS-SCR (at 100 V) during HMM-50 test with and without added 50  $\Omega$  resistor



expected, that the PNP can conduct at least the same ESD stress as during forward conduction.

Thus correlation issues exist for IEC 61000-4-2 type of HMM tester and a 50  $\Omega$  HMM testers. They might need to be address to gain an appropriate confidence in component level test results. In general 50  $\Omega$  HMM test systems should be used taking into account the reverse recovery and negative current generation effects.

## 2.6 Summary

The demand on highly integrated SoC and SoP ICs created a design paradigm shift towards the on-chip system level ESD protection. The significant gap between component and system level test methods and standards has been bridged by the introduction of the HMM method and component level ESD gun test as well as on-

wafer methodologies. These methods provide stress pulses for the component level close to system-level standards pulse waveforms like for example IEC 61000-4-2. As a result, today, not only the final system blocks, but also modules, PCB and IC designs can be evaluated for system level ESD stress.

Both from technical realization perspective and from an overall methodological point of view, the on-chip system level ESD design requires a good understanding of the test standards and procedures, especially for their adaptation to the IC component level and on-wafer verification. The aspects of such understanding include the measurements of the pulse waveforms, transient characteristics, and the correlation factors between different tester types.

The physical aspects of the key test methodologies and their application specific support of on-chip ESD system level design are related to ESD gun testing itself, the test board design, and the tester and ESD pulse correlation factors. The gun system level tests according to the commonly used IEC 61000-4-2 and ISO 10605 standards and their realization in the ESD laboratory environment are described above.

The approach for Human Metal Model (HMM) testing as a major practical component level emulation of the system level ESD stress is based on the understanding of the major standards and test procedures, as well as board and wafer level testing methodologies.

A significant progress has been made in on-chip system level IC development by the implementation of the component and on-wafer testing methods. These methods simulate the system level ESD discharge pulse waveforms at least with some acceptable accuracy for the initial design. In particular, understanding the IEC 61000-4-2 standard requirements led to the development of a component-level test method with the same stress waveform. While the system level IEC and ISO ESD standards for the contact discharge define the tests for the system ports, the HMM methodology, on the contrary, is primarily targeting the evaluation of the IC pins robustness.

A similar approach has been successfully applied for evaluation and comparative analysis of the standalone ESD solutions on test chips. This is done based on the assumption that, if the HMM pulse waveform repeats the system level waveform, then some correlation of the passing level can be expected. The follow-up studies have demonstrated that in many cases the correlation between standard system level gun tests in the corresponding laboratory setup has a direct correlation with the passing level during HMM stress. In spite of a number of reported miscorrelations, today, HMM likely represents the most practical and widely used approach for on-chip ESD design. This will be broadly demonstrated in the examples of the following Chapters.

The primary goal of any ESD design is to meet the required passing level during component and system-level ESD qualification. However, relying only on the passing level would be rather difficult during the development of the ESD solutions and the conduction of ESD case studies. For that the capturing of voltage and current during ESD stress is required. The exact implementation of suitable

measurement setups is not an easy task. Therefore calibration and de-embedding methods for the removal of distortions by tester parasitic have been presented and applied to examples. As an alternative, Kelvin setups are used for ESD on-wafer measurement setups. Both, calibration and the Kelvin setups are required to capture the real transient device and circuit response during ESD stress.

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