

Preface

Subject and Purpose of This Book

Over the last decade a significant paradigm shift in systems and analog IC design was initiated with new market demands and the availability of emerging technologies. The rapid evolution of the handheld and mobile device market segment, dramatic increase of electronic content in automotive products, and the substantial progress in industrial and medical applications created a new need for on-chip protection against system level ESD stresses. The expansion of this trend is not limited to only the ESD specification. Compliance with other, system level electromagnetic compatibility (EMC) standards might also be required. It can include surge protection, EMI compatibility, overvoltage protection (OVP), and even added ability to withstand longer electrical pulses specific to defibrillator equipment or lightning strikes.

This new trend in combination with high level system on chip (SoC) and system in package (SiP) integration, a substantial increase in data rates, electronic system portability, lower power consumption, and lower operation voltages has initiated intensive research and design activities. As a result, an understanding of the need for development of the new test methodologies, adaptation of the system level test standards and procedures toward the IC components, and ESD IP design on test chips has significantly changed the ESD development landscape and the overall research and development investment today. As a result, the engineering of new high current capable ESD on-chip devices and more advanced transient voltage suppressors (TVS) with precise electrical characteristics has emerged.

Essentially, a new on-chip system level protection ESD design culture has been formed. It includes physical design of the high current capable devices taking into account a variety of latchup and transient latchup scenarios, the print circuit board (PCB) and future systems design, and the understanding of the correlation of the characteristics of different devices, stress types, and setups. As an ultimate goal, this activity is now targeting a new system-IC co-design approach. The creation of this *new system level ESD design culture* is getting more and more acknowledged not only by the authors of this book, but by many leading experts in the ESD, IC,

and system design community. So far, however, the overall understanding of the on-chip system level design is greatly dispersed across multiple papers, tutorials, white papers, and IC product application notes.

With its main purpose, this book represents a first attempt to organize, to structure, to simplify, and to bring to the reader the understanding of the major aspects of this system level on-chip ESD design culture. The authors pursue this attempt at the level of the most possible logical and simple way of understanding that requires no specific previous knowledge which makes it compatible for a broad audience.

During the work on this book the authors have made a joint effort to combine and summarize their research and industrial design experience, accumulated in the field, to bring the understanding to the next level. The material of this book is composed to present the on-chip system level ESD design within the scope of five chapters. They are logically focused on the introduction of the system level on chip design principles, presentation of the major test methods, on-chip ESD design solutions taking into account latchup phenomena, and finally on bringing the outline for an IC-system co-design approach.

Although many original research papers are referenced across the book chapters, the overall purpose of this book is not to deliver a review of the most up-to-date publications or standards in the field. Instead, the challenging task, as targeted by the authors, was to find and bring under each aspect or design step a logical emphasis of the basic physical principles behind the solution, design, or methodology. This is done to enable readers to apply the in-depth physical understanding generated by reading of the book material toward the solution of their own specific system and chip ESD design problems. The authors expect that creativity and innovation required for solving future system level ESD design problems will be substantially supported by this book. In particular, the readers will see the advantage of physical design approach supported by a mixed-mode device-circuit simulation methodology that uses parameterized devices, circuits, and processes.

The authors carry on a genuine hope that this book will be found useful not only by dedicated ESD design practitioners, but also by a broad audience of IC and system designers, application and product engineers.

The Book Structure

The book has a five-chapter structure. The first introductory [Chap. 1](#) defines major principles and methodologies for the on-chip ESD design. [Chapter 2](#) focuses on ESD test standards and methods. [Chapter 3](#) describes the device and clamp level solutions for the on-chip system level ESD protection, which is extended in [Chap. 4](#) toward the remaining aspects of the chip design, latchup, and transient-induced latchup. Finally, [Chap. 5](#) leverages the previous chapter's knowledge outlining the new chip-system co-design approach.

The introductory [Chap. 1](#) is an important step to understand the material of the following chapters. The chapter sets the terminology that is used throughout the book. It starts from the basic understanding of an ESD event as a transfer of energy between two connected objects and continues with the description of the on-chip ESD protection strategies as well as the differentiation of on-chip and off-chip ESD protection approaches. A more detailed specification of the understanding for the system level ESD pulses, standards, and test methods is further summarized in [Chap. 2](#). The material in [Chap. 1](#) outlines an understanding that the demand of new age electronics creates a significant design paradigm shift both in on-chip system level design with integrated system level ESD protection devices and off-chip PCB design. New precision Si TVS solutions provide now electrical characteristics for significantly more accurate voltage clamping in comparison to the commonly used polymer or zinc-oxide multilayer varistors under very low capacitive load. A more detailed device level description for Si TVS devices is given in [Chap. 3](#), while the understanding of the on-chip and off-chip co-design aspects with Silicon TVS is discussed in [Chap. 5](#). An important aspect to pass certain system level tests is related not only to power-off, but also to power-on stress conditions. Thus, those pins need to be protected for an order of magnitude higher current level than the standard component specifications Charge Device Model (CDM), Machine Model (MM), and Human Body Model (HBM). [Chapter 1](#) emphasizes that the ESD “solutions” for the system are no longer a simple choice of a suppressor component to be connected at the system port. An effective solution requires the application of a design methodology that takes into account the layout of the circuit board, the electrical characteristics of the suppressor, and the ESD characteristics of the IC itself. The chapter also brings up a number of design aspects that should be taken into account during the challenging design of a functional and reliable product. An elevating complexity of the required design solutions requires innovation and novel approaches.

The last two sections of [Chap. 1](#) introduce two key simulation methodologies to support physical ESD design relying on the ESD compact modeling and the new Technology CAD approach based on the parameterized mixed-mode analysis with the DECIMM tool. The approach enables an automated mixed-mode device-circuit analysis with both parameterized process profiles and device templates.

After the main terminology and the direction of the book is set, [Chap. 2](#) brings the background for the physical aspects of key test methodologies and their applications for the on-chip ESD system level design at each development stage. Focus is made on the understanding of the ESD gun testing on board level, followed by the package and wafer level test methods toward an approach for a more effective on-chip design. This chapter focuses first of all on system level tests like the commonly used IEC 61000-4-2 and ISO 10605 standards. This material is followed by the explanation of the key methodological approach of Human Metal Model (HMM) testing, which is the first component-level emulation of system level ESD stress. For completeness, the chapter covers the understanding of other

practically used test methods for the on-chip design as the transmission line pulse methodology (TLP), ESD waveform capturing and analysis, and the physical bases behind the correlation factors for different pulses, device types, and test conditions. The testing methodologies presented in this chapter are widely applied in the remaining chapters of the book.

On-chip ESD solutions and the process technology aspects are discussed in [Chap. 3](#). The chapter targets a structured and logical understanding of rather cross-disciplinary subjects required for the successful design of pins protected with system level requirements. These topics include principles of ESD device operation in the breakdown state, under injection and conductivity modulation conditions, clamp layout design, process technology options, the safe-operation area (SOA), the self-protection capability of standard devices, and the co-design of the on-chip ESD network and analog internal circuit blocks. Thus, the chapter challenges the structural presentation of the high-level introductory material for device design, the ESD devices, and clamp design principles specific for rather advanced system level on-chip protection. The major challenge, covered here is the high voltage (HV) system level ESD cell design focused on achieving the proper pulsed-type independent width scaling for high current performance, taking advantage from available process technology features. The nonlinear effects impacting the performance of the structure due to current crowding, improperly balanced layout, the multifinger turn-on effect, or an undedicated “sneak” current path formed in a particular cell and product layout are discussed. The chapter is based on a substantial physical experimental verification and validation of the final solutions, TCAD mixed-mode analysis of the ESD devices, clamp circuits, and analog peripheral circuit blocks based on the new approach enabled by the DECIMMTM tool [19, 20]. The chapter concludes by a discussion of the critical topic related to process capability for ESD solution design and confidence of ESD protection window targeting.

In wafer-level packaging (or micro surface mounting devices) design, the flip chip bonding bumps is evenly distributed on the top of the entire active layout area. At a high current from a system level ESD event, the injection from an analog circuit clamp area can disturb the operation of many more connected active devices. A “sneak” latchup current path can form deep inside the layout of the internal circuit components. Therefore, clamp latchup isolation is an important part of the design. These latchup phenomena are summarized in [Chap. 4](#) as a logical continuation of the previous chapter’s material. The key point of [Chap. 4](#) is that the chip-level integration of a validated standalone ESD clamp for system level requirements is not a simple problem. Application specifications and chip functionality need to be thoroughly taken into account to avoid clamp interaction with internal circuit blocks during both system level ESD stress and normal operation. In high injection conditions induced by the system level ESD current, parasitic devices capable of supporting the conductivity modulation regime may also turn on. From this perspective, a system level ESD event in power-on

conditions can conceptually be treated as similar to latchup phenomena. Here, differentiation is done between three major latchup scenarios that represent physically different phenomena. The *conventional CMOS Latch-up* is represented as a high-current turn-on of a parasitic SCR formed by a PMOS-NMOS inverter pair as a result of current injection in the form of two subcases: an I/O buffer with internal injection and a core circuit with injection from a remote injector. The *HV Nepi-to-Nepi Latch-up*, the turn-on of the parasitic n-p-n structure in a high current state, is a result of the current injection in one of the pockets. The understanding of the electron injection from a low-side pocket and the hole injection from a high-side pocket are explained. Finally, the *Transient induced Latch-up* is introduced as a combination of the physical phenomena where the ESD clamp turns on as a result of a short-term voltage overstress. Thus the chapter covers many important industrial design aspects that make a bridge for on-chip integration of validated standalone ESD clamps, taking into account the chip functionality, internal circuit blocks interaction, during both system level ESD stress and normal operation. The latter is demonstrated on the example of a highly integrated smart-power IC with a CAN transceiver.

The final [Chap. 5](#) combines the tools and methodologies of the previous chapters to develop an effective and robust ESD co-design for system level IC pins and systems. The chosen approach combines transient device characterization with test boards and on-wafer setups, and device and circuit simulations. The combination of simulations and on-wafer characterization enables the design and verification of system level ESD protection solutions during an early stage of the IC design and even long before a final system is designed or built. The first section introduces the available off-chip ESD protection devices. This is followed by a study of the available simulation tools for the ESD protection design. Methodologies and examples for the device and circuit modeling are provided. The simulation models are used for two system level ESD design methodologies: datasheet-based design and co-design. The required input for each methodology is discussed together with the advantages and disadvantages of each methodology. Through several case studies, recommendations for the design of ESD protection structures for system level IC pins are provided. The chapter concludes with a comparison, benchmarking, and discussion of the introduced design methodologies. Simulations and transient device characterization are essential for the analysis and development of ESD protection solutions for system level IC pins. ESD device models can be simplified to reduce the modeling effort and the simulation time of large protection networks. Mixed-mode ESD simulations enable higher accuracy or the simulation of devices with a complex behavior during ESD stress. Highly accurate FEM models allow the simulation and extraction of the device behavior in the transient domain. SPICE and compact models can be added to the mixed-mode simulation setup to enable circuit-like simulations. The presented simulation approaches are applied to different case studies to analyze and benchmark system level ESD design concepts. The chapter introduces the *datasheet-based system design* with TVS

on-PCB components as a methodology which is based on designs experience or the request of higher ESD protection level by the IC supplier. The application of the datasheet-based approach leads in many cases either to an overdesign on the system side and/or costly overdesigned ESD protection solution on IC-level. In some applications this approach can create additional challenges to design simultaneously an ESD robust and functional system. As a result many more off-chip components than necessary might be added.

The alternative methodology is an *IC-system co-design* approach which involves obtaining the pulsed device characteristics. TLP testing and TLP I-V curves are used to provide information about the on-chip and off-chip ESD protection to the system designer. The material in this chapter is greatly based on case studies which combine TLP testing results with transient simulations required to identify the transient behavior of the on-chip and off-chip ESD protection devices during system level ESD stress. An important extension of the *IC-system co-design* methodology is achieved by adding extensive HMM characterization data, obtained from the external IC pins to the design flow. The information is used to verify if the residual currents into the on-chip ESD protection do not exceed the standalone HMM failure level. It is concluded that the co-design approach will stay as a challenge for future SiP and SoC due to the continued scaling of CMOS technologies, novel device concepts like 3D transistors (multi-gate-FET, FINFET), as well as new integration principles like 2.5 and 3D integration which are defined with new backend of line structures like through-silicon-vias.

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