

Preface

All-Digital Phase Locked Loops (ADPLLs) have become very common in low cost and feature mobile phones. In recent years, extensive research activity on ADPLLs has focused on increasing the performance of ADPLLs, thus increasing the range of their possible applications. The theoretical noise performance of an ADPLL is limited by the quantization error of the TDC and the DCO. In the literature, noise shaping of the quantization error is one of the main techniques used to reduce the impact of the quantization error of the TDC and the DCO on the noise performance of an ADPLL. In this book, we present a framework to analyse, design, simulate and compare different ADPLL architectures with noise shaping TDCs and DCOs.

In [Chap. 1](#), we summarize the main contributions of the book.

In [Chap. 2](#), we review the operations of the main ADPLL architectures in terms of phase-to-digital conversion.

In [Chap. 3](#), we review the main TDC architectures and relate their operations to quantizers and/or sigma-delta modulators.

In [Chap. 4](#), we derive discrete-time models for the main ADPLL architectures and derive analytical equations for predicting the phase noise performance.

In [Chap. 5](#), we show the advantages of noise shaping and dither by means of an analytical method in the time domain.

In [Chap. 6](#), we focus on simulating ADPLLs as mixed-signal systems. We show that there is a tradeoff between accuracy and simulation time. We describe a simulation method in Simulink that can mitigate this tradeoff.

In [Chap. 7](#), we discuss phase noise in more detail. We describe a procedure to model and extract the phase noise of a signal in Matlab.

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Modeling, Simulation, Analysis and Design

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