Perspectives of UTBB FD SOI MOSFETs for Analog and RF Applications

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Abstract Ultra-thin body and buried oxide (UTBB) fully depleted (FD) silicon-on-insulator (SOI) MOSFETs are widely recognized as a promising candidate for 20 nm technology node and beyond, due to outstanding electrostatic control of short channel effects (SCE). Introduction of a highly-doped layer underneath thin buried oxide (BOX), so called ground-plane (GP), targets suppression of detrimental parasitic substrate coupling and opens multi-threshold voltage (V_{Th}) and dynamic-V_{Th} opportunities within the same process as well as the use of back-gate control schemes [1, 2]. Electrostatics, scalability and variability issues in UTBB MOSFETs as well as their perspectives for low power digital applications are widely discussed in the literature [1–5]. At the same time assessment of UTBB FD SOI for analog and RF applications received less attention. This *chapter* will discuss Figures of Merit (FoM) of UTBB MOSFETs of interest for further analog/RF applications summarizing our original research over the last years [6–15]. Device analog/RF performance is assessed through the key parameters such as the transconductance, g_m, the output conductance, g_d, the intrinsic gain, A_v and the cut-off frequencies, f_T and $f_{\max}$. Particular attention is paid to (1) a wide-frequency band assessment, the only approach that allows fair performance prediction for analog/RF applications; (2) the effect of parasitic elements, whose impact on the device performance increases enormously in deeply downscaled devices, in which they can even dominate device performance. Whenever possible, we will compare FoM achievable in UTBB FD SOI devices with those reported for other advanced devices.

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1 Introduction

Enormous progress of the semiconductor technology during the last decade is mostly driven by the continuous demand for the increase of the operation speed and the integration density of complex digital circuits. In order to be able to continue device scaling down to 20 nm and beyond, both new materials and new device architectures are unavoidably employed. Therefore, nowadays we deal not simply with proportional shrinking of respective device dimensions, but as well as with new architectures and materials in both channel and gate oxide. Both these factors will evidently affect analog/RF device features. From the device architecture point of view, two main contenders clearly appear as able to satisfy ITRS requirements for device downscaling: planar FD SOI with ultra-thin body and ultra-thin BOX (so-called UTBB, or UTBOX, or UT2B or ETSOI) and multiple-gate devices or MuGFET.

Focus of this chapter is UTBB FD SOI MOSFETs, while some benchmarking with other devices is provided whenever possible. Main features which allow UTBB FD SOI withstanding ITRS requirements for 20 nm-node and beyond are the following:

- outstanding electrostatic integrity;
- effective suppression of fringing fields through the BOX (by BOX thinning);
- ease of heat exhaust through the thin BOX and thus attenuated self-heating (SH) is expected;
- possibility of back-gate control schemes implementation.

However, lateral coupling of source and drain through the substrate is enhanced in the case of thin-BOX devices. This calls for realization of highly-doped layer just under the BOX, or so-called Ground Plane (GP), which screens or prevents electric field lines penetration into the substrate and thus coupling through the substrate. Furthermore, GP opens a practical way for multi-V_{Th} and back-gate biasing schemes realization.

Technological aspects, electrostatics, scalability and variability issues in UTBB FD SOI MOSFETs as well as their perspectives for low power digital applications are widely discussed and shown to be excellent [1–5]. However, till now almost no attention has been paid to analog and RF performance of these devices. Similarly, UTBB MOSFET small-signal behavior in a wide frequency range is rarely discussed except in our works issued during last 3 years [6–15].

2 Devices

UTBB FD SOI MOSFETs discussed in this chapter have been processed at CEA-Leti on UNIBOND^{TM} SOI wafers with either 25 or 10 nm-thick BOX. Wafers without GP, with n- and p-type GP are considered. The Si film in the channel region is thinned down to 7–8 nm, depending on the wafer, and left undoped. Elevated source-drain structures are employed to reduce parasitic resistance. The

gate stack is formed by a HfSiON dielectric with the equivalent oxide thickness of ~1.3 nm and a TiN electrode. More process details can be found e.g. in [1, 2].

The studied devices are n-channel MOSFETs with the gate length L ranging from 30 nm to 10 μm and the channel width W from 80 nm to 10 μm. Multi-fingers devices are used and embedded in coplanar waveguide access pads for performing RF characterization.

3 MOSFET's Key Parameters and Methodology Applied

It is worth firstly to list the key device parameters and FoM of interest for analog/RF applications and describe the methodological approach, which allows a fair comparison of different devices under different bias conditions.

Main key-factors of any MOSFET are: cut-off frequencies (f_T and $f_{\max}$) and intrinsic voltage gain (A_{v0}), which itself varies in a frequency range (as will be discussed in Sect. 5):

$$f_T = \frac{g_m}{2 \cdot \pi \cdot C_{gg}}, \tag{1}$$

$$A_{v0} = \frac{g_m}{g_d} = \frac{g_m}{I_d} \cdot V_{EA} \neq const(f) \tag{2}$$

These key factors in turn depend on such device parameters as transconductance (g_m), drive/drain current (I_d), output conductance (g_d), Early voltage ($V_{EA} = I_d/g_d$), g_m/I_d, gate capacitance (C_{gg}), etc. One should not forget as well about parasitic capacitance and resistance elements (as will be discussed below).

If one considers the application circuit level (e.g. amplifier), then it involves gain bandwidth product, GBW, which depends in turn on the same device parameters (g_m/I_d and I_d):

$$GBW = \frac{g_m}{2 \cdot \pi \cdot C_L} = \frac{g_m}{I_d} \cdot \frac{I_d}{2 \cdot \pi \cdot C_L}, \tag{3}$$

where C_L is load capacitance.

From methodological point of view, a very useful approach for analog performance assessment of different devices is calculating g_m/I_d as a function of normalized drain current [16, 17]. Firstly, because such plot gives a complete picture of studied device, which is valid for different applications: from base-band applications, where high gain, high precision is needed, to high frequency application where high drive current is requested (Fig. 1). Secondly, as g_m/I_d is inversely proportional to the subthreshold swing, S in weak inversion regime and proportional to $\mu \cdot C_{ox}/n$ (where μ is mobility, C_{ox} is oxide capacitance and n is body factor) in strong inversion, such plot is independent of threshold voltage, V_{Th}, of substrate/back gate (or body) bias, V_{bg} and to the first order is also independent of

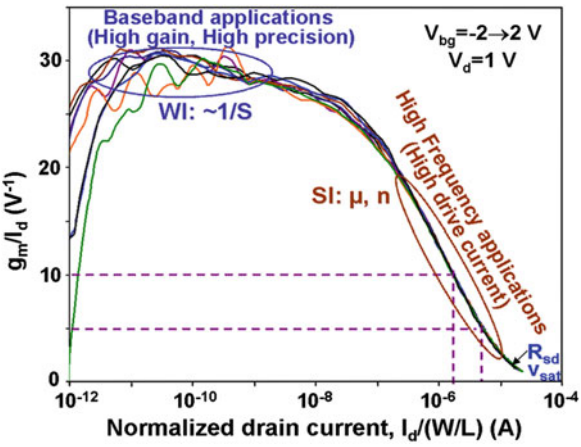

Fig. 1 g_m/I_d versus $I_d/(W/L)$ *curves* for 28 nm-long UTBB FD SOI nMOSFET measured at different V_{bg} from −2 to 2 V. $V_d = 1$ V. *Dashed lines* are drawn to represent $I_d/(W/L)$ extraction approach at a fixed $g_m/I_d = 10$ or 5 V^{-1}

L. In practice, one may fix g_m/I_d value and extract corresponding $I_d/(W/L)$ values as shown in Fig. 1. This allows assessment of device performance purely related to physical parameters as μ or body factor, thus providing a fair comparison of devices issued from different technologies, featuring different dimensions and operated at different conditions.

Figure 2 presents the complete small-signal equivalent circuit of a MOSFET. It is important to clearly distinguish between intrinsic elements, i.e. related to the device itself and extrinsic (or parasitic) elements, as access resistances, fringing and overlap capacitances. Parasitic capacitive components (for instance, capacitive coupling between source and drain through the BOX and substrate, fringing gate-to-source and gate-to-drain coupling, etc.) attain particular importance at high/RF frequencies.

With device length scaling down, importance of parasitic components increases enormously. Parasitic elements can even dominate the device performance (as will be shown in Sect. 6). Thus, ability of separate extraction of "intrinsic" and "extrinsic" elements in advanced nowadays technologies becomes crucial. Firstly, this allows for predicting "intrinsically" achievable idealistic or target values one can reach with optimization of parasitics. Secondly, for the process/configuration optimization, it is important to know wherefrom the problem comes (either intrinsic or extrinsic part). Indeed, if extrinsic part limits device performance, any innovations introduced to boost intrinsic performance (e.g. strain, orientation, etc.) will give negligible improvement to the final device performance.

Considering equivalent circuit shown in Fig. 2, MOSFET expressions for cut-off frequencies (Eq. 1) become more complex, accounting for parasitic elements and clearly reflecting SCE (through C_{gs}/C_{gd} ratio):

$$f_T \approx \frac{g_m}{2 \cdot \pi \cdot C_{gs}} \cdot \frac{1}{\left(1 + \frac{C_{gd}}{C_{gs}}\right) + (R_s + R_d) \cdot \left(\frac{C_{gd}}{C_{gs}} \cdot (g_m + g_d) + g_d\right)} \tag{4a}$$

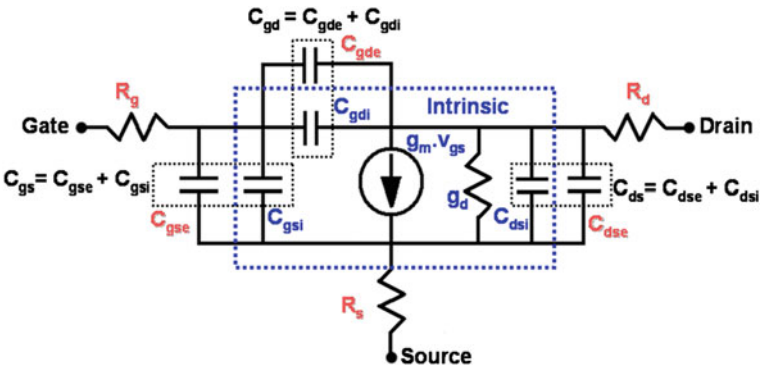

Fig. 2 MOSFET complete small-signal equivalent circuit, including both intrinsic (denoted 'i') and extrinsic (denoted 'e') elements

$$f_{\max} \approx \frac{g_m}{4 \cdot \pi \cdot C_{gs}} \cdot \frac{1}{\left(1 + \frac{C_{gd}}{C_{gs}}\right)\sqrt{g_d\left(R_g + R_s\right) + \frac{1}{2} \cdot \frac{C_{gd}}{C_{gs}}\left(R_s \cdot g_m + \frac{C_{gd}}{C_{gs}}\right)}} \tag{4b}$$

With length shrinkage, C_{gd}/C_{gs} ratio increases indicating the lost of a gate control over the channel and dominance of control from the drain (increase of capacitive coupling between gate and drain). Comparing Eqs. 4a, 4b and 1 one can see that this effect can strongly degrade 'intrinsic' cut-off frequency. Next to that, f_T and $f_{\max}$ are degraded by the parasitic access resistances, R_s and R_d. Gate resistance, R_g, however, affects only $f_{\max}$ (see Eq. 4b). According to Eq. 1, as g_m is inversely proportional to L and proportional to W, while C_{gg} is proportional to the area, f_T is expected to increase with L and be independent of W. However, this does not hold in experiments due to strong parasitic effects (as will be shown in Sect. 6).

Extraction of a complete equivalent circuit demands S-parameter measurements in a wide frequency range. Therefore, adequate structures with RF access pads must be included in the layout from a very beginning of the technology development. Details on the extraction procedure can be found for instance in [18].

4 UTBB FD SOI MOSFET Analog FoM

4.1 Benchmarking with Other MOSFETs

Extended benchmarking of analog FoM of UTBB FD SOI MOSFETs with respect to other both planar FD SOI MOSFETs and multiple-gate SOI-based FinFETs was performed in [6]. Table 1 summarizes analog FoM achievable in UTBB FD SOI with different geometries and compares them with SOI FinFET ones. One can see that UTBB FD SOI devices feature rather high values of I_d, V_{EA}, A_{v0}, $g_{m\_\max}$, which are comparable and in certain cases can be even higher than in another

Table 1 Main analog FoM for different devices

	$g_{m\ \max}$, (μS/μm)	$I_d/(W/L)$ g_m/I_d = 10 V^{-1} (μA)	$I_d/(W/L)$ g_m/I_d = 5 V^{-1} (μA)	V_{EA} $V_g \sim V_{Th}$ (V)	V_{EA} $V_g \sim 1$ V (V)	A_{v0_max} (dB)
L = 30 nm						
FinFET	1,050	1.2	5.1	1.2	5.1	33.5
strained FinFET	1,410	1.3	6.4	1.5	6	34
UTBB FD SOI W = 10 μm	1,015	1.74	5.4	3.4	11	36
UTBB FD SOI W = 80 nm	1,510	2.3	7.2	5.5	10	38
strained UTBB FD SOI W = 10 μm	1,375		8			
L = 100 nm						
FinFET	700	3.1	10.8	4	12	40
strained FinFET	1,050	4.7	16.6	5	18	43
UTBB FD SOI W = 10 μm	810	4	13	8	20	46
UTBB FD SOI W = 80 nm	1,220	6	20	15	20	51
strained UTBB FD SOI W = 10 μm	985	5.6	17	5.5	16	40.5

$V_d = 1$ V. $V_{sub} = 0$ V

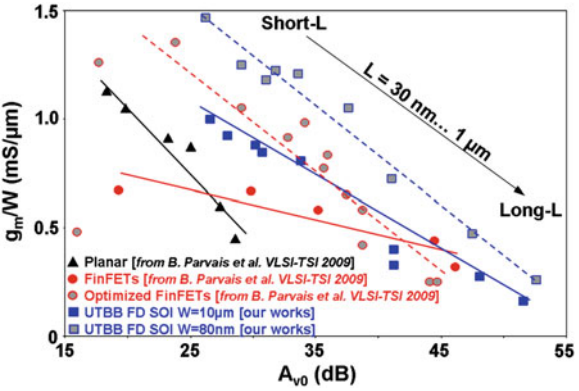

Fig. 3 g_m/W as a function of A_{v0} for different devices and processes. V_d is in saturation (1 V in our works and 1.1 V in [19]). $V_g = V_{Th} + 0.6$ V, $V_{bg} = 0$ V. $L = 30$ nm–1 µm for UTBB FD SOI MOSFETs. $L = 45$ nm–1 µm for FinFETs. Lines are intended to guide eyes

advanced architecture as FinFET. This becomes more visible in g_m/W versus A_{vo} metric plotted in Fig. 3 for various device architectures with different gate lengths. It reveals that UTBB FD SOI MOSFETs clearly outperform planar MOSFETs and non-optimized FinFETs. UTBB FD SOI MOSFETs are also very close and can even outperform optimized FinFETs particularly if narrow channel devices (offered simultaneously higher g_m/W and higher A_{vo}) are used.

It would be important to point out that UTBB FD SOI MOSFETs maintain their excellent performance in a wide temperature range, with very limited degradation of main parameters [6]. For instance, only 5 dB reduction of A_{v0} was observed over 200 °C. This makes UTBB FD SOI MOSFETs particularly attractive for high-precision analog circuits. Furthermore, A_{vo} was demonstrated [6] to be maximized in the moderate inversion regime (at $\sim V_{Th}$), which is beneficial for low-power applications.

4.2 Effect of GP and Back Gate Bias

A unique feature of UTBB FD SOI architecture is related to the possibility of back-gate biasing. In order to implement this back-gate biasing scheme, a highly-doped region, or ground plane, should be formed just below the BOX. Realization of GP region requires heavy implantation through the Si film and hence one can think about possible μ degradation. Next to that, GP suppresses substrate depletion, which means that there is no "BOX thickening" (provided by substrate depletion region) and hence body factor might be higher comparing to the no-GP case. Therefore, the question is "how these two facts affect Analog FoM?" Answering this question, [3, 8] demonstrate that g_{m_max} and I_d values stay almost unaffected. In the same time [8] reveals the sensitivity of the intrinsic gain to GP realization and hence a special

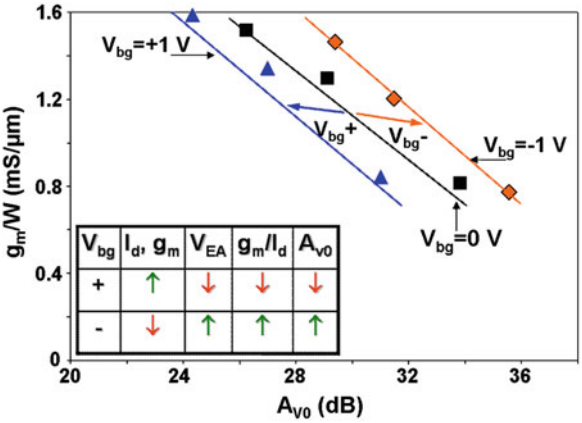

Fig. 4 g_m/W as a function of A_{v0} for different V_{bg}. $V_d = 1$ V. $V_g = V_{Th} + 0.6$ V. $L = 30$–100 nm. Lines are intended to guide eyes. Inset-table summarizes effect of back-gate bias polarity on main analog FoM

care has to be taken in order to assure high doping level just under the BOX. If the GP implantation is not well adjusted some reduction of intrinsic gain may appear (due to *DIBL* and related V_{EA} degradation) [8].

Effect of back-gate biasing on electrostatic and digital figures have been widely studied [3–5]. In this section we discuss how back-gate bias application affects analog FoM. From one side, negative back-gate bias results in V_{Th} increase and hence on-current I_{on} reduction, but in the same time it provides S and *DIBL* decrease (i.e. improvement). From another side, application of positive V_{bg} pushes channel centroid [5] to the bottom Si/BOX interface and hence higher g_m and I_{on} (due to higher μ values [20]) might be expected. These two trends give a clear trade-off for analog FoM. [6] demonstrates that 5–10 % enhancement of I_d and g_m may be achieved by application of positive V_{bg} and that 5–10 dB higher A_{vo} is reached in the case of negative V_{bg}. Thus, trends in I_d and A_{v0} dependence on the back-gate bias are opposite and hence the choice of "positive" or "negative" bias application for performance boosting finally depends on the target application (either high I_d or A_{v0}) (Fig. 4).

Another way to boost the device performance available in UTBB devices with GP is realization of so-called asymmetric double-gate (ADG) regime, i.e. gate to GP connection $V_g = V_{bg}$ (inset in Fig. 5), similar to DTMOS regime in PDSOI devices. [2, 8] reveals that such regime does not only allow improved SCE control, but also ~20 % performance enhancement in terms of I_d and g_m (Fig. 5). This evidently results into improved g_m versus A_{vo} metric; more details can be found in [8].

Even further performance boost can be expected in the case of so-called quasi-double gate (QDG) realization, i.e. simultaneous sweep of top and back gates with a certain coefficient k ($k > 1$) $V_g = k*V_{bg}$ [12, 14]. Possibility of V_{Th} modulation together with improved SCE control accompanied by improved I_{on} and constant I_{off} achieved in QDG mode can be exploited for digital applications. Higher g_m and

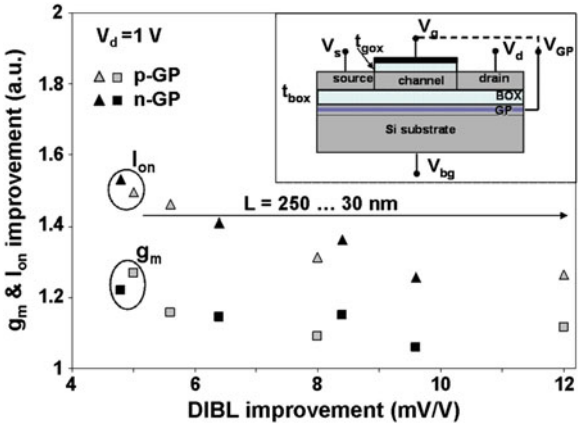

Fig. 5 g_m and I_{on} improvement in ADG mode comparing to a standard single-gate (SG) mode (calculated as g_{m_ADG}/g_{m_SG} and I_{on_ADG}/I_{on_SG}) as a function of DIBL improvement in ADG mode ($=DIBL_{SG} - DIBL_{ADG}$). Insert schematically shows ADG regime. g_m is taken at $V_g = V_{Th} + 0.6$ V and $V_d = 1$ V. I_{on} is taken at $V_g = V_d = 1$ V. $L = 30$–250 nm. BOX thickness, $T_{BOX} = 10$ nm

I_d combined with a lower DIBL (and hence higher A_{v0}) (Fig. 6) can potentially be exploited for analog applications. Thinner BOX evidently appears more promising for QDG realization [14], allowing lower k values for the same performance boost level (Fig. 6). More details on advantages of QDG mode and its exploitation for boosting the sleep transistor performances in the practical use case of a power-gated processor can be found in [13, 14].

5 Wide Frequency Band Assessment

This section points out an importance of the wide-frequency band assessment. Indeed, above-discussion was built on DC results but cited figures of merit vary over frequency. Figure 7 quasi-schematically shows simulated g_d variation as a function of frequency in FD SOI MOSFET. Increase of output conductance with frequency results in turn into decrease/degradation of intrinsic gain. This graph points out that solely DC and/or RF based extractions are not sufficient to reproduce and predict device behavior at different frequencies. Usual DC-based extractions give overestimated performance, whereas purely RF-based one, done in GHz range, underestimates device performance in MHz region. Only wide frequency band measurements allow a complete picture and thus fair analysis and comparison of different devices.

Different effects contribute to g_d variation with frequency.

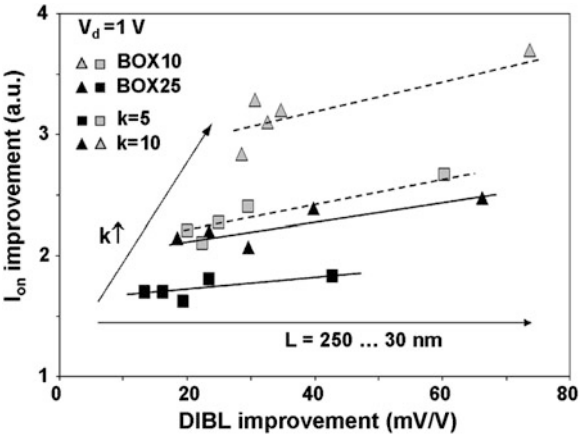

Fig. 6 I_{on} improvement in ADG mode comparing to a SG mode (calculated as I_{on_QDG}/I_{on_SG}) as a function of DIBL improvement in ADG mode (=$DIBL_{SG} - DIBL_{QDG}$). BOX thicknesses of 10 and 25 nm are considered. I_{on} is taken at $V_g \cong V_{Th}$. $V_d = 1$ V. $L = 30$–250 nm

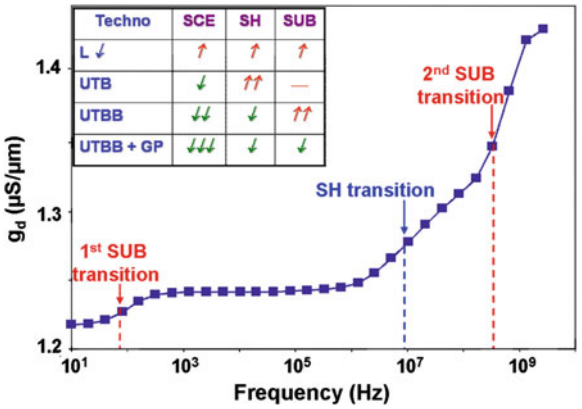

Fig. 7 Simulated g_d variation with frequency in FD SOI nMOSFET. *Dashed lines* schematically indicate transitions related to self-heating (SH) and substrate (SUB) effects. Inset-table summarizes evolution of these effects with technology advances

$$g_d(f) = g_{d\_in} + \Delta g_{d\_FB}(f) + \Delta g_{d\_SH}(f) + \Delta g_{d\_SUB}(f) \tag{5}$$

The frequency independent intrinsic term g_{d_in} is related to channel length modulation and DIBL. The second term, Δg_{d_FB} related to the floating body effect can be for the first order neglected in thin-film FD SOI MOSFETs under standard operation conditions. Two main reasons for g_d variation with frequency in advanced FD SOI devices are related to self-heating, Δg_{d_SH} and source-to-drain coupling through the substrate, Δg_{d_SUB}. Self-heating effect and its increased

importance in SOI-based devices are widely known [21, 22]. Less known, substrate-related frequency dependent effect [23, 24] appears as a result of a substrate capacitance, C_{sub} variation with frequency resulting in the variation of the potential at the SUB-BOX interface, which then through g_m is translated into g_d variation [23]:

$$\Delta g_{d\_SUB} = (n-1) \cdot g_m \cdot \frac{\upsilon_{BGS}}{\upsilon_{DS}}, \tag{6a}$$

$$\upsilon_{BGS} \cong \frac{C_{BGD}}{C_{BGD} + C_{SBG} + C_{GBG} + C_{sub}} \cdot \upsilon_{DS} \tag{6b}$$

Frequency dependence of C_{sub} can be represented in a first order by two RC networks related to majority and minority carriers response [23, 24]. With frequency increase, first minority (in tens-hundreds Hz range) and then majority carriers (in a 100 MHz range) become unable to follow AC excitation so that C_{sub} decreases. Thus, two substrate-related transitions appear in g_d versus frequency curve.

Inset-Table in Fig. 7 schematically summarizes how the main effects which degrade output conductance evolve with technology advances.

Technology progress is mostly motivated by the need of SCE control and thus, first UTB, then UTBB and finally UTBB with GP were introduced.

Considering SH behavior with device downsizing and related technology advances, one can expect that

1. With *channel length reduction* phonon boundary scattering increases, thermal capacitance decreases, density of the current passing through the device increases and moreover SOI-like structures, known to suffer from enhanced self-heating start to be widely employed. All these facts contribute to the self-heating enhancement.
2. With *thinning of the Si film* (i.e. UTB devices) interface proximity enhances interface scattering resulting in thermal conductivity reduction [25] and hence thermal resistance R_{th} increase confirmed by simulations (see e.g. [26, 27]). Thus, self-heating is expected to increase with Si film thinning.
3. With *BOX thinning* one expects reduction of self-heating due to thinner thermal barrier and therefore easier heat exhaust from the channel. This assumption was also confirmed by simulations [26, 27].
4. Finally, GP introduction is not expected, in a first order, to modify SH.

Considering evolution of substrate-related effect with device downsizing and related technology advances, one can expect that

1. With *channel length shortening* source and drain become closer to each other thus naturally enhancing coupling through the substrate. Therefore, substrate-related degradation is expected to increase [28, 29].
2. There is almost no effect of *Si film thinning* on the substrate-related effect in a first order.

3. With *BOX thinning* electric field lines penetrate stronger in the substrate. Thus, coupling through the substrate is naturally expected to be enhanced. 2D simulations performed in [28, 29], indeed, confirm this hypothesis.
4. Finally, as GP acts as screen layer preventing substrate depletion and electric lines penetration, thus, coupling through the substrate and related g_d variation with frequency are expected to strongly reduced.

Figure 8 gives an example of experimental g_d variation with frequency in 30 nm long UTBB FD SOI device without GP under different bias conditions.

Firstly, one can see that both SH- and substrate-related transitions clearly appear in g_d frequency response. Secondly, it would be important to point out that g_d variation over the frequency range is very strong: low-frequency values are about three times lower than those at high frequency. Thirdly, such curves allow extracting temperature rise in the device [22]:

$$\Delta T = R_{th} \cdot I_d \cdot V_d, \text{ where } R_{th} = \frac{\Delta g_{d\_SH}}{(I_d + g_{LF} \cdot V_d) \cdot dI_d/dT_a} \tag{7}$$

Makovejev et al. [7] reveals that despite the use of ultra-thin BOX, device temperature in UTBB MOSFETs can reach about 100 °C at high V_g and V_d. The temperature rise results in 5–7 % I_d degradation [11]. However, the main problem caused by SH in advanced UTBB devices is g_d degradation which is an important issue for analog applications. Finally, it is important to emphasize that in UTBB devices without GP, substrate-related degradation exceeds SH-related one. This gives an additional motivation for GP introduction.

Makovejev et al. [10], indeed, demonstrates that p-GP implementation allows efficient reduction of substrate-related g_d transition (Fig. 9) thanks to suppression of source-to-drain coupling through the substrate. This in turn results in significantly smaller A_{v0} reduction at high frequencies (Fig. 9) [10].

Nowadays UTBB FD SOI devices employ BOX with thickness of either 25 or 10 nm. Makovejev et al. [11] compares them in terms of SH and its effect on the Analog FoM degradation. It reveals that while temperature rise is indeed stronger in devices with 25 nm-thick BOX (see inset table in Fig. 10), there is almost no difference in g_d and I_d degradation caused by device heating in 10 and 25 nm-thick BOX devices at fixed bias conditions (Fig. 10) [11]. This suggests that thicker BOX might be used to reduce e.g. coupling through the substrate, without having much impact on the I_d and g_d degradation caused by thermal effects.

Finally, comparing A_{v0} reduction at high frequencies in FinFETs and UTBB MOSFETs with GP (Fig. 11), one can conclude that A_{v0} reduction level is very similar ($\sim$12–15 %) for these two main approaches for deeply downscaled MOSFET realization. While both SH and substrate-related effects are present in both types of devices, SH appears as a main source of A_{v0} variation ($\sim$10 %). Therefore, further developments should be focused on the optimization of device configuration/materials to ease the heat evacuation.

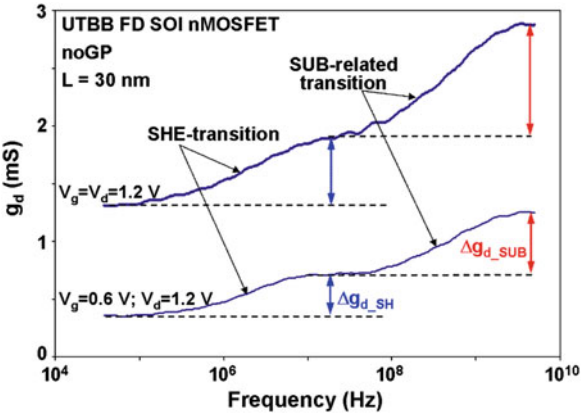

Fig. 8 The experimental g_d frequency response at $V_g = 0.6$ and 1.2 V, $V_d = 1.2$ V in the UTBB FD SOI MOSFET without GP. $L = 30$ nm. $W_{tot} = W \times N_f = 0.25 \times 80$ μm. $T_{BOX} = 10$ nm

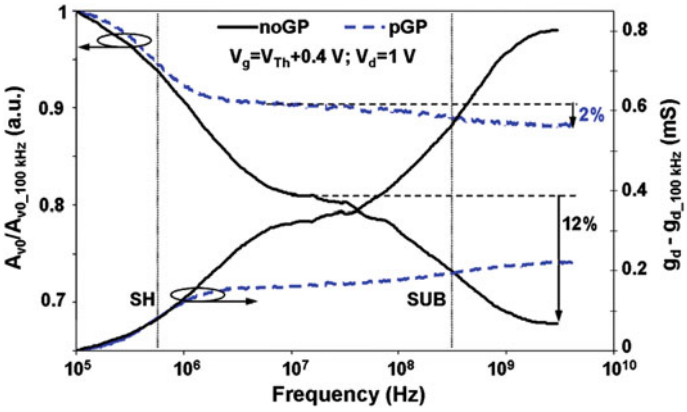

Fig. 9 g_d and A_{v0} variations with frequency with respect to their values at 100 kHz at $V_g = V_{Th} + 0.4$ V, $V_d = 1$ V in the devices with (*dashed lines*) and without GP (*solid lines*). $L = 100$ nm. $W_{tot} = W \times N_f = 1 \times 30$ μm. $T_{BOX} = 10$ nm

6 UTBB FD SOI MOSFETS RF FOM

6.1 Length and Width Dependence

This section discusses the evolution of UTBB FD SOI MOSFET RF FoM with L and W shrinking down. Thanks to the outstanding SCE control in UTBB FD SOI MOSFETs g_m/g_d and C_{gs}/C_{gd} ratios (see Eq. 4a, 4b for their effect on $f_T, f_{\max}$) stay higher than in other technologies [9] thus allowing relatively high $f_T, f_{\max}$ (particularly for the process/devices which were not optimized for RF applications) (Fig. 12).

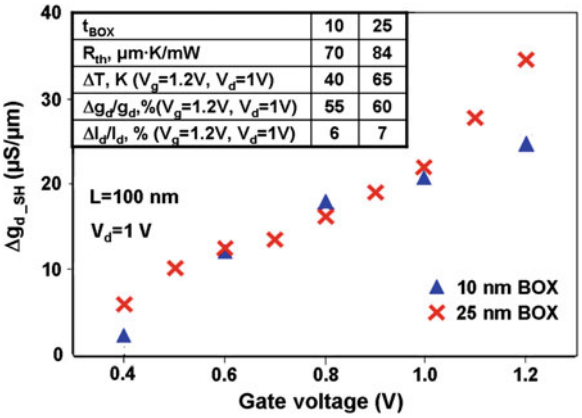

Fig. 10 Amplitude of SH-related g_d transition as a function of V_g for UTBB FD SOI MOSFETs with BOX thickness of 10 nm (*triangles*) and 25 nm (*crosses*). $L = 100$ nm. Inset table gives respective thermal resistance, temperature rise and SH-related analog FoM degradation taken at $V_g = 1.2$ V, $V_d = 1$ V

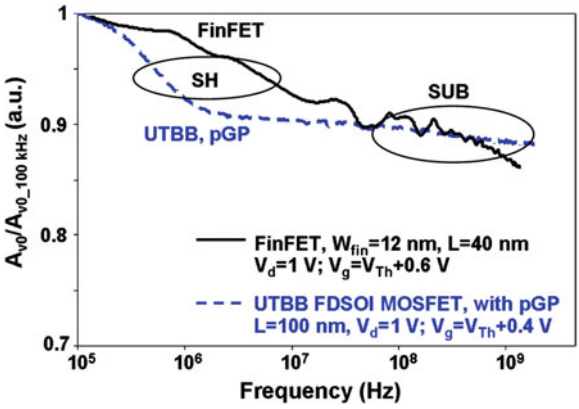

Fig. 11 Variation of the intrinsic gain with frequency with respect to its value at 100 kHz in FinFET (*solid line*) and UTBB FD SOI MOSFET (*dashed line*) with pGP

As was discussed above, 'intrinsic' cut-off frequencies are expected to increase with L scaling down and be independent of W provided that effect of parasitic elements is not strong. [9] studies L and W dependences of cut-off frequencies and different parasitic elements. It reveals that while f_T increases with length shrinking (Fig. 12), this increase is smaller then one could expect from Eq. 1. Analysis of C_{gg} and g_m dependence on L allows for concluding that f_T dependence is dominated by C_{gg} reduction (which is nevertheless lower than expected), while g_m stays almost constant. Another interesting observation to be pointed out is that, contrarily to general expectations and results for previous technology generations, in advanced devices f_T may become higher than f_{max} as a result of strong R_g effect.

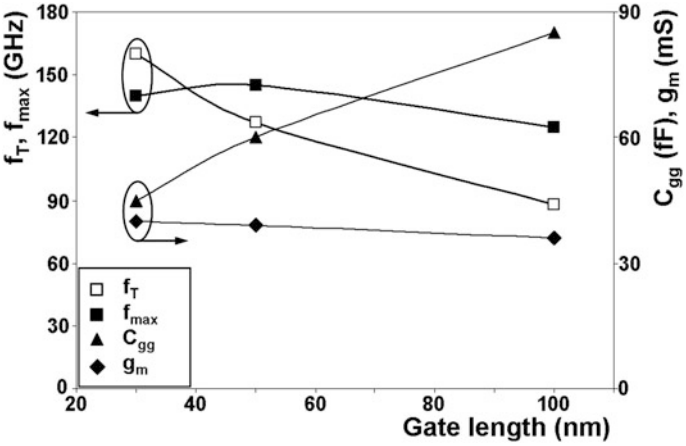

Fig. 12 f_T, $f_{\max}$, C_{gg} and g_m as a function of gate length in UTBB FD SOI nMOSFET without GP. $T_{BOX} = 10$ nm. $W_{tot} = W \times N_f = 0.5 \times 80$ µm. C_{gg} is the total gate capacitance ($C_{gg} = C_{gs} + C_{gd}$)

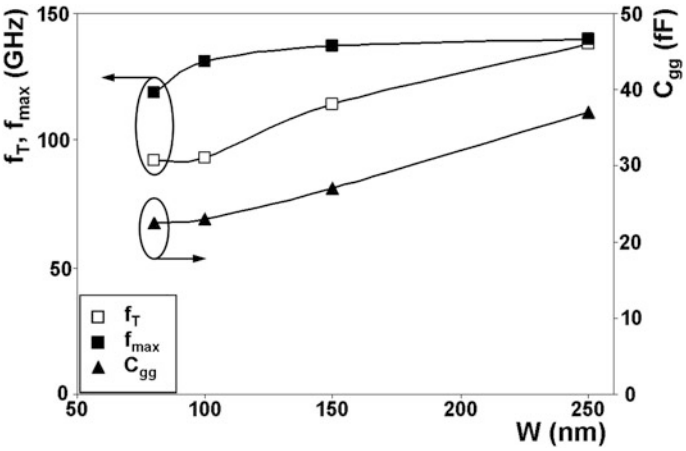

Fig. 13 f_T, $f_{\max}$ and C_{gg} as a function of gate width in UTBB FD SOI nMOSFET without GP. $L = 30$ nm. $T_{BOX} = 10$ nm. $N_f = 120$

Furthermore, [9] demonstrates that expected W independence of f_T and $f_{\max}$ is not maintained in UTBB FD SOI MOSFETs. Indeed, both f_T and $f_{\max}$ degrade with W reduction. It is important noting that this trend is opposite to the one obtained from DC measurements (see e.g. Figs. 3 and 13) thus indicating the role of parasitic elements which degrade RF performance. Effect of parasitic elements is indeed confirmed by the equivalent circuit extraction performed in [9, 15]. W reduction was

demonstrated to result in sub-linear C_{gg} decrease (whereas g_m scales down almost linearly) suggesting strong fringing field effect at the perimeter.

Next section details effect of parasitic elements and distinguishes between 'extrinsic' and 'intrinsic' values.

6.2 Harmful Effect of Parasitic Elements on FoM

Md Arshad et al. [15] decomposes total (or as measured)C_{gg} in 'intrinsic' C_{gg_intr} (i.e. related to 'useful' device) and 'extrinsic' C_{gg_extr} (i.e. related to parasitics) parts (Fig. 14), $C_{gg} = C_{gg\_intr} + C_{gg\_extr}$. It is interesting to note that 'extrinsic' part is smaller that 'intrinsic' one in 100 nm-long devices, but it dominates in the case of 50 and 30 nm long ones. In fact, C_{gg_extr} stays almost constant independently of the device length. As a result total measured C_{gg} does not scale proportionally to L.

Next to that, [15] clarifies effect of R_{sd} on g_m extracting both 'as measured' and 'intrinsic'/ideally achievable (i.e. free from R_{sd}) g_m values. With L reduction impact of R_{sd} increases and while intrinsic g_m continues to growth, 'as measured' one stays almost invariable (Fig. 14).

Finally both these above-described effects affect cut-off frequency. [15] distinguishes 'as measured' f_T and 'intrinsic' one when first R_{sd} and then both C_{gg_extr} and R_{sd} effects are withdrawn. 'As measured' f_T is seen to be strongly degraded comparing to the intrinsically achievable one, particularly in the shortest device (Fig. 15). One can see that while 'intrinsic' f_T (with R_{sd} and C_{gg_extr} withdrawn) continues to grow strongly with L reduction, 'as measured' f_T slows down. It is worth to point out again that the process was not optimized for RF applications and specific approaches used for reduction of extrinsic C_{gg} and R_{sd} lowering were not employed. From another side 'intrinsic' f_T with R_{sd} and C_{gg_extr} withdrawn is evidently overestimated comparing to the really achievable one as parasitic elements are unavoidably present in real devices. Therefore, [15] goes further and calculates f_T which one could achieve in the case R_{sd} and C_{gg_extr} requirements imposed by ITRS are respected. It demonstrates that in this case f_T values of 310 GHz are achievable in 30 nm-long device, i.e. as high as requested by ITRS for LP applications.

Therefore, future work should be focused on the optimization (i.e. minimization) of the parasitics. There are indeed some works devoted to the optimization of parasitic elements. For example, "faceted Source/Drain" was demonstrated to be of interest for the fringing capacitance reduction [30, 31]. Thicker and/or low-k capping layer, thicker gate, etc. are also discussed as a potential solution for C_{gg_extr} reduction [32, 33]. Different silicides, both conventional ones (as NiSi, CoSi, etc.) and emerging ones (e.g. platinum, erbium or ytterbium) are studied as potential materials allowing for R_{sd} reduction [34–36]. Furthermore, different possibilities of performance improvement by geometry and overlap/underlap optimization are considered [37, 38]. However, this is a subject of separate discussion which is out of scope of this chapter. More detailed information can be found e.g. in [15].

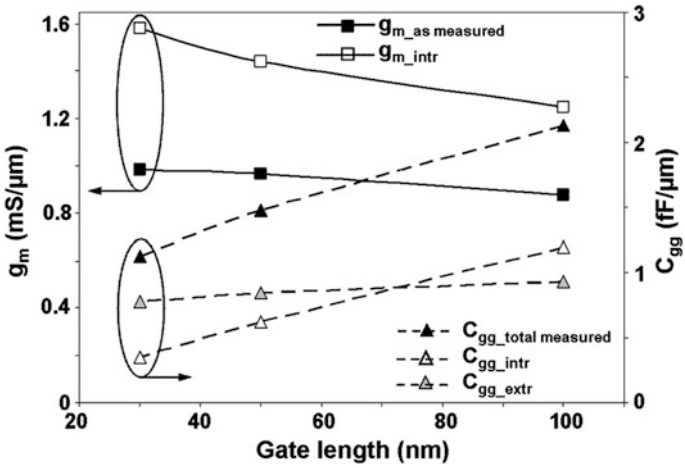

Fig. 14 Measured and intrinsic g_m ($g_{m\_as\ measured}$ and g_{m_intr}) (*squares*) as well as total measured, extrinsic and intrinsic C_{gg} ($C_{gg\_total\ measured}$, C_{gg_intr}, C_{gg_extr}, respectively) (*triangles*) as a function of gate length for UTBB FD SOI nMOSFET, without GP. $T_{BOX} = 10$ nm. $W_{tot} = W \times N_f = 0.5 \times 80$ µm

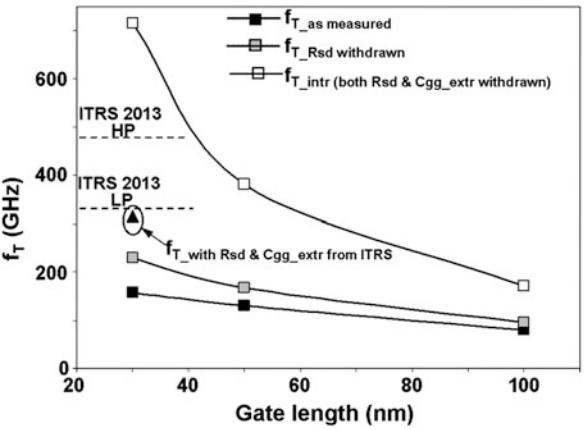

Fig. 15 Measured f_T, f_T with R_{sd} withdrawn and intrinsic f_T with both R_{sd} and C_{gg_extr} withdrawn as a function of gate length for UTBB FD SOI MOSFETs without GP. *Triangle* gives f_T estimation in the case of R_{sd} and C_{gg_extr} values from ITRS. $T_{BOX} = 10$ nm. $W_{tot} = W \times N_f = 0.5 \times 80$ µm. ITRS requirements based on 27 nm technology node FD-SOI targeted high performance (HP, $L = 22$ nm) and low power (LP, $L = 24$ nm) applications are indicated by *dashed lines*

7 Conclusions

There are two main conclusions which one should keep from this chapter:

1. First conclusion concerns *UTBB FD SOI MOSFET performance*. This device architecture features promising performance for analog/RF applications, which is comparable or even outperform other technologies, particularly in the cases when combination of high frequency with LOP/LSTP feature is needed. Furthermore, UTBB FD SOI MOSFETs possess potential for further performance improvement through the optimization of parasitics. This suggests UTBB FD SOI as a good contender for mobile/wireless applications with LOP/LSTP options.
2. Second conclusion concerns *importance of wide frequency band characterization*. We have shown that performance prediction based on DC data exclusively may be inaccurate and device benchmarking may appear even misleading. Next to that, impact of parasitics on device performance enormously increases with L downscaling and hence separation of "intrinsic" and "extrinsic" elements and related performances becomes mandatory in nowadays advanced devices. These two points call for the wide frequency band analysis for a fair FoM assessment. Therefore, adequate structures with RF access pads should be included in the layout from the very beginning of the technology development.

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References

1. Fenouillet-Beranger, C., et al.: Efficient multi-VT FD SOI technology with UTBOX for low power circuit design. In: Proceedings of the IEEE Symposium on VLSI Technology, pp. 65–66 (2010)
2. Andrieu, F., et al.: Low leakage and low variability ultra-thin body and buried oxide (UT2B) SOI technology for 20 nm low power CMOS and beyond. In: Proceedings of the IEEE Symposium on VLSI technology, pp. 57–58 (2010)
3. Fenouillet-Beranger, C., et al.: Impact of a 10 nm ultra-thin BOX (UTBOX) and ground plane on FD SOI devices for 32 nm node and below. Solid-State Electron. **54**(9), 849–854 (2010)
4. Monfray, S., et al.: Thin-film devices for low power applications. Solid-State Electron. **54**(2), 90–96 (2010)
5. Burignat, S., et al.: Substrate impact on threshold voltage and subthreshold slope of sub-32 nm ultra thin SOI MOSFETs with thin buried oxide and undoped channel. Solid-State Electron. **54**(2), 213–219 (2010)

6. Kilchytska, V., et al.: Ultra-thin body and thin-BOX SOI CMOS technology analog figures of merit. Solid State Electron. **70**, 50–58 (2012)
7. Makovejev, S., et al.: Impact of self-heating and substrate effects on small-signal output conductance in UTBB SOI MOSFETs. Solid-State Electron. **71**, 93–100 (2012)
8. Md Arshad, M.K., et al.: UTBB SOI MOSFETs analog figures of merit: effects of ground plane and asymmetric double-gate regime. Solid State Electron. (2013). doi:10.1016/j.sse.2013.02.051
9. Md Arshad, M.K., et al.: RF Behavior of undoped channel ultra-thin body with ultrathin BOX MOSFETs. In: Proceedings of the Silicon Monolitic Integrated Circuits in RF Systems (SiRF), pp. 105–108 (2012)
10. Makovejev, S., et al.: Comparison of small-signal output conductance frequency dependence in UTBB SOI MOSFETs with and without ground plane. In: Proceedings of the IEEE SOI Conference (2011)
11. Makovejev, S., et al.: On extraction of self-heating features in UTBB SOI MOSFETs. In: Proceeding of the 13th International Conference on Ultimate integration on silicon, pp. 109–112 (2012)
12. Kilchytska, V., Andrieu, F., Flandre, D.: On the UTBB SOI MOSFET performance improvement in quasi-double-gate regime. In: Proceedings of the Solid State Device Research Conference (ESSDERC), pp. 246–249 (2012)
13. Bol, D., Kilchytska, V., De Vos, J., Andrieu, F., Flandre, D.: Quasi-double gate mode for sleep transistors in UTBB FD SOI low-power high-speed applications. In: Proceedings of the IEEE SOI Conference (2012)
14. Kilchytska, V., Bol, D., De Vos, J., Andrieu, F., Flandre, D.: Quasi-double gate regime to boost UTBB SOI MOSFET performance in analog and sleep transistor applications. Solid-State Electron. **84**, 28–37 (2013)
15. Md Arshad, M.K., et al.: Effect of parasitic elements on UTBB FD SOI MOSFET RF figures of merit. Solid-State Electron. **97**, 38–44 (2014)
16. Flandre, D., Ferreira, L.F., Jespers, P.G.A., Colinge, J.-P.: Modelling and application of fully depleted SOI MOSFETs for low voltage, low power analogue CMOS circuits. Solid-State Electron. **39**(4), 455–460 (1996)
17. Kilchytska, V., et al.: Influence of device engineering on the analog and RF performances of SOI MOSFETs. IEEE Trans. Electron Devices **50**(3), 577–588 (2003)
18. Raskin, J.-P., Gillon, R., Chen, J., Vanhoenacker-Janvier, D., Colinge, J.-P.: Accurate SOI MOSFET characterization at microwave frequencies for device performance optimization and analog modeling. IEEE Trans. Electron Devices **45**(5), 1017–1025 (1998)
19. Parvais, B., et al.: The device architecture dilemma for CMOS technologies: opportunities and challenges of Finfet over planar mosfet. In: Proceedings of the International Symposium on VLSI Technology, Systems and Applications, pp. 80–81 (2009)
20. Rudenko, T., et al.: Experimental study of transconductance and mobility behaviors in ultra-thin SOI MOSFETs with standard and thin buried oxides. Solid-State Electron. **54**(2), 164–170 (2010)
21. Tenbroek, B.M., Lee, M.S.L., Redman-White, W., Bunyan, R.J.T., Uren, M.J.: Self-heating effects in SOI MOSFET's and their measurement by small signal conductance techniques. IEEE Trans. Electron Devices **43**(12), 2240–2248 (1996)
22. Jin, W., Liu, W., Fung, S.K.H., Chan, P.C.H., Hu, C.: Self-heating characterization for SOI MOSFET based on AC output conductance. IEEE Trans. Electron Devices **48**(4), 730–736 (2001)
23. Kilchytska, V., Levacq, D., Lederer, D., Raskin, J.-P., Flandre, D.: Floating effective backgate effect on the small-signal output conductance of SOI MOSFETs. IEEE Electron Device Lett. **24**(6), 414–416 (2003)
24. Kilchytska, V., et al.: Substrate effect on the output conductance frequency response of SOI MOSFETs. In: Hall, S., Nazarov, A.N., Lysenko, V.S. (eds.) Nanoscaled Semiconductor-on-Insulator Structures and Devices, pp. 221–238. Springer, Dordrecht (2007)

25. O'Neill, A.G., et al.: Reduced self-heating by strained silicon substrate engineering. Appl. Surf. Sci. **254**(19), 6182–6185 (2008)
26. Fiegna, C., Yang, Y., Sangiorgi, E., O'Neill, A.G.: Analysis of self-heating effects in ultrathin-body SOI MOSFETs by device simulation. IEEE Trans. Electron Devices **55**(1), 233–244 (2008)
27. Braccioli, M., Curatola, G., Yang, Y., Sangiorgi, E., Fiegna, C.: Simulation of self-heating effects in different SOI MOS architectures. Solid-State Electron. **53**(4), 445–451 (2009)
28. Kilchytska, V., et al.: Frequency variation of the small-signal output conductance of decananometer MOSFETs due to substrate cross. IEEE Electron Device Lett. **28**(5), 419–421 (2007)
29. Kilchytska, V., Flandre, D., Raskin, J.-P.: Silicon-on-nothing MOSFETs: an efficient solution for parasitic substrate coupling suppression in SOI devices. Appl. Surf. Sci. **254**(19), 6168–6173 (2008)
30. Khakifirooz, A., Cheng, K., Kulkarni, P.: Challenges and opportunities of extremely thin SOI (ETSOI) CMOS technology for future low power and general purpose system-on-chip applications. In: Proceedings of the International Symposium on VLSI Technology, System and Applications, pp. 110–111 (2010)
31. Khakifirooz, A., et al.: Scalability of extremely thin SOI (ETSOI) MOSFETs to sub-20-nm gate length. IEEE Electron Device Lett. **33**(2), 149–151 (2012)
32. Ko, C., Kuan, T., Zhang, K.: A novel CVD-SiBCN low-k spacer technology for high-speed applications. In: Proceedings of the International Symposium on VLSI Technology (2008)
33. Niebojewski, H., et al.: Extra-low parasitic gate-to-contacts capacitance architecture for sub-14 nm transistor nodes. In: Proceedings of the EuroSOI Conference (2013)
34. Ieong, M., et al.: Transistor scaling with novel materials. Mater. Today **9**, 26–31 (2006)
35. Larson, J.M., Snyder, J.P.: Overview and status of metal S/D Schottky-barrier MOSFET technology. IEEE Trans. Electron Devices **53**(5), 1048–1058 (2006)
36. Connelly, D., Clifton, P.: Ultra-thin-body fully depleted SOI metal source/drain n-MOSFETs and ITRS low-standby-power targets through 2018. In: Proceedings of the IEEE Electron Devices Meeting (IEDM), pp. 8–11 (2005)
37. Ohguro, T., Higashi, Y., Okano, K., Inaba, S., Toyoshima, Y.: The optimum device parameters for high RF and analog/MS performance in planar MOSFET and FinFET. In: Proceedings of the International Symposium on VLSI Technology, pp. 149–150 (2012)
38. Lim, T.C., Armstrong, G.A.: The impact of the intrinsic and extrinsic resistances of double gate SOI on RF performance. Solid-State Electron. **50**(5), 774–783 (2006)

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