Chapter 1
Introduction

Analog circuits are still necessary and have a right to exist in a society that is shaped by the digital revolution. The digital advance is driven by various trends of market and economy [12]. High-performance multimedia systems allow a colorful and high-resolution presentation of digital contents while simultaneously navigating and interacting with this medium. In telecommunication and high-speed communication systems the data volume and speed is rising rapidly while the receiving terminals have to process the incoming data stream in time. Computer systems become faster in terms of higher clock speed and contain a huge amount of data storage in order to provide enough performance, which is necessary to execute the growing number of resource intensive applications in a convenient time.

These few examples give an impression on the progress in digital CMOS design. The development of low-power CMOS technologies is mainly forced by power dissipation, manufacturing costs, and speed performance [38]. During the last decades these requirements are mostly obtained by the technological progress of scaling of the device feature sizes to the nanometer domain. Scaling has a significant impact on the density of digital circuits [33]. A larger number of transistors per chip area increases the functionality and lowers the fabrication costs. Another benefit of shrinking structure sizes is the reduction of the parasitic transistor capacitances. Smaller parasitic capacitances cause thus lower dynamic power dissipation in digital logic. The shortest available channel length ensures the maximum speed [103]. However scaling induces undesirable and challenging effects as well [134]. Short-channel MOSFET transistors suffer from the so-called short-channel effects. These are, among other things, velocity saturation, hot electrons, and impact ionization. The breakdown of the transistors is another issue. The scaling of the minimum feature sizes requires the lowering of the supply voltage due to the rising electric fields inside the transistor. A high electric field, which is inversely proportional to the distance, can destroy the transistor. The lowering of the supply voltage has a power saving effect in digital logic. Power saving in digital applications provokes lower costs for cooling and longer battery life-time for handheld devices. Summarizing, the ongoing downscaling of digital CMOS technology pushes the development stimulus in economy and science.

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Unfortunately, the world where digital systems operate has an analog manner and, thus, interfaces between analog and digital blocks have to be created. An interfacing block may be an analog-digital or a digital-analog converter, an amplifier, an I/O buffer, an analog filter, a mixer, or a radio frequency (rf) front-end for a communication channel. From an economical point of view it is favorable for high-volume applications to integrate all analog and digital system blocks into a mixed-signal system on one chip. Although the analog part is not the essential core of such a mixed-signal system, it has a great impact on the overall system performance. The process of scaling affects the performance of the MOS transistors in analog circuitry severely [36]. Therefore, analog system design in digital CMOS is an important and difficult task. One of the major challenges is the low supply voltage, which is limiting the maximum signal swing. The increasing 1/f noise at small structure sizes increases this challenge. Errors due to device mismatch are inversely proportional to the device sizes as well [9]. Additional gate leakage due to reduced gate oxide thickness has a considerable magnitude [4]. The downscaling of CMOS transistors also has some advantages for analog circuits, of course [47]. For example, the transit frequency of the transistors is rising due to the smaller parasitic capacitances, similar to rising clock frequencies of digital logic.

For the purpose of a power and cost saving device, system on chip solutions are desirable. In this work analog continuous-time filters for radio frequency front-ends are presented as an element in a system on chip. Analog continuous-time filters are sometimes preferable in contrast to switched-capacitor filters or digital filters because of the possibility for high-frequency operation and low power dissipation [120]. Many passive discrete-component filter structures are known, which use the inductor as an important element [121]. Integrated inductors offer only small inductance values and are difficult to realize due to the bad quality factor and large chip area. Inductors can be substituted by the use of active analog continuous-time filters, which use an active element, resistors, and capacitors. Active elements may be operational amplifiers or transconductance amplifiers. Integrated analog filter design in nanometer CMOS faces many technological restrictions, for example the limited dynamic range and matching [11]. The limited signal swing, caused by the low supply voltage and the constant noise level, decreases the dynamic range of analog filters at a constant current consumption. Additionally varying device parameters due to mismatch cause a non-constant frequency response. The use of an active tuning system may correct those errors.

This book considers above mentioned issues and is structured as follows. Chapter 2 classifies filters, describes analog filter types and deals with filter approximations. The nanometer CMOS technologies used for the fabrication of the filters presented in this book are described in Chap. 3. Chapter 4 summarizes operational transconductance amplifiers. Chapter 5 describes g_m-C filters for ultra-wide-band applications and compares the results of the implemented ones with the state-of-the-art in literature. The description of realized current-mode filters for software defined radio applications and the comparison of their results with the state-of-the-art follows in Chap. 6. Chapter 7 presents operational amplifier filters for handheld digital video broadcast and LTE applications.

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