Chapter 2
Design of Power, Dynamic Range, Bandwidth and Noise Scalable ADCs

B. Bakkaloglu, S. Kiaei, H. Kim and K. Chandrashekar

Abstract The proliferation of portable electronic devices with high data-rate wireless communication capabilities and the increasing emphasis on energy efficiency is continuously applying pressure on the performance and power consumption of ADCs and other mixed-signal systems. Power scalable designs enable an ADC core to be reusable under different input and sampling frequency conditions improving system efficiency. The power consumption of pipeline and ΣΔ ADCs scales approximately linearly with sampling rate and roughly quadruples for every additional bit resolved. Hence, increasing the performance requirements of an ADC in a system can significantly increase the power consumption to impractical levels especially in a battery powered environment. The approaches presented in this chapter focus on design techniques for power scalable and low power pipeline and bandwidth scalable continuous-time ΣΔ ADCs.

2.1 Introduction

The proliferation of portable consumer electronics and the increasing emphasis on energy efficiency continuously apply pressure on the power and performance of Analog-to-Digital Converters (ADC) and other mixed signal systems. Most electronic systems today rely heavily on digital processing to achieve higher integration and lower static power consumption. In most instances, it is desirable to move from

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analog signal processing to digital signal processing as early as possible in the system's signal chain. Typical analog circuitry provides amplification of desired signals and filtering to improve the input signal dynamic range. The elimination of analog signal processing circuitry results in signals with poorer dynamic range, which carry less information, leading to lower data rates unless significant improvements are made in the resolution and sampling rate (F_S) of ADCs, which serve as the link between the analog and digital domains. Thus, the performance of ADCs is critical to applications such as Software Defined Radio (SDR), bio-medical sensors, and wideband wireless communication systems. These applications typically require pipeline ADCs, which have the capability to efficiently achieve medium to high resolution (8–14 b) at high sampling rates (20–200 MS/s).

The power consumption of pipeline and ΣΔ ADCs scales approximately linearly with sampling rate and roughly quadruples for every additional bit resolved.[1] Hence, increasing the performance requirements of an ADC in a system can significantly increase the power consumption to impractical levels especially in a battery powered environment. The research presented in this chapter focuses on design techniques for power and dynamic range scalable ADCs.

Power scalable designs enable an ADC core to be reusable under different input and sampling frequency conditions improving system efficiency. Power consumption of an ADC is typically optimized for a specified SNDR requirement at a given sampling rate and input frequency range. When the input frequency (f_{in}) range increases, increasing sampling rate to meet Nyquist conditions, the ADC analog core has to be re-designed for more stringent settling time requirements. Same approach is required for radio receivers where blocker profile of the receive channel changes. Scalable and reconfigurable designs aim to reuse the ADC core over a range of sampling and input frequencies by scaling power consumption.

The first part of this chapter presents a power scalable 12 b pipeline ADC that enables or disables OTAs connected in parallel to scale the settling response of Multiplying DAC (MDAC) and Sample/Hold (S/H) amplifiers in order to achieve constant SNDR performance over a range of sampling rates. The proposed technique facilitates optimal power consumption over the entire sampling rate range and reduces design complexity by maintaining constant DC bias conditions in the scaled analog blocks. The reduced design complexity allows for an earlier optimal design to be quickly reconfigured for changed specifications without requiring extensive re-design of the ADC analog core.

The second part of this chapter focuses on the development of an adaptive blocker-rejection wideband continuous-time sigma-delta ADC (CT ΣΔ ADC). An integrated blocker detector reconfigures the ADC architecture in real time to reject interference, which improves the selectivity and sensitivity of the receiver without increasing its dynamic-range requirements. To minimize power consumption, the ADC uses a built-in high-pass filter that performs blocker-level detection without

[1] Cho, T.: Low-power low-voltage analog-to-digital conversion techniques using pipelined architecures. PhD Thesis, University of California, Berkeley (1995)

utilizing any additional circuitry. The adaptive operation relaxes baseband channel-filtering requirements for a WiMAX receiver. The proposed ADC has been integrated in a 130 nm CMOS process occupying a silicon area of 1.5 × 0.9 mm^2. The CT ΣΔ ADC achieves 70 dB of DR, 65 dB of peak signal to noise-plus-distortion ratio (SNDR), and 68 dB of peak signal to noise ratio (SNR) over a 10 MHz signal bandwidth, consuming 18 mW from a 1.2 V supply. The ADC reconfigures the loop-filter topology within 50 μs without any transient impact on bit-error rate. In the blocker-suppression mode, the ADC can withstand 30 dBc blocker at the adjacent channel, achieving −22 dB error-vector magnitude with a 24 Mbps 16-QAM signal.

2.2 Power Scalable Pipeline ADC Design

Power consumption of a pipeline ADC is typically optimized for a specified SNDR requirement at a given sampling rate and input frequency range. When the input frequency (f_{in}) range increases, increasing sampling rate to meet Nyquist conditions, the ADC analog core has to be re-designed for more stringent settling time requirements. Scalable and reconfigurable designs aim to reuse the ADC core over a range of sampling and input frequencies by scaling power consumption. The relationship between the pipeline ADC power, sampling rate and resolution are discussed in the following sections and common design techniques for power scalable ADCs is presented.

2.2.1 MDAC Power and Performance

The architecture of a pipeline stage and its transfer function are shown in Fig. 2.1. For the MDAC to achieve N_i bit accuracy, the output voltage must settle with a gain error of less than $1/2^{Ni}$. The settling characteristic of the SC amplifier at sample instant k is given by

$$Vo[k] = \left(1 + \frac{C_S}{C_F}\right) \cdot \left(1 - e^{-t/n\tau}\right) \cdot \left(\frac{\beta}{\beta + 1/A_{OL}}\right) \tag{2.1}$$

where n is the number of time constants (τ) available for settling, β is the feedback factor of the amplifier, and A_{OL} is the open-loop DC gain of the OTA. The error in the first term from capacitor mismatch can be minimized by good layout practices. The errors in the second and third terms arise from finite settling time and finite open-loop DC gain of the OTA respectively. The error from finite open-loop DC gain can be minimized by designing for A_{OL} to be much greater than 2^{Ni}.

The large signal and small signal settling time of the amplifier can be related to the OTA characteristics as

$$t_{ls} = \frac{VFS}{SR} \tag{2.2}$$

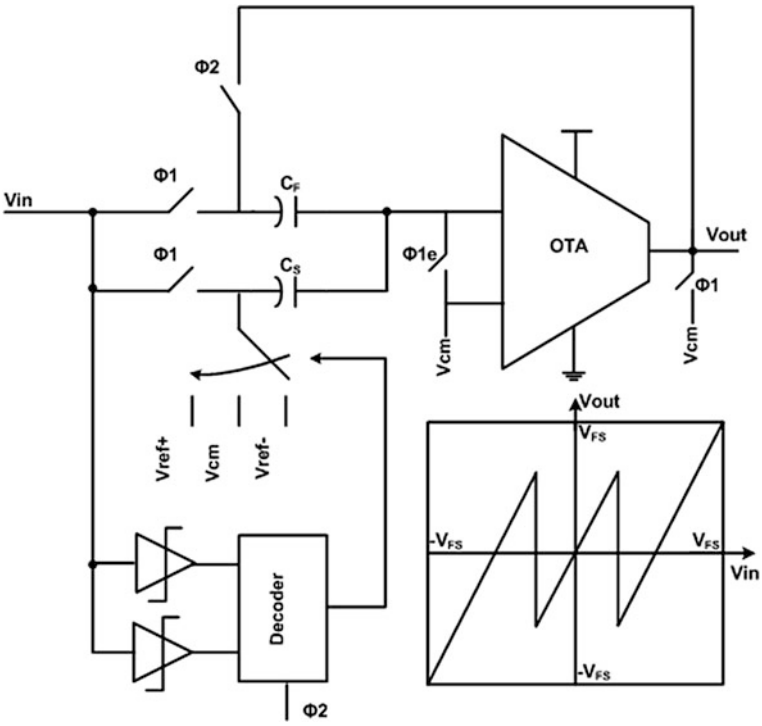

Fig. 2.1 Schematic of a typical 1.5 b/stage MDAC with transfer function

$$t_{ss} = n \cdot \tau = \frac{n}{\beta \cdot GBW} \tag{2.3}$$

where *SR* is the slew rate and *GBW* is the gain bandwidth product of the OTA. The value of n is determine by the resolution required of the stage as $n = N_i \bullet ln(2)$. This assumes a single pole frequency response for the OTA for simplicity. The worst case settling time (t_s) required to settle to N_i bit accuracy, which should be less than approximately one-half clock cycle ($\sim 1/2F_S$), is determined by the slew rate (*SR*) and gain-bandwidth product (*GBW*) of the OTA as[2]

$$t_s = \left(\frac{VFS}{SR}\right) + \left(\frac{n}{\beta \cdot GBW}\right) \leq \frac{1}{2 \cdot F_S} \tag{2.4}$$

For a single stage OTA, the *SR* and *GBW* are functions of the load capacitance (C_L), and the tail current (I_t) and transconductance (gm) of the OTA's input pair. Substituting these relationships in Eq. 2.4, the following relation between the sampling rate and OTA power is derived

[2] Lotfi, R., Taherzadeh–Sani M., Azizi, M.Y., Shoaei, O.: A low-power design methodology for high-resolution pipelined analog-to-digital converters. In: Proceedings of ISLPED, pp. 334–339 (2003)

$$\frac{1}{2 \cdot F_S} \approx \left(\frac{VFS}{I_t} + \frac{n}{\beta \cdot gm} \right) \cdot C_L \tag{2.5}$$

It can be seen from Eq. 2.5 that given a sampling rate and resolution requirement, the OTA current is a critical design parameter. The load capacitance is determined by thermal noise consideration and is typically fixed parameter during the design of the MDAC stage OTA. If sampling rate is increased, the OTA current must also be increased to maintain constant performance. This fact is utilized in the design and operation of power scalable pipeline ADCs.

The optimal OTA tail current ($I_{t,opt}$) of a pipeline MDAC stage for a given capacitive load, resolution and sampling rate can be shown to be

$$I_{t,opt} = \left(\frac{C_L}{2} \right) \cdot \left(VFS + \frac{n \cdot V_{dsat}}{2 \cdot \beta} \right) \cdot F_S \tag{2.6}$$

where V_{dsat} is the difference between the input pair transistor's V_{GS} and threshold voltage (V_{th}). This equation is derived assuming that a constant V_{dsat} is maintained. Equation (2.6) shows that the optimal power of the MDAC stage is approximately linearly related to the sampling rate. However, if an existing design is to be operated at a higher sampling rate and the power is increased to maintain performance, the relationship is no longer linear. While slew rate scales linearly with the tail current, the gain-bandwidth product of the OTA is proportional to the square-root of the current. Thus, the MDAC stage power does not scale linearly with sampling rate and for situations where small signal settling is much larger than large signal settling, the power is approximately proportional to the square of the sampling rate.

2.2.2 Bias Current Scaling and Switched-Opamp Scaling

Power scalability in pipeline ADCs is typically implemented by scaling the bias currents of the OTAs as shown in Fig. 2.2.[3,4,5,6] Scaling OTA bias currents results in large variations of the transistors' DC bias conditions. At the lower end of the sampling rate range the bias transistors are in moderate or weak inversion. In the sub-threshold region transistor mismatch increases thereby increasing the OTA

[3] Hernes, B. et al.: A 1.2 V 220MS/s 10b pipeline ADC implemented in 0.13/spl mu/m digital CMOS. In: IEEE International Solid-State Circuits Conference Digital Technology Papers, vol. 1 pp. 256–526 (2004)

[4] Andersen, T.N. et al.: A 97mW 110MS/s 12b pipeline ADC implemented in 0.18 mm digital CMOS. In: Proceedings of European Solid-State Circuits Conference, pp. 247–250 (2004)

[5] Gulati, K., Lee, H.-S.: A low-power reconfigurable analog-to-digital converter. IEEE J. Solid-State Circuits **36**(12), 2446–2455 (2001)

[6] Ahmed, I., Johns, D.A.: A 50-MS/s (35 mW) to 1-kS/s (15 uW) power scaleable 10-bit pipelined ADC using rapid power-on opamps and minimal bias current variation. IEEE J. Solid-State Circuits **40**(12), 2446–2455 (2005)

offset. The transistors are also more susceptible to transient disturbances due to the exponential dependence of the drain current on the gate voltage. Increasing the bias currents with sampling rate also increases the overdrive voltage (V_{dsat}) of the transistors. This reduces the maximum voltage swing at the OTA inputs and outputs, and adversely impacts the dynamic range of the ADC during low power supply operation. Also, in order to maintain a high OTA DC open-loop gain, transistors must be biased in saturation in order to maintain their high output resistance. Bias current scaling significantly increases the design complexity since the OTA operation must be verified not only over temperature and process variations, but also, over large bias current variations.

In Eq. (2.6) it was shown that the optimal OTA current required for a given accuracy and load capacitance scales linearly with sampling rate. However, this assumes that the V_{dsat} is maintained constant. Since a constant V_{dsat} cannot be maintained using bias current scaling, the scaled power consumption exceeds the optimal power required at a given sampling rate as shown in Fig. 2.3. Thus, bias current scaling requires that the OTA must be designed for the highest sampling rate with power scaled down for lower sampling rates. This leaves the design more susceptible to transistors operating in sub-threshold at lower sampling rates.

Powering off OTAs in the sampling phase, coupled with bias current scaling, provides appreciable power savings (see footnote 6). The OTAs are powered on only during the hold phase thereby halving the average power consumption. This technique is also utilized in switched-opamp ADCs.[7,8,9] However, a portion of the hold phase is required to power on the OTA, which reduces the time available for output voltage settling. The power-on interval occupies a significant portion of the hold phase at high sampling rates, requiring an increase in the OTA power to compensate for the loss of available settling time. The design challenges of a rapid power-on OTA limit this approach to low sampling rate applications.

The following chapter will present a power scalable pipeline ADC technique that enables or disables OTAs connected in parallel to scale the settling response of the MDAC and S/H amplifiers in order to achieve constant SNDR performance over a range of sampling rates. The proposed technique facilitates optimal power consumption over the entire sampling rate range and reduces design complexity by maintaining constant DC bias conditions in the scaled analog blocks. The reduced design complexity allows for an earlier optimal design to be quickly reconfigured for changed specifications without requiring extensive re-design of the ADC analog core.

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[7] Kim, H-C., Jeong, D-K., Kim, W.: A partially switched-opamp technique for high-speed low-power pipelined analog-to-digital converters. IEEE Trans. Circuits Syst. I: Regul. Pap. **53**(4), 795–801 (2006)

[8] Waltari, M. Halonen, K.A.I.: 1-V 9-bit pipelined switched-opamp ADC. IEEE J. Solid-State Circuits **36**(1), 129–134 (2001)

[9] Wu, PY., Cheung, V.S-L., Luong, H.C.: A 1-V 100-MS/s 8-bit CMOS switched-opamp pipelined ADC using loading-free architecture. IEEE J. Solid-State Circuits **42**(4), 730–738 (2007)

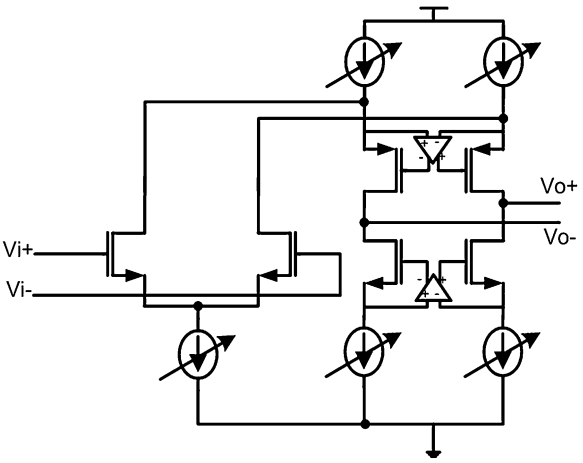

Fig. 2.2 Folded-cascode OTA with variable bias for scalable pipeline ADC

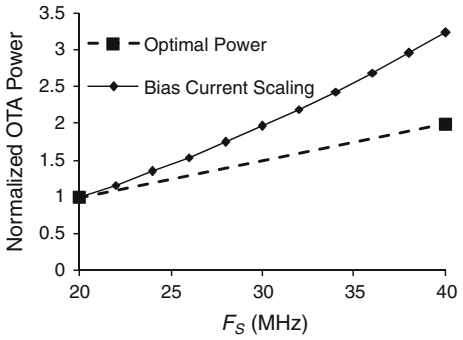

Fig. 2.3 Normalized OTA power with bias current scaling compared to optimal power over a range of sampling rates

2.3 Parallel OTA Scaling Approach

This section presents a design technique for scalable pipeline ADCs that enables or disables OTAs connected in parallel to scale the settling response of the MDAC and S/H amplifiers in order to achieve constant SNDR performance over a range of sampling rates. The proposed technique facilitates linear and optimal power consumption over the entire sampling rate range and reduces design complexity by maintaining constant DC bias conditions in the scaled analog blocks. The reduced design complexity allows for an earlier optimal design to be quickly reconfigured for changed specifications without requiring extensive re-design of the ADC analog core. In,[10] programmability in Gm-C filters was achieved by switching in

[10] Pavan, S., Tsividis, Y.P., Nagaraj, K.: Widely programmable High-frequency continuous-time filters in digital CMOS technology. IEEE J. Solid-State Circuits **35**(4), 503–511 (2000)

transconductances (Gm) in parallel. Since amplifiers in switched capacitor stages are essentially Gm stages driving capacitor loads, a similar switched transconductance technique can also be used in pipeline ADCs by enabling or disabling individual OTAs in parallel.

2.3.1 Description of Parallel OTA Scaling

In Eq. (2.4), it can be seen that the settling performance of switched capacitor amplifiers can be scaled by varying the OTA bias current. Increasing the OTA bias current increases the current available for slewing and increases the small signal settling performance by increasing the transconductance of the OTA. The improvement in settling performance is obtained at the cost of disturbing the DC bias conditions of OTA transistors. In the proposed parallel OTA scaling technique, scalable settling performance is obtained by enabling or disabling OTAs connected in parallel in the S/H and MDAC stages of the pipeline ADC. A scalable MDAC stage implemented using two OTAs connected in parallel is shown in Fig. 2.4. Since the OTAs only share the input and output nodes, the DC bias conditions of the internal nodes of each individual OTA are unperturbed.

2.3.2 Settling Analysis of Parallel OTA Scaling

The output current signal of the identical individual OTAs, each with transconductance gm_i, are summed at the shared output, scaling the effective transconductance (Gm_{eq}) of the stage as

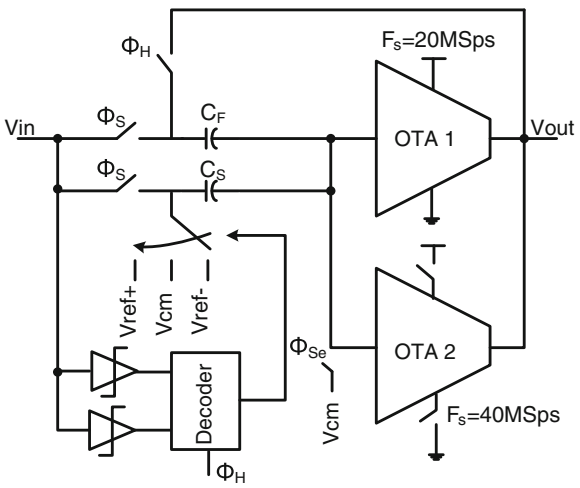

Fig. 2.4 Implementation of a scalable MDAC stage using the parallel OTA scaling technique

$$i_{out} = \sum_{i=1}^{k} i_{out,i} = \sum_{i=1}^{k} gm_i \cdot v_{in} \tag{2.7}$$

$$Gm_{eq} = \frac{i_{out}}{v_{in}} = \sum_{i=1}^{k} gm_i = k \cdot gm_i \tag{2.8}$$

Thus, Gm_{eq} is an integer multiple of gm_i and can be varied in discrete steps by enabling or disabling parallel OTAs. Since the GBW is proportional to the transconductance, the GBW of the equivalent OTA (GBW_{eq}) is now proportional to the number of parallel OTAs as

$$GBW_{eq} = \frac{Gm_{eq}}{C_L} = k \cdot \frac{gm_i}{C_L} = k \cdot GBW_i \tag{2.9}$$

where GBW_i is the gain bandwidth product of an individual OTA.

When the input voltage signal is stepped causing the OTAs to slew, each individual OTA contributes a current $I_{t,i}$ to slew the output voltage. Thus, the slew rate of the equivalent OTA (SR_{eq}) also increases linearly with the number of enabled parallel OTAs as

$$SR_{eq} = \frac{\sum_{i=1}^{k} I_{t,i}}{C_L} = k \cdot \frac{I_{t,i}}{C_L} = k \cdot SR_i \tag{2.10}$$

where SR_i is the slew rate of an individual OTA. Thus, the effect of enabling parallel OTAs on the settling time response of the switched capacitor amplifier is

$$t_s = \frac{1}{k} \cdot \left(\frac{VFS}{I_{t,i}} + \frac{N_i \cdot \ln(2)}{\beta \cdot gm} \right) \cdot C_L \leq \frac{1}{2 \cdot F_S} \tag{2.11}$$

The effect of parallel OTA scaling on the output settling response is illustrated in Fig. 2.5. From Eq. (2.11), it can be seen that the settling time response of the switched capacitor amplifier is now inversely proportional to the number of enabled parallel OTAs. Thus, the total power of the switched capacitor stage scales linearly with sampling rate. This linear relationship between power and sampling rate allows for optimal power consumption to be achieved over the entire sampling rate range.

The optimal OTA tail current ($I_{t,opt}$) of an MDAC stage at a fixed sampling rate, expressed by Eq. 3.6, assumes a fixed V_{dsat} for the input differential pair of the OTA, determined by matching and input voltage swing considerations. In the parallel OTA scaling technique, since the DC bias conditions of individual OTAs are unchanged, a constant V_{dsat} is maintained over the sampling rate range. Thus, if the individual OTAs are designed for optimal power consumption at one sampling rate, the scaled power consumption will track the optimal power consumption over the sampling rate range.

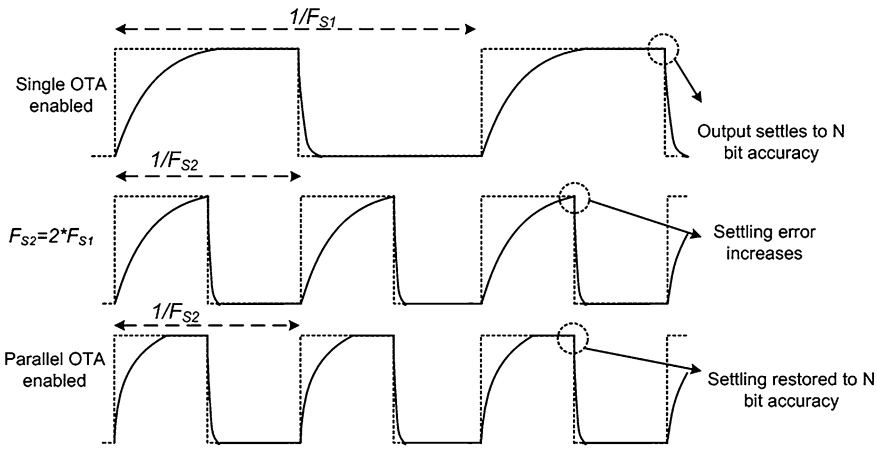

Fig. 2.5 Illustration of the effect of parallel OTA scaling on the output settling response

2.3.3 Parallel OTA Scaling Design Considerations

When the OTAs are connected in parallel, the effective output resistance is reduced. Since this decrease is accompanied by an increase in the effective transconductance, the DC open-loop gain of the OTAs in parallel is equal to open-loop gain of an individual OTA. This is also a result of the internal DC bias conditions remaining unchanged.

The previous analysis of the MDAC settling response assumes that the individual OTAs exhibit single-pole response. This is approximately true if the non-dominant pole of the OTA is located at a much higher frequency than the dominant pole. When two OTAs are connected in parallel the dominant pole frequency increases by a factor of 2. The non-dominant pole remains unchanged since the bias conditions of the internal nodes that are responsible for the non-dominant pole are unchanged. This results in a reduction of the phase margin. The frequency of the non-dominant pole limits the number of parallel OTAs that can be enabled before the phase margin is insufficient for stable operation.

The addition of OTAs in parallel also increases the total parasitic capacitance at the input (C_p). This results in a reduction of the feedback factor, which increases the settling time response of the MDAC. The load capacitance is also increased by the parasitic capacitance. The effect on the feedback factor and C_L will be minimized if the MDAC capacitors are much larger than the input parasitic capacitances of the OTA.

2.3.4 Scalable Pipeline ADC Implementation

The ADC core comprises a S/H stage, ten 1.5 b stages, and a 2 b flash ADC as shown in Fig. 2.1. The design process targeted a sampling frequency range between 20 and 40 MS/s. The reference voltages required for the analog to digital conversion is generated on-chip by a reference amplifier driving a resistor string. The ADC draws signal dependent current from the reference amplifier, which has finite settling time, leading to significant degradation of SNDR if the output impedance increases in the signal bandwidth. In order to minimize power consumption and maintain a low output resistance over the signal bandwidth, a reference amplifier with low DC output resistance and low bandwidth driving a large off-chip load capacitor is used. The large load capacitance ensures low output impedance at frequencies above the bandwidth of the reference amplifier.[11]

A clock buffer is used to buffer the off-chip clock and the non-overlapping clock signals are generated on-chip. In order to reduce the power consumption of the clock circuitry and layout complexity, 3 non-overlapping clock generators, each driving 4 stages (including S/H and Flash ADC), were used. This reduced the load capacitance driven by each clock generator and allowed for lower power dissipation in the clock circuitry. The RSD algorithm to correct for comparator offsets was implemented off-chip allowing for verification of individual stages during testing. Since comparator offsets as large as one-fourth the single-ended full-scale voltage are corrected for, dynamic comparators, without preamplifiers, are used in order to minimize power consumption.[12] The schematic of the dynamic comparator is shown in Fig. 2.6. Bootstrapped switches are used in the signal path of the S/H stage to minimize distortion caused by the dependence of the transistors' on-resistance on the gate-to-source and gate-to-drain voltages.

2.3.5 S/H and MDAC Amplifiers

The schematic of the scalable OTA used in the MDAC and S/H stages is shown in Fig. 2.7. The two individual OTAs are implemented in the folded cascode topology. Gain-boosting is used only for OTAs in the S/H and first 4 stages in order to achieve sufficient gain for 12 b resolution. The individual OTAs are each designed for operation at 20 MS/s and only one OTA is enabled in each stage for 20 MS/s operation.

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[11] Maulik, P.C. et al.: A 16-Bit 250-kHz delta sigma-modulator and decimation filter. IEEE J. Solid-State Circuits **35**(4), 458–467 (2000)

[12] McCarroll, B.J., Sodini, C.G., Lee, H-S.: A high-speed CMOS comparator for use in an ADC. IEEE J. Solid-State Circuits **23**(1), 159–165 (1988)

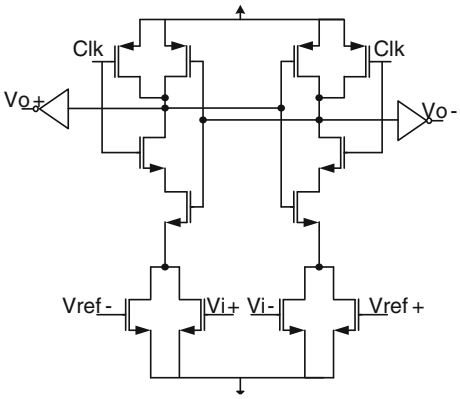

Fig. 2.6 Schematic of dynamic comparator

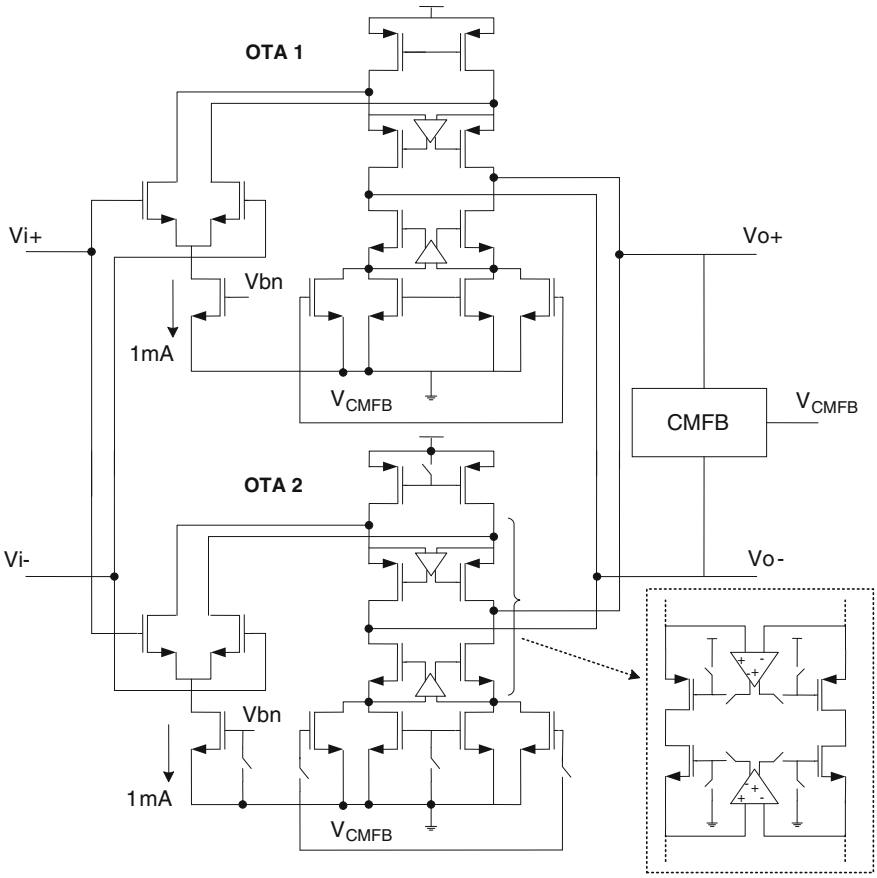

Fig. 2.7 Schematic of reconfigurable OTA in first MDAC stage which is implemented with two gain-boosted folded cascode OTAs for operation at 20 and 40 MS/s

The disabling switches, shown in Fig. 2.5, ensure that the unutilized OTA is turned off and exhibits a high output impedance so as not to affect the operation of the enabled OTA. A low or comparable output resistance in the disabled state will adversely impact the DC open-loop gain of the enabled OTA. Since the switches drive only transistor gates and do not pass any analog signals, low on-resistance is not required and minimum sized transistors are sufficient. A single switched capacitor common-mode feedback circuit is sufficient to maintain the output common-mode since the OTAs' outputs are shared.

When both parallel OTAs are enabled for operation at 40 MS/s, the GBW_{eq} and SR_{eq} are expected to be doubled. However, due to the non-dominant pole and the increase in the load capacitance from increased parasitic capacitance at the OTA input, a slightly lower than expected increase is achieved. The simulated open-loop frequency of the individual OTA in the first stage is compared to the response with two OTAs in parallel in Fig. 2.8. It can be seen that enabling an OTA in parallel increases GBW_{eq} by a factor of 1.97. The effect of reducing the dominant and non-dominant poles' separation is largely responsible for the <2 increase. The increased OTA input parasitic capacitance has a less significant effect since the sampling capacitors are comparatively larger. The simulated step response of an

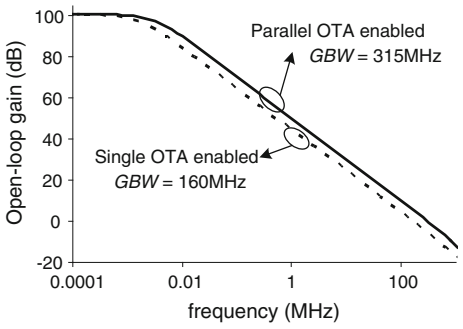

Fig. 2.8 Simulated scaling of open-loop frequency response of scalable OTA from first MDAC stage

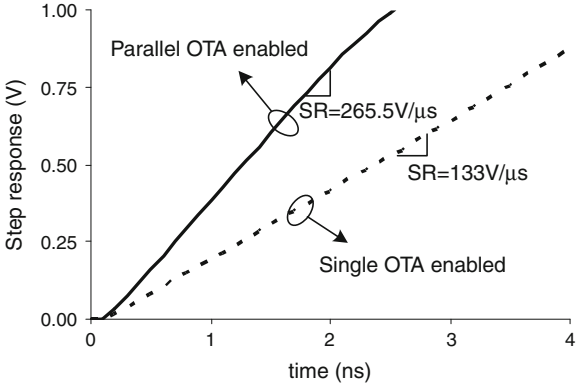

Fig. 2.9 Simulated scaling of step response of scalable OTA from first MDAC stage

individual OTA is compared to the response of two parallel OTAs in Fig. 2.9. The slew rate is increased by a factor of 1.996 when the parallel OTA is enabled. Adequate margin was incorporated in the final OTA design specifications to account for the effect of the non-dominant pole and process variation.

2.4 Characterization Results for the Power Scalable ADC

The proposed ADC was fabricated in a 1.8 V 0.18 μm CMOS process and occupies a die area of 1.9 mm^2. The die micrograph is shown in Fig. 2.10. For test purposes, two additional OTAs were added in parallel in the S/H and MDAC stages for a total of four OTAs in each stage. The differential full-scale voltage of the ADC is 1.2 V_{pp}. At $F_S = 20$ MS/s, only one OTA is enabled in each stage and the analog blocks consume 36 mW. When F_S is increased to 40 MS/s, a second parallel OTA is enabled in each stage and the measured analog power consumption increases to approximately 72 mW, which is twice the power consumed at 20 MS/s. Thus, the ADC achieves linear power scaling with respect to sampling rate. If a continuous range of power scaling is desired, bias current scaling can be used at each OTA over a ±10 MS/s range. Since the bias current scaling is utilized only over a limited frequency range, the resulting DC bias variation is minimized by the parallel OTA technique.

Figure 2.11 shows the measurement results for the SNR and SNDR of the ADC versus the input signal frequency at 20 and 40 MS/s sampling rates. For each F_S, it can be seen that the SNR and SNDR are fairly constant over the input frequency within the Nyquist range. The SNR for an input signal of 1 MHz sampled at 20 MS/s is 66.6 dB and the SNDR is 66.2 dB (ENOB = 10.7 b). At a sampling rate of 40 MS/s, the SNR for a 1 MHz input signal is 62.2 dB and SNDR is 62 dB (ENOB = 10 b). The reduction of SNR from 20 to 40 MS/s operation is due to the

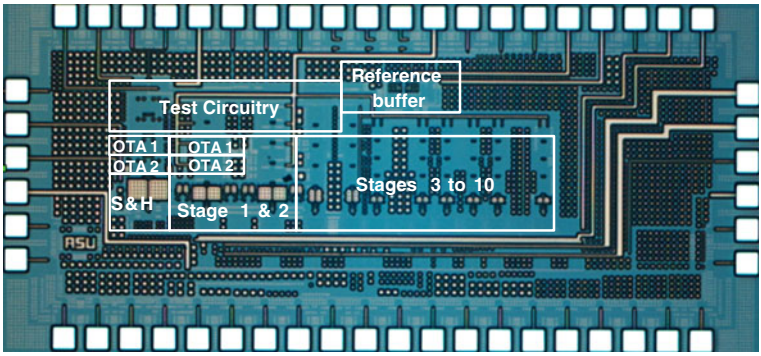

Fig. 2.10 Die micrograph of the power scalable ADC

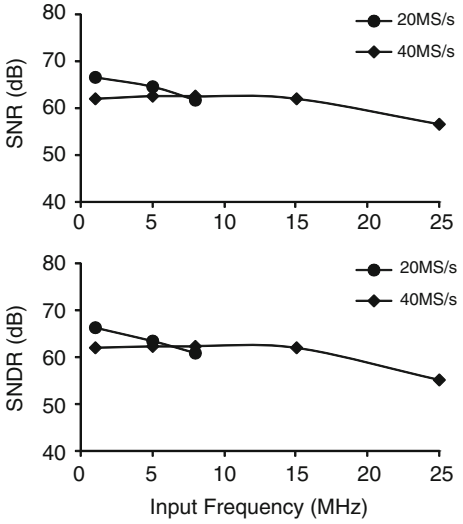

Fig. 2.11 Measured SNR and SNDR versus input frequency for $F_S = 20$ and 40 MS/s

increased supply and substrate noise from the on-chip digital logic and I/O circuitry coupling to the analog circuitry. The Figure of Merit (FOM), expressed in Eq. (2.12), at 20 MS/s is calculated to be 1.1 pJ and at 40 MS/s is calculated to be 1.75 pJ.

$$FOM = \frac{Power}{F_S \cdot 2^{ENOB}} \tag{2.12}$$

Since the power scales linearly with the sampling rate, the increase in the FOM at 40 MS/s operation can be attributed largely to the reduction in the effective resolution caused by increased switching noise from the digital logic and I/O circuitry. The measured power versus sampling rate is plotted in Fig. 2.12. The measured SNR and SNDR at 60 MS/s (3 parallel OTAs enabled) and 80 MS/s (4 parallel OTAs enabled) are plotted versus input frequency in Fig. 2.13. A SNDR of 57.4 dB (ENOB = 9.24 b) is obtained at 60 MS/s and the SNDR

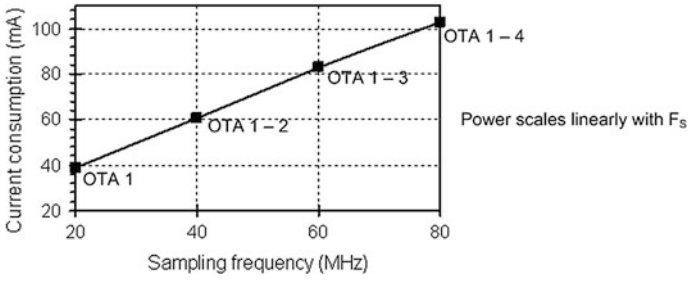

Fig. 2.12 Measured ADC power versus sampling rate

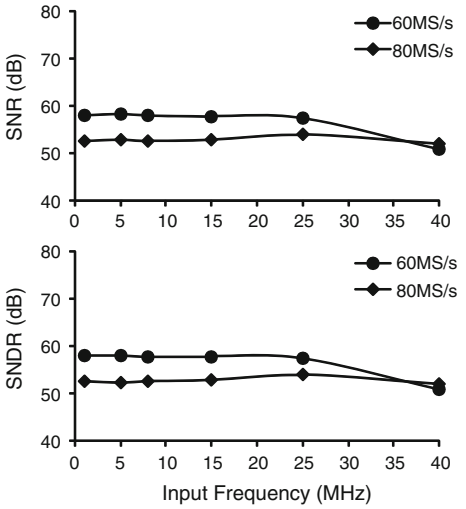

Fig. 2.13 Measured SNR and SNDR versus input frequency for $F_S = 20$ and 40 MS/s

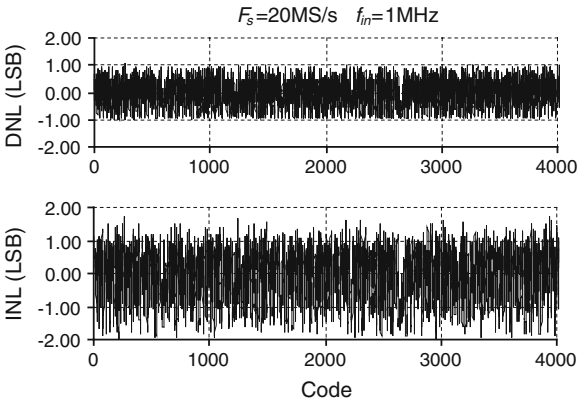

Fig. 2.14 Measured DNL and INL

Table 2.1 Measurement summary for the Scalable Pipeline ADC

	20 MS/s	40 MS/s
Technology	0.18 μm CMOS	
Power supply	1.8 V	
Resolution	12 b	
Full scale input	1.2 V_{pp}	
Area	1.9 mm^2	
Analog power	36 mW	72 mW
SNR (f_{in} = 1 MHz)	66.6 dB	62.2 dB
SNDR (f_{in} = 1 MHz)	66.2 dB	62 dB
ENOB (f_{in} = 1 MHz)	10.7 b	10 b
DNL, INL	±1 LSB, 1.7/−1.97 LSB	

further reduces to 52.2 dB (ENOB = 8.4 b) at 80 MS/s operation. The additions of the third and fourth parallel OTAs demonstrate the limitation on the number of possible parallel OTAs before degradation in settling performance. The individual OTAs were designed for operation between 20 MS/s and 40 MS/s. The location of the non-dominant pole was determined accordingly. Enabling more than two OTAs in parallel reduces the phase margin significantly affecting the settling performance. The DNL and INL, measured using the code density test for $F_S = 20$ MS/s and $f_{in} = 1$ MHz, are plotted in Fig. 2.14. The measurement results are summarized in Table 2.1.

2.5 Review of Recent ΣΔ ADCs with Adaptive Bandwidth and Interferer Filtering

In the second section of this chapter we will analyze techniques to adjust the loop filter bandwidth, dynamic range and out of band interferer rejection performance of continuous time ΣΔ ADCs. Highly digital direct-conversion receivers can reduce system complexity by removing analog automatic-gain control and DC-offset cancellation loops at the expense of increased DR requirements on the ADC. However, if the ADC DR specification is too high, the silicon area and power consumption of the receiver employing this approach will be larger than that of conventional direct conversion (DC) receivers.[13] In order to resolve this issue, several ADC design techniques have been proposed. In this subsection, these techniques are described briefly and their advantages and disadvantages are discussed.

2.5.1 Reconfigurable Discrete-Time Multi-Stage Noise Shaped ΣΔ ADC

During normal operation of the receiver, both the signal power and the interferer profile can change, and thus stringent channel-select filtering or ADC performance is not always necessary. A flexible and reconfigurable architecture targetted at the RF front-end and the ADC would allow for the optimization of power consumption and SNR performance of the receiver depending on operating conditions. Recently, a reconfigurable discrete-time (DT) multi-stage noise-shaped (MASH) ΣΔ ADC has been proposed for power-adaptive operation under blocker

[13] Garrity, D. et al.: A single analog-to-digital converter that converts two separate channels (I and Q) in a broadband radio receiver. IEEE J. Solid-State Circuits **43**(6), 1458–1469 (2008)

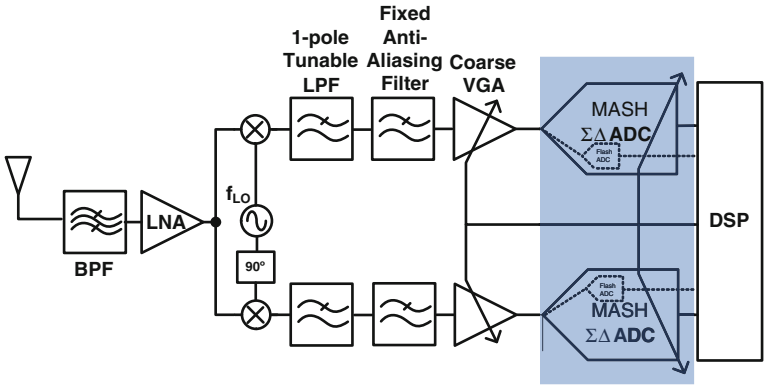

Fig. 2.15 Receiver architecture with a reconfigurable DT MASH ΣΔ ADC (see footnote 15)

condition.[14] Figure 2.15 shows a receiver architecture with the MASH ΣΔ ADC. It has a single-pole low-pass filter, fixed anti-aliasing filter, and coarse variable-gain amplifier in front of a MASH ΣΔ ADC. The system reconfigures the order of the ADC based on desired channel and interferer levels at the ADC input. The power-level estimation is performed by a 5-bit flash ADC at the modulator input and digital-signal processing (DSP). Latency in DSP processing may result in failure to meet the standard specifications or system instability when a high blocker is present at the ADC and a VGA control loop is required.

2.5.2 CT ΣΔ ADC with Increased Blocker Suppression

CT ΣΔ ADCs are widely used for mobile wireless systems because they can achieve high DR with low power consumption. In addition, thanks to their implicit anti-aliasing filtering and channel select-filtering performance by an STF, the requirements for analog baseband filtering or ADC DR can be relaxed.

Figure 2.16 shows commonly used CT ΣΔ ADC architectures. To increase immunity to interferers, a CT ΣΔ ADC with a chain of integrator with distributed feedback (CIFB) architecture can be used since its STF has a faster roll-off in out-of-channel frequencies in comparison to feed-forward loop architectures. Since each integrator output has a significant amount of input signal swing, lower integrator coefficients are necessary to avoid signal clipping and should be implemented with larger capacitance increasing silicon area. In addition, a reduced integrator coefficient in the first stage results in increased input-referred thermal noise and non-linearity caused by the following stages. Therefore, power

[14] Malla, P. et al.: A 28 mW spectrum-sensing reconfigurable 20 MHz 72 dB-SNR 70 dB-SNDR DT ADC for 802.11n/WiMAX receivers. In: IEEE ISSCC Digital Technical Papers, pp. 496–497 (2008)

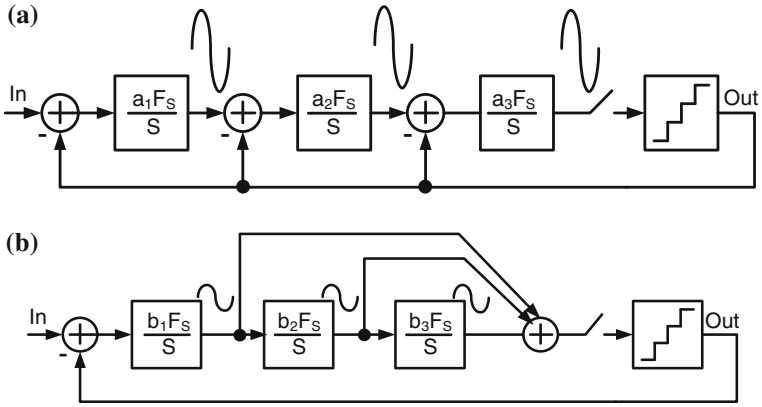

Fig. 2.16 **a** Chain of integrator with distributed feedback **b** chain of integrators with feedforward summation architecture

consumption of these stages should be increased to reduce their non-ideal contributions.

For low-power implementation, a chain of feed-forward summation (CIFF) topology can be used. Since each integrator output contains only a quantization-error signal, its output swing is relatively small compared to the feedback topology. Therefore, large integrator coefficients can be used and noise and distortion contribution of the second and following stage integrators caused by reduced bias current can be tolerated. However, since a CIFF architecture exhibits gain peaking in its STF at high frequencies, this architecture will be overloaded or unstable when high-power interferers are applied to the modulator input.

To maintain the fast roll-off while reducing power consumption and silicon area, a CT ΣΔ ADC with feed-forward topology can be modified as shown in Fig. 2.17.[15] If the two filters are complementary and they satisfy the following condition:

$$H_{LPF}(s) \cdot H_{HPF}(s) = 1,$$

the STF can be modified without changing the noise transfer function (NTF), which is given by

$$STF(s) = H_{LPF}(s)\frac{LF(s)}{1 + LF(s)}, \tag{2.13}$$

where $LF(s)$ is the loop filter of the modulator. These additional filters scarcely increase the total power consumption and area for narrow-band applications. However, if this ADC were used for wideband and high-speed applications such as

[15] Philips, K. et al.: A continuous-time ΣΔ ADC with increased immunity to interferers. IEEE J. Solid-State Circuits **39**(12), 2170–2178 (2004)

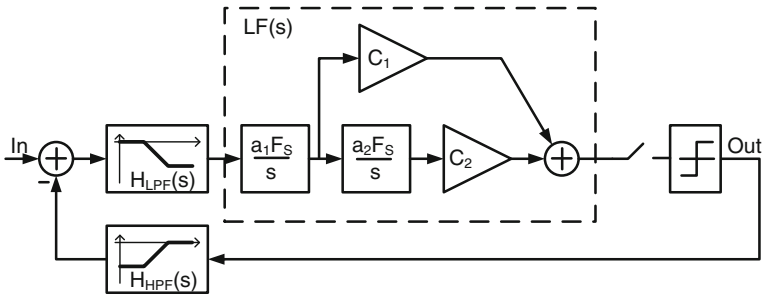

Fig. 2.17 ΣΔ ADC with increased interferer immunity (see footnote 15)

WiMAX, the required matching of the two filters would be very stringent. This requirement would increase the complexity of this architecture.

2.5.3 Direct Feedforward Compensation Technique in ΣΔ ADCs

Figure 2.18a shows a conventional single-loop ΣΔ ADC architecture. When the input signal *In* is stationary, the quantizer output *Out* is also stationary. Therefore, the error signal *E* entering the loop filter has small amplitude. If the input *In* changes abruptly, the quantizer output *Out* is still stationary during the excess loop delay. Consequently, the error signal *E* is fed to the loop filter and the modulator will be overloaded. This scenario frequently occurs in automobile tuner systems, which experience fading of received signals due to dynamically changing interferers. To avoid this problem, a direct feed-forward compensation technique in a ΣΔ DC has been proposed, as shown in Fig. 2.18b.[16] If a non-delayed feedback technique is employed, the quantizer output *Out* is not delayed with respect to the input *In*. Therefore, the error signal *E* can remain of small amplitude. However, this topology still requires channel-select filters to protect the ADC from overload when a high interferer is accompanied by the desired channel signal.

2.5.4 Comparing Advantages and Disadvantages of the Recent ΣΔ ADCs

In the previous subsection, recent ΣΔ ADC design techniques are briefly reviewed. The reconfigurable DT MASH ΣΔ ADC can optimize power consumption and SNR performance based on the desired channel signal and blocker-power levels.

[16] Yamamoto, T., Kasahara, M., Matsuura, T.: A 63 mW 112/94 dB DR IF bandpass ΣΔ modulator with direct feed-forward compensation and double sampling. IEEE J. Solid-State Circuits **43**(8), 1783–1794 (2008)

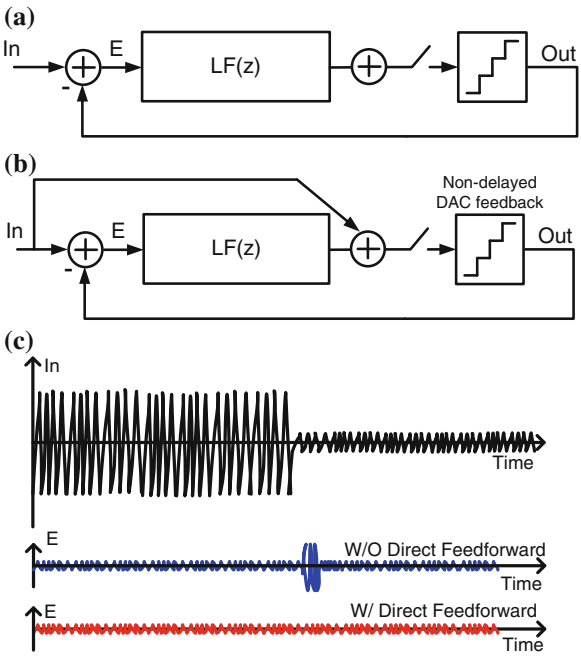

Fig. 2.18 **a** Conventional S ADC, **b** SD ADC with direct feedforward compensation, and **c** illustrations of transient waveforms with sudden input changing (see footnote 16)

The power-level estimation is performed by a 5-bit flash ADC at the modulator input with digital-signal processing, and thus latency in DSP processing can result in either failure to meet the standard specifications or system instability when a high blocker is present at the ADC. Moreover, this approach requires a VGA control loop as well as an anti-aliasing filter due to DT implementation.

The second approach, which employs addition filters in the feed-forward and feedback path, can achieve strong blocker-suppression strength with low power consumption. However, the required matching condition is very stringent, increasing the complexity of this architecture, if this ADC is used for wideband and high-speed applications. In addition, the filter in the feedback path would increase excess loop delay and thus reduce the stability of the modulator.

The last approach uses a direct feed-forward path to protect the ADC from overloading and instability when high blockers are applied or input signals change abruptly. However, this topology requires channel-select filters to protect the ADC from overload when a high interferer is accompanied by the desired channel signal.

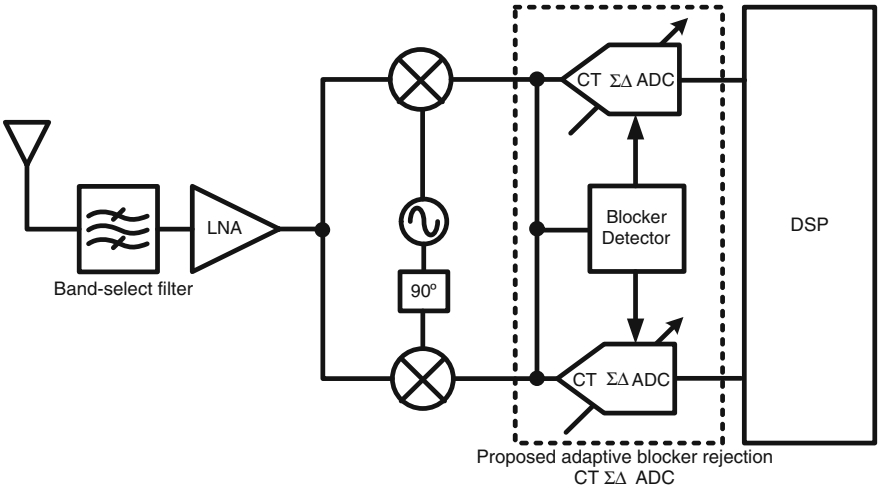

Fig. 2.19 Direct Conversion (DC) receiver architecture with the proposed adaptive blocker rejection CT ΣΔ ADC

2.6 Blocker-Adaptive ΣΔ ADC for Mobile WIMAX Applications

2.6.1 ADC Requirements

Figure 2.19 shows a DC receiver with the proposed SD ADC approach. By exploiting adaptive blocker rejection performance of the ADC, the receiver can improve system selectivity without an additional channel select filter and optimize ADC performance based on the blocker level. This section describes the procedure of defining DR and linearity requirements of the ADC and the same procedure presented in Chap. 1 is employed to define the specifications.

Before determining the ADC dynamic range (DR) requirement, the STF of the modulator should be defined because the DR specification strongly depends on the filtering performance of the STF. The reconfigurable modulator has two operation modes: One is normal mode and the other is blocker suppression mode. Details of the modes will be explained in the next section. The DR requirement is defined under condition of the worst case in which the desired input signal has the lowest power level and blockers have the strongest power level. In this condition, the modulator should be operated in the blocker suppression mode. If the STF has a second-order LPF characteristic with a corner frequency of 20 MHz, The STF can theoretically have 6 dB attenuation at the adjacent channel and 12 dB attenuation at the alternate channel frequency as illustrated in Fig. 2.20.

Figure 2.21 illustrates the link budget analysis to determine the ADC dynamic range requirements. With a 1.2 V maximum supply for 130 nm CMOS process,

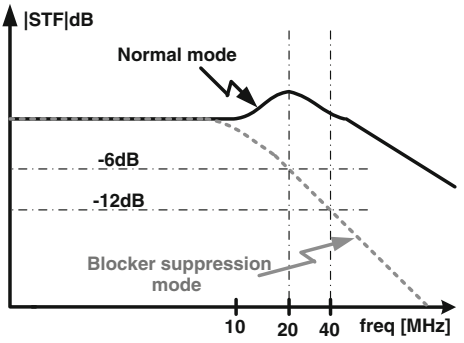

Fig. 2.20 Illustrated STFs of the normal and blocker suppression modes

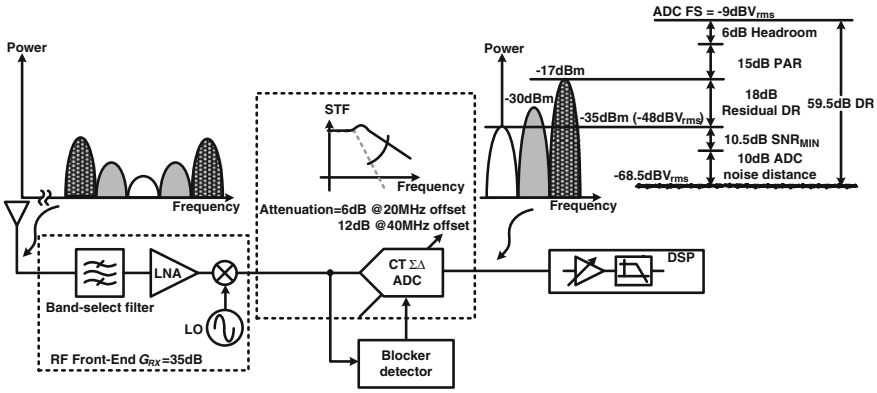

Fig. 2.21 ADC dynamic range requirement under blocking conditions

the full-scale input voltage (FS) of the ADC is set to 1 V_{pk-pk} differential. A 6 dB headroom margin is taken into account to cover DC offsets and transient signal variations. OFDM modulation used in the WiMAX standard has a typical PAR in the range of 12–17 dB depending on the number of sub-channels, and the ADC should account for this value to avoid signal compression or clipping. With a 35-dB RF front-end gain, G_{RX} provided by the band-select filter, LNA and mixer, the -70 dBm (-83 dBV_{rms}) desired channel at the antenna input can be amplified up to -48 dBV_{rms} which is 18 dB below the maximum signal level at the ADC input, defined as DR_{res}. To meet the bit error rate (BER) specifications, a minimum 10.5 dB SNR is required at the digital demodulator input. Moreover, a 10 dB additional noise margin is added to avoid ADC noise floor impacting the overall noise figure of the receiver. Therefore, the ADC noise floor is set at -68.5 dBV_{rms} while the required ADC DR is 59.5 dB.

To account for gain variability of the RF chain (i.e., high-Q LC loads), the ADC must be able to cope with the worst case of a higher than expected RF gain. Since

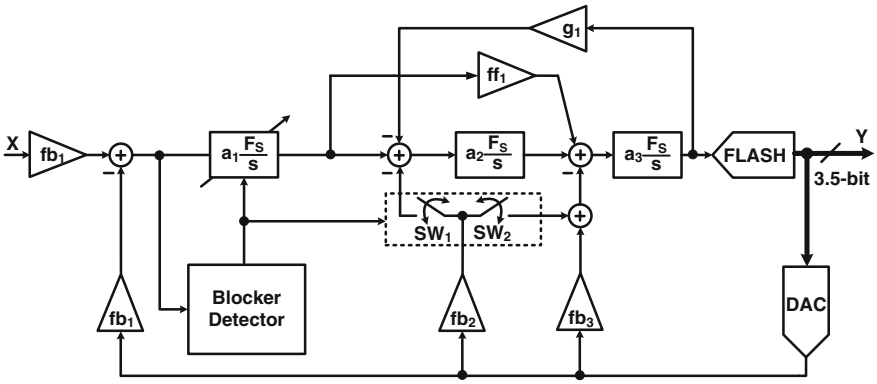

Fig. 2.22 Architecture of the proposed ΣΔ ADC

no filtering performance is also assumed for the RF front-end, a 10 dB additional margin is taken into account in the IIP3 requirement for the ADC. This yields the ADC IIP3 specification of 7.25 dBm.

2.6.2 Proposed ΣΔ ADC Architecture

Figure 22 shows the architecture of the proposed ΣΔ ADC, which consists of the reconfigurable loop filter and blocker detector. When blockers are weak or absent at the ADC input, the ADC operates in normal mode and switch SW_1 is open and SW_2 closed. In this mode the modulator shows a combination of feedforward and feedback stabilized loops.[17] By using the feedforward path ff_1, the first integrator's output swing can be reduced and thus its integrator coefficient can be increased. This results in reduction of overall power consumption since non-idealities of the second and third integrators due to reduced bias currents can be tolerated by the high coefficient of the first integrator. In addition, this architecture can achieve good anti-aliasing performance due to the feedback path. However, in the presence of strong blockers, the gain peaking in the STF at the adjacent channel frequency would produce a higher noise floor or lead to system instability.

In order to protect the ADC from overloading, the blocker detector reconfigures architecture by closing SW_1, opening SW_2 and reducing the first integrator coefficient a_1 by 50 %. The feedback path to the first integrator output removes the gain peaking, while the reduction of a_1 increases blocker suppression strength at the expense of reduced quantization noise shaping.

[17] Muñoz, F., Philips, K., Torralba, A.: A 4.7 mW 89.5 dB DR CT complex ADC with built-in LPF. In: IEEE ISSCC Digital Technical Papers, pp. 500–501 (2005)

2.6.3 Loop Filter and Feedback Path Design

In the normal operation mode, the loop filter $LF_{NOR}(s)$ and feedforward filter $FF_{NOR}(s)$ transfer functions are given by:

$$\begin{aligned} LF_{NOR}(s) &= \frac{a_3(fb_2+fb_3)F_S s^2 + a_1a_3fb_1ff_1F_S^2 s + a_1a_2a_3fb_1F_S^3}{s^3 + a_2a_3g_1F_S^2 s}, \\ FF_{NOR}(s) &= \frac{a_1a_3fb_1ff_1F_S^2 s + a_1a_2a_3fb_1F_S^3}{s^3 + a_2a_3g_1F_S^2 s}, \end{aligned} \tag{2.14}$$

where F_S is the sampling frequency. In the blocker suppression mode, the same transfer functions are calculated as

$$\begin{aligned} LF_{BLK}(s) &= \frac{a_3fb_3F_S s^2 + (0.5a_1a_3fb_1ff_1 + a_2a_3fb_2)F_S^2 s + 0.5a_1a_2a_3fb_1F_S^3}{s^3 + a_2a_3g_1F_S^2 s}, \\ FF_{BLK}(s) &= \frac{0.5\left(a_1a_3fb_1ff_1F_S^2 s + a_1a_2a_3fb_1F_S^3\right)}{s^3 + a_2a_3g_1F_S^2 s} \end{aligned} \tag{2.15}$$

The STF can be calculated by $FF(s)/1 + LF(s)$ and NTF can be calculated by $1/1 + LF(s)$. Figure 2.23 shows the simulated STF and NTF of the normal and blocker suppression modes. The signal bandwidth is set to 10 MHz and the sampling frequency is set to 250 MHz. The normal mode can achieve better SNDR performance with better noise shaping than the blocker suppression mode when blockers are weak, but it would show lower SNDR and poor stability under strong blocker conditions. On the other hand, the blocker suppression mode has an enhanced blocker suppression performance, with 8 dB attenuation at the adjacent

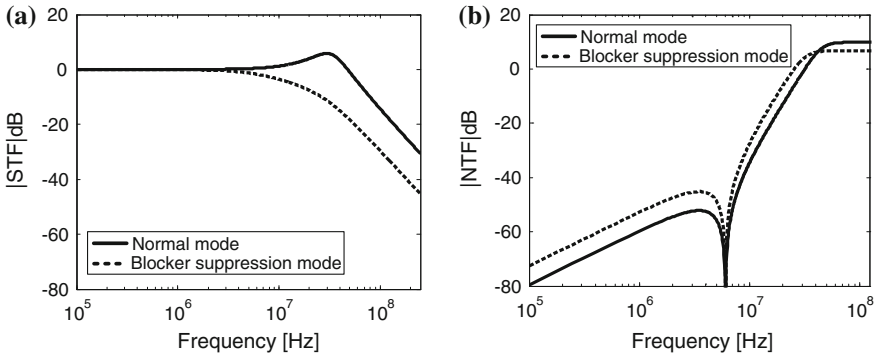

Fig. 2.23 ΣΔ ADC **a** STF and **b** NTF of the normal and blocker suppression mode

channel and 15 dB attenuation at the alternate channel. The drawbacks of this mode are reduced noise shaping and band-edge droop.

In the normal mode, increasing feedforward coefficient ff_1 can also reduce the gain peaking. However, it increases the −3 dB frequency of the STF and reduces the system stability because of increased high-frequency gain of the NTF. Thus an additional feedback path to the first integrator output is necessary.

2.6.4 Behavioral Simulations

Complex mixed-signal circuit design is often time-consuming and accompanies algorithmic iterative processes. Behavioral modeling and simulations can reduce

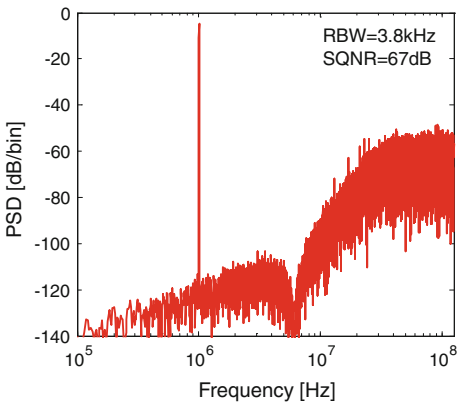

Fig. 2.24 Output PSD of the ADC with ideal blocks for an input signal 3 dB below full scale at 1 MHz

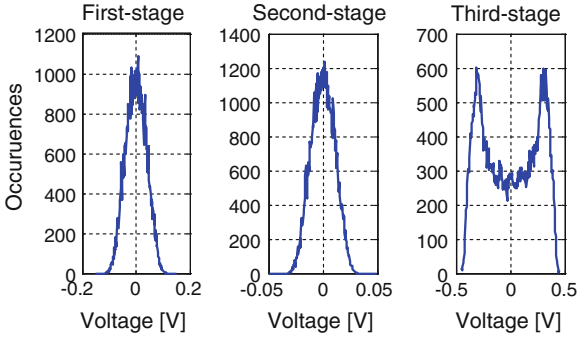

Fig. 2.25 Histograms of each integrator's output

such long design process and give initial specifications of circuit blocks for transistor level design.

Figure 2.24 shows the simulated output power spectrum density (PSD) of the ideal model and 67 dB SQNR is achieved. Figure 2.25 shows the simulated histograms of each integrator's output. From this simulation, a requirement of each integrator output swing can be estimated. The first stage integrator should have at least a 0.35 V_{pk-pk} output swing range to avoid signal clipping and a 0.1 V_{pk-pk} swing range is required for the second stage. Finally, the third stage must have a 1 V_{pk-pk} output swing range.

2.7 Behavioral Simulations with Non-idealities

2.7.1 Finite DC Gain and GBW in an OP-Amp

The finite DC gain and GBW of an op-amp creates an integrator coefficient's error and an additional pole which degrades performance of a modulator. To determine the minimum requirements for both parameters, iterative simulations with behavioral models can be performed.

The integrator transfer function with a finite DC gain and GBW can be shown as:

$$I_i(s) = \frac{k_i f_s}{s\left(1+\frac{1}{A(s)}\right)+\frac{1}{A(s)}\sum_{l=1}^{n} k_l f_s} = \frac{1}{1+\frac{s}{k_i f_s}} \cdot \frac{A(s)}{1+A(s)\beta(s)}, \tag{2.16}$$

where $\beta(s)$ is given by

$$\beta(s) = \frac{\frac{s}{k_i f_s}+\frac{1}{A(s)}\frac{\sum_{i} k_{l,l\neq i}}{k_i}}{1+\frac{s}{k_i f_s}} \tag{2.17}$$

Therefore the integrator with the finite gain and bandwidth can be modeled as shown in Fig. 2.26.

Figure 2.27 shows the simulated SQNR of the ADC with various open-loop DC gains and GBWs of the amplifier for each operation mode. With an ideal amplifier, the modulator has about 74 dB and 67 dB SQNR for the normal and blocker suppression mode, respectively. The SQNR starts decreasing, when the gain becomes lower than 40 dB and the GBW becomes lower than 1 GHz. Thus, the amplifier should have at least a 40 dB open-loop DC gain and 1 GHz GBW.

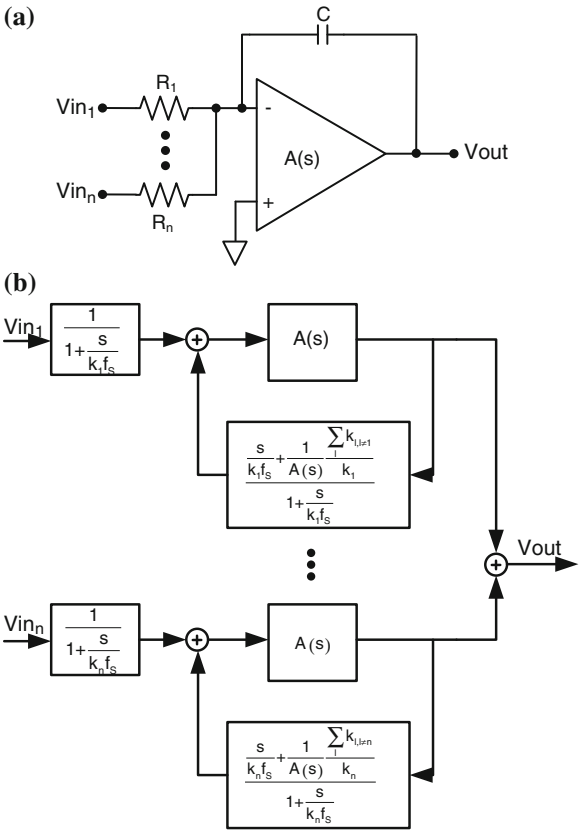

Fig. 2.26 **a** *n*-input active-RC integrator schematic and **b** its behavioral model

2.7.2 OP-Amp's Finite DC Gain for Blocker Detection

In an active-RC integrator with finite GBW OTAs, virtual ground at the OTA inputs degrades with the inverse of the amplifier AC response, providing a cost effective HPF performance to detect blockers.[18] Figure 2.28a shows a simple first-order CT ΣΔ ADC. With a linear quantizer model, the signal path shows LPF characteristic while a HPF characteristic results at the virtual ground node V_X due to a finite GBW of the OTA. The resulted HPF and STF equations are given by

$$HPF(s) = \frac{V_X(s)}{V_{IN}(s)} \approx \frac{\omega_1(s+\omega_c)}{s^2 + \omega_c A_{DC} s + \omega_1 \omega_c A_{DC}}$$

[18] Yoshizawa, A., Tsividis, Y.: A channel-select filter with agile blocker detection and adaptive power dissipation. IEEE J. Solid-State Circuits **42**(5), 1090–1099 (2007)

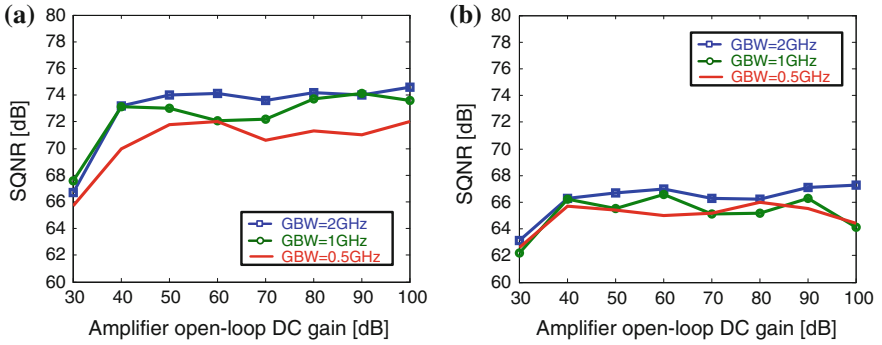

Fig. 2.27 Simulated SQNR of the proposed ADC with various open-loop DC gains and GBWs of the amplifiers for **a** the normal mode and **b** blocker suppression mode

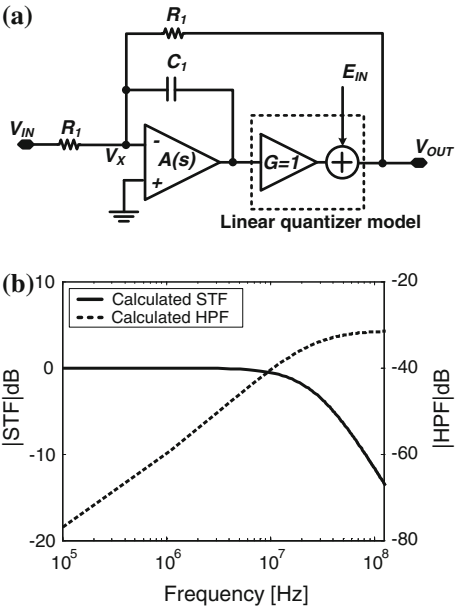

Fig. 2.28 **a** First-order CT ΣΔ ADC with a linear quantizer model **b** STF and HPF of the first-order CT ΣΔ ADC

$$STF(s) = \frac{V_{OUT}(s)}{V_{IN}(s)} \approx \frac{\omega_1 \omega_c A_{DC}}{s^2 + \omega_c A_{DC} s + \omega_1 \omega_c A_{DC}}$$

where A_{DC} and ω_c are the open-loop DC gain and -3 dB frequency of the op-amp, respectively and $\omega_1 = 1/R_1 C_1$ Fig. 2.28b shows the calculated STF and HPF when $A_{DC} = 75$ dB, ω_c=100 kHz, $R_1 = 1.5$ kΩ, and $C_1 = 4$ pF.

If the second and third integrators are assumed as ideal, the HPF characteristic of the proposed ΣΔ ADC in normal mode can be expressed as:

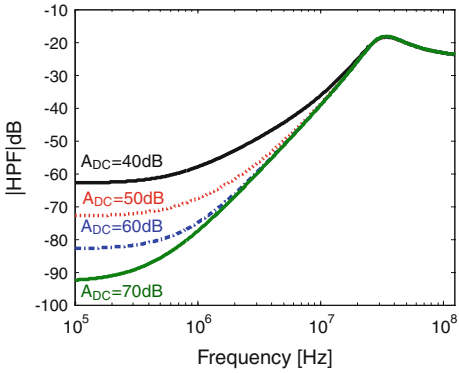

Fig. 2.29 Calculated HPF characteristic with various open-loop DC gains of the first op-amp

$$HPF(s) = \frac{1 + H_2(s)}{H_1(s)A_1(s) +_s C_1R_1[1 + A_1(S)][1 + H_2(s)] + 2H_2(s) + 2} \tag{2.18}$$

where $A_1(s)$ is the open-loop transfer function of the first op-amp. $H_1(s)$ is the transfer function from the first integrator output to the quantizer input in Fig. 2.22. $H_2(s)$ is the loop filter transfer function when the feedback path fb_1 is set to zero.

The transfer functions are given by:

$$\begin{aligned} H_1(s) &= \frac{a_3 ff_1 F_s S + a_2 a_3 F_s^2}{s^2 + a_2 a_3 g_1 F_s^2}, \\ H_2(s) &= \frac{a_3(fb_2 + fb_3)F_s^s}{s^2 + a_2 a_3 g_1 F_s^2} \end{aligned} \tag{2.19}$$

Figure 2.29 shows the HPF of the proposed ΣΔ ADC with various open-loop DC gains of the first stage op-amp when the amplifier has 1 GHz of GBW. The HPF has the corner frequency at 20 MHz and the gain peaking at adjacent channel frequency. For SQNR performance, 40 dB of DC gain is enough but in order to detect interferers at adjacent and alternate channel frequencies of WiMAX standard while suppressing the desired channel signals, additional DC gain is necessary. Thus, 60 dB of DC gain is set for the specification. This additional gain would also reduce the input referred thermal noise and non-linearity contributions from the second and third stage integrator and the quantizer.

2.7.3 Device Noise

In most of state-of-the-art ADCs, achievable DR is usually limited by device noise. Consequently, effort to reduce the device should be accompanied during design process with minimum power consumption. In CT ΔΣ ADCs, the input referred device noise primarily originates from the first stage integrator and feedback DAC. In order to achieve a 60 dB DR over a 10 MHz bandwidth with the 1 V_{pk-pk}

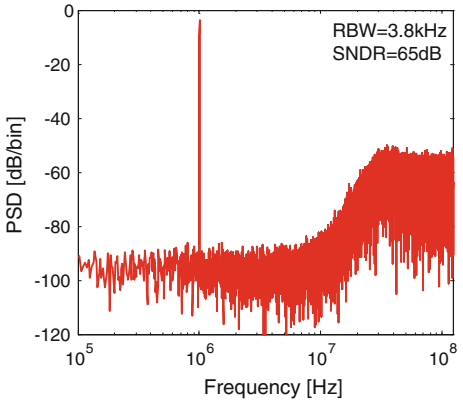

Fig. 2.30 Simulated output PSD for an input signal 3 dB below full scale at 1 MHz with 60 dB DC gain and 1 GHz GBW of the op-amps, and 56 nV/$\sqrt{\text{Hz}}$device input referred noise

differential FS range, the input referred noise density should be lower than 56 nV/$\sqrt{\text{Hz}}$. In reality the thermal noise will add to the quantization noise floor due to op-amp's finite DC gain and GBW.[19] Consequently, the ADC behavioral model must be simulated with equivalent device noise sources, to obtain a more accurate estimation of the DR. Figure 2.30 shows the simulated power spectrum density (PSD) of the modulator operating in the blocker suppression mode with 60 dB DC gain and 1 GHz GBW of the op-amps, and 56 nV/$\sqrt{\text{Hz}}$ device input referred noise. The modulator can achieve 65 dB SNDR which is 5 dB greater than the DR requirement.

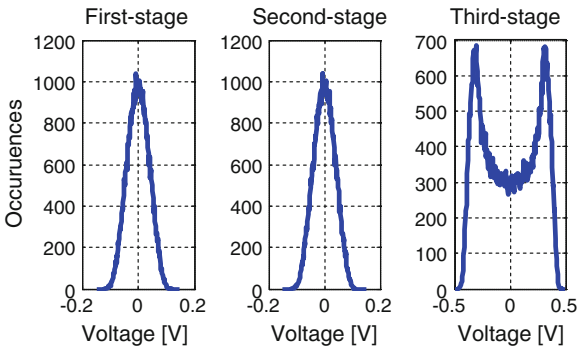

Fig. 2.31 Histograms of the integrators' output of the proposed modulator

[19] Park, M.: A fourth-order continuous-time ΣΔ ADC with VCO-based integrator and quantizer. Ph.D. dissertation, Massachusetts Institute Technology, Cambridge (2009)

2.7.4 Integrator Output Swing

In active-RC integrators, nonlinearity is usually determined by integrators' output swing range. Thus, loop filter architecture should be properly determined or integrators should have an enough output swing range. To specify the required output swing range, behavioral simulations can be performed. Figure 2.31 shows the histograms of the integrators' output of the proposed ΣΔ ADC. The first and second stage integrator should have at least 0.35 V_{pk-pk} output swing range to avoid signal clipping. The third stage must have 1 V_{pk-pk} output swing range. The requirement of the second and third stage can be reduced because nonlinearities caused by these stages would be reduced by the first stage integrator. Here, all signal swing range is differential.

2.7.5 DAC Mismatch

In a multi-bit ΣΔ modulator, a modulator's nonlinearity originates from mismatches in the first stage feedback DAC. To estimate system performance versus the DAC mismatch, the unit current of the multi-bit DAC i_{DAC}, can be modeled as:

$$i_{DAC} = i_{nom} + i_{error} \tag{2.20}$$

where i_{nom} is the nominal value of the unit current and i_{error} represents the mismatch between unit current elements, which is a Gaussian distributed random number. SNDR performance of the proposed modulator with DAC mismatch can be investigated by using the above model and Fig. 2.32 shows the behavioral simulation result with different standard deviations of the error when the modulator is operating in the blocker suppression mode. To meet the 60 dB DR requirement, the standard deviation should be lower than 0.4 %. This condition can be easily satisfied by employing a self-current calibration technique.[20]

2.7.6 Clock Jitter

Unlike DT ΣΔ modulators, CT counterparts are very sensitive to sampling clock uncertainties, called clock jitter. Clock jitter adds random noise to a loop filter of the modulator and increases noise floor. Additive error sequence due to the clock jitter can be expressed as[21]

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[20] Groeneveld, D.W.J. et al.: A self-calibration technique for monolithic high resolution D/A converters. IEEE J. Solid-State Circuits **24**(6), 1517–1522 (1989)

[21] Hernandez, L. et al.: Modeling and optimization of low pass continuous-time sigma-delta modulators for clock jitter noise reduction. ISCAS, pp. 1072–1075 (2004)

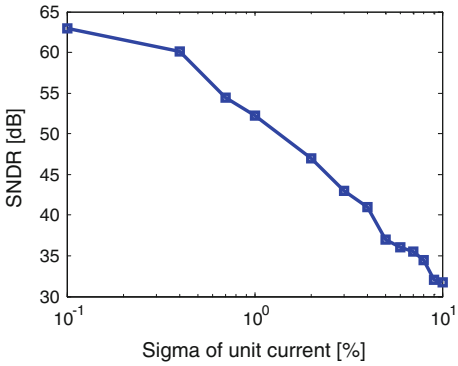

Fig. 2.32 SNDR versus DAC unit current mismatch

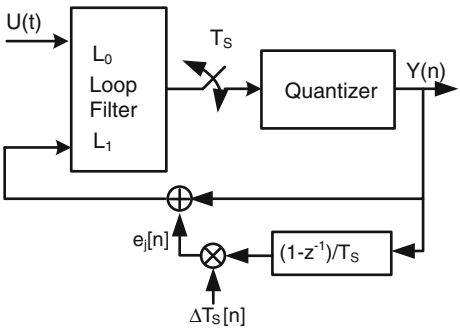

Fig. 2.33 CT ΣΔ ADC model with additive clock jitter

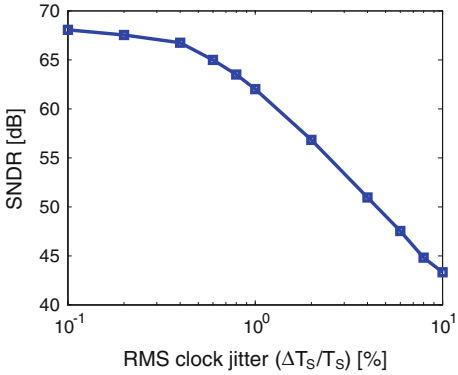

Fig. 2.34 SNDR versus RMS clock jitter

$$e_j[n] = (y[n] - y[n-1])\frac{\Delta T_s[n]}{T_s}, \tag{2.21}$$

where T_S is a clock period and ΔT_S represents clock uncertainty. From Eq. (2.21), a CT ΣΔ modulator with clock jitter can be modeled as shown in Fig. 2.33. The modulator is simulated with different amount of clock jitter and the result is shown

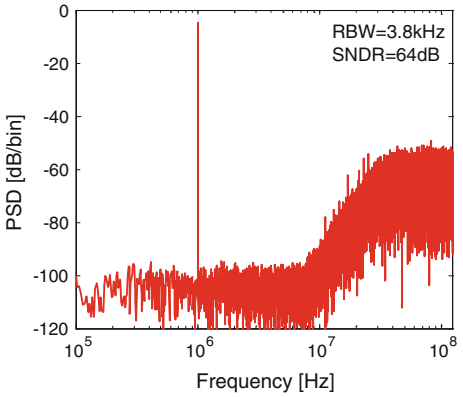

Fig. 2.35 Simulated output PSD for an input signal 3 dB below full scale at 1 MHz with 60 dB DC gain and 1 GHz GBW of the op-amps, 56 nV/$\sqrt{\text{Hz}}$ device input referred noise, and 16 ps RMS clock jitter

in Fig. 2.34. To achieve 66 dB DR, the RMS clock jitter should be less than 0.4 % respect to T_S (16 ps). The ADC is also simulated with non-idealities defined previously and the simulated PSD of the ADC output is shown in Fig. 2.35. With all non-idealities defined in this chapter, the modulator can achieve 64 dB DR.

2.7.7 Simulations with a 24 Mbps 16-QAM Signal

To investigate feasibility of the blocker-adaptive ΣΔ ADC for WiMAX applications, the modulator needs to be tested with a modulated input signal specified in the standard. Figure 2.36 shows the test setup for this behavioral simulation. A 24 Mbps 16-QAM signal with OFDM is generated by using MATLAB Communications toolbox and the desired channel and interferer powers are set as specified by the standard. Also the RF front-end gain, G_{RX}, is placed between the

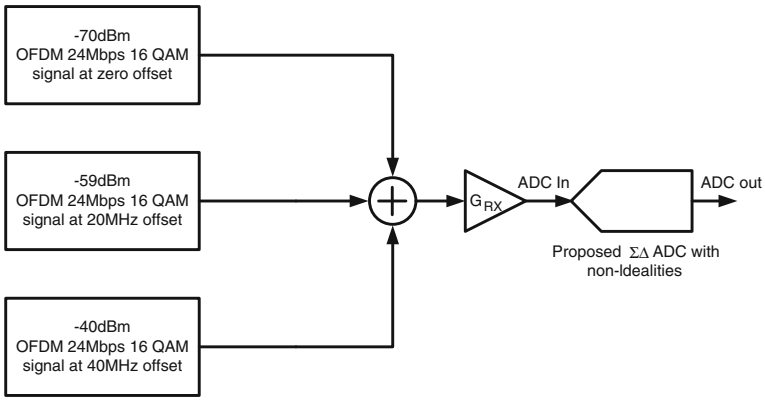

Fig. 2.36 Behavioral simulation test set-up with 24 Mbps 16-QAM WiMAX signals

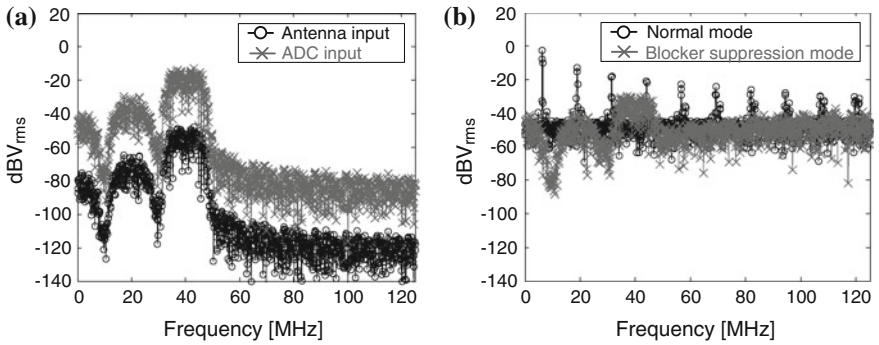

Fig. 2.37 Simulated PSDs of 16-QAM WiMAX signals at **a** the antenna and ADC inputs and **b** ADC output

Table 2.2 Summary of specifications of the proposed ADC

Process	130 nm digital CMOS process
VDD	1.2 V
FS	1 V_{pk-pk} differential
DR	60 dB
IIP3	7.25 dBm

ADC and the WiMAX signal generator. Furthermore, all the previously defined non-idealities are accounted for in the ADC model.

Figure 2.37 shows the PSDs at the antenna and ADC inputs and ADC output for the normal mode and blocker suppression mode. With 35 dB RF front-end gain, the ADC faces strong interferers which are -37 dBV_{rms} and -18 dBV_{rms} at the adjacent channel and alternate channel, respectively. In the normal mode, the 5 dB gain peaking in the adjacent and alternate channel leads to ADC instability. On the other hand, with 8 dB and 15 dB attenuation at those frequencies the ADC remains functional with good performance in the blocker suppression mode. As discussed above, to account for non-idealities of the proposed modulator such as finite DC gain and GBW of op-amps, DAC nonlinearities, integrators' output swing, clock jitter, and device noise, several behavioral modeling methods are introduced. Also, with iterative behavioral simulations, the circuit parameters are determined and they are summarized in Table 2.2. Corresponding ADC parameters are summarized in Table 2.3.

2.8 Implementation of the Blocker Adaptive ΣΔ ADC

Figure 2.38 shows the schematic of the proposed adaptive blocker rejection ΣΔ ADC. It can be divided into four blocks: the 3rd-order reconfigurable loop filter,

Table 2.3 Summary of specifications of the proposed ADC and circuit building blocks

Process	130 nm digital CMOS process
ADC specifications	
VDD	1.2 V
FS	1 V_{pk-pk} differential
DR	60 dB
IIP3	7.25 dBm
Circuits' specifications	
Op-amp DC gain	60 dB
Op-amp GBW	1 GHz
1st/2nd/3rd stage integrator output swing (differential)	0.35/0.35/1 V_{pk-pk}
Device input referred noise	56 nV/$\sqrt{\text{Hz}}$
DAC mismatch	0.4 % (standard deviation)
Clock Jitter	16 ps

quantizer, feedback path DACs, and blocker detector. For high linearity, active-RC integrators are used to implement to the loop filter. A 13-level flash ADC is used for quantizer to improve system stability and DR. For high-speed operation (250 MHz), current steering DACs are employed. Excess loop delay caused by the quantizer and DACs is compensated by the digital differentiator in the feedback path, to avoid an additional summing amplifier or a return-to-zero DAC, which would require extra power.[22] DAC2 is re-used for both operating modes, thus no extra die area is required to implement the adaptive architecture.

2.8.1 Loop Filter Design

The 3rd-order reconfigurable loop filter is designed with active-RC integrators due to their high linearity and well-defined common mode voltage. The reconfigurability can be performed by closing or opening switches SW1 s and SW2 s. The main drawback of the active-RC integrators is RC time constant variation which is up to ±40 %.[23,24] To compensate for these variations, manually controlled binary-weighted tunable capacitor arrays are employed as shown in Fig. 2.39. For the 1st and 2nd stage integrator, the main capacitor, C_{MAIN}, is set to 2.6 and a 0.2 pF of

[22] Mitteregger, G. et al.: A 20-mW 640-MHz CMOS continuous-time ADC with 20-MHz signal bandwidth, 80-dB dynamic range and 12-bit ENOB. IEEE J. Solid-State Circuits **41**(12), 2641–2649 (2006)

[23] Kappes, M.S., Jensen, H., Gloerstad, T.: A versatile 1.75 mW CMOS continuous-time delta-sigma ADC with 75 dB dynamic range for wireless applications. In: Proceedings European Solid State Circuits Conference pp. 279–282 (2002)

[24] Giandomenico, A.D. et al.: A 15 MHz bandwidth sigma-delta ADC with 11 bits of resolution in 0.13 m CMOS. In: Proceedings European Solid State Circuits Conference, pp. 233–236 (2003)

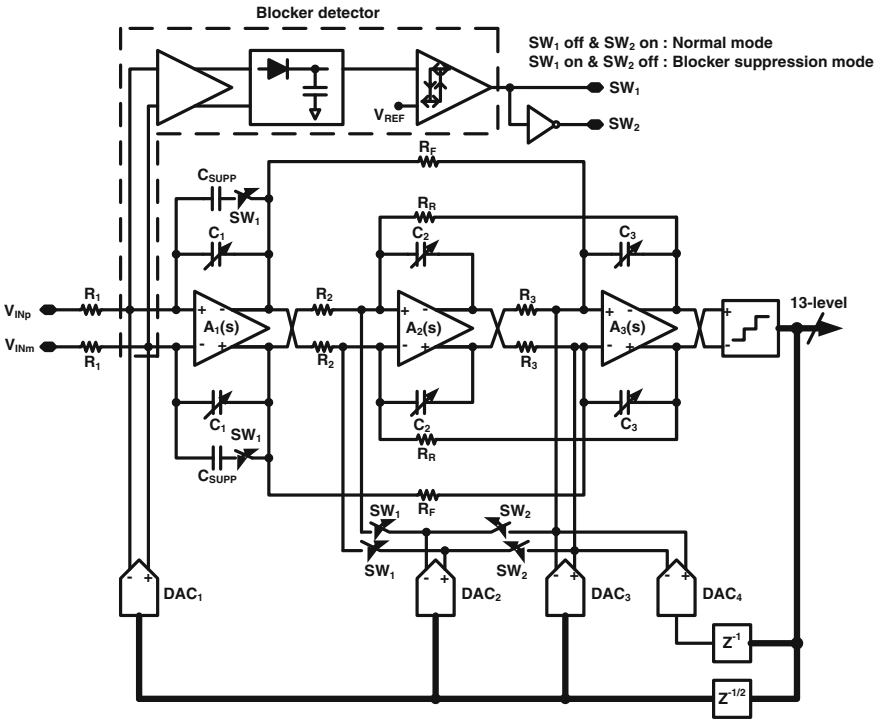

Fig. 2.38 Schematic of the proposed ΣΔ ADC

the least significant bit (LSB) capacitor, C_{LSB}, is employed. This configuration gives a tuning range of from 2.6 to 5.6 pF with 5 % accuracy.

Figure 2.39a shows the schematic of the OTA used for the first active-RC integrator which sets the performance of the overall modulator. Since the required differential output swing range is just 0.35 V_{pk-pk}, a power efficient telescopic cascode amplifier with gain boosting can be used.[25] The gain-boosting amplifiers are single-ended cascade common source amplifiers while the OTA's tail current source is biased in triode region to increase the output voltage swing.

Figure 2.41 shows the simulated open-loop frequency response of the first stage OTA. The OTA has 75 dB of open-loop DC gain and 1-GHz GBW with 4 pF load capacitance while consuming 3 mA quiescent current and achieves 70° phase margin. Although a low output impedance output stage is preferred to drive resistive loads, with a 40 kΩ load, the OTA gain is reduced by only 10 dB (red dashed line in Fig. 2.41), and thus the output stage was not adopted to save power.

[25] Christen, T., Burger, T., Huang, Q.: A 0.13 m CMOS EDGE/UMTS/WLAN tri-mode ADC with −92 dB THD. In: IEEE ISSCC Digital Technical Papers, pp. 240–241 (2007)

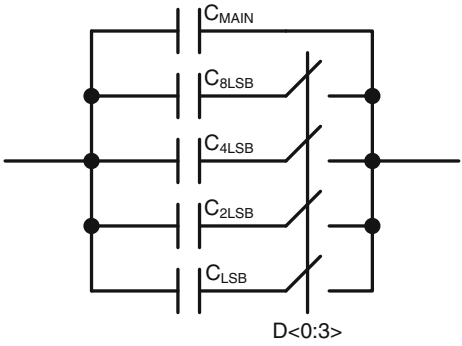

Fig. 2.39 Binary weighted tunable capacitor array

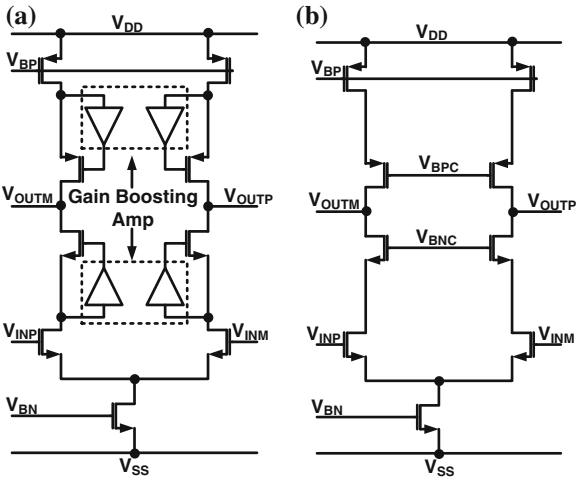

Fig. 2.40 Schematic of **a** the first stage and **b** following stages' OTA

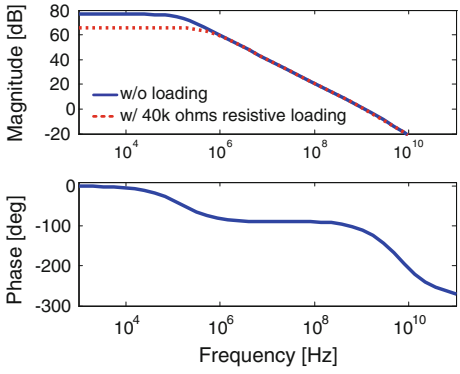

Fig. 2.41 Simulated open-loop frequency response of the first stage OTA

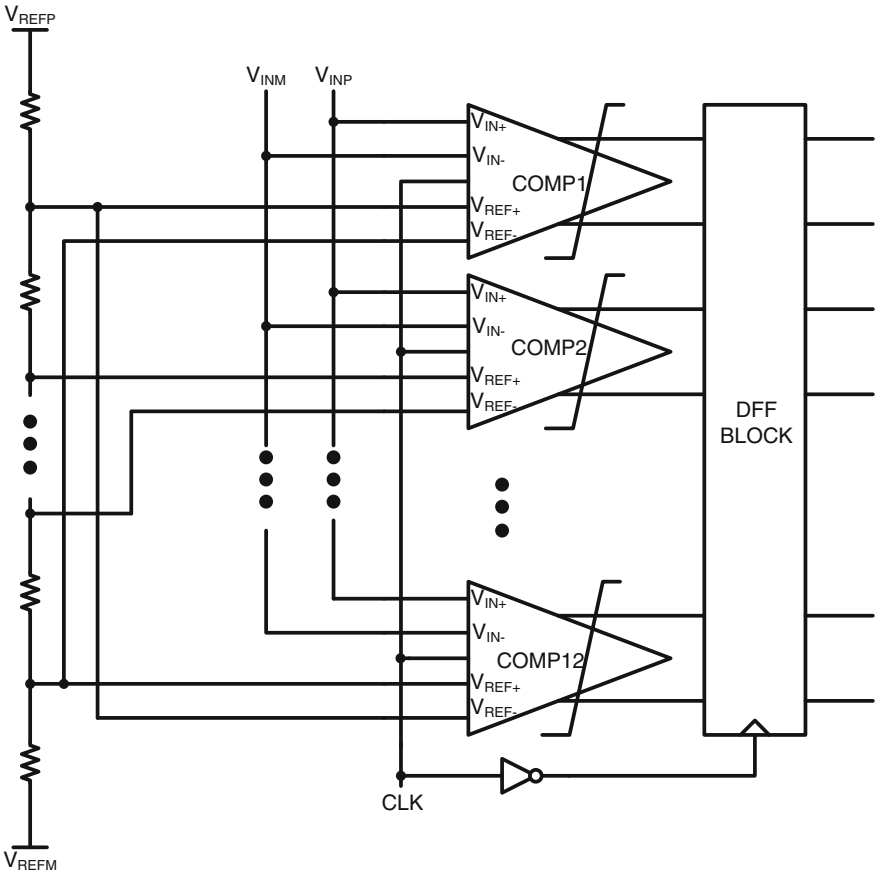

Fig. 2.42 Schematic of the quantizer

Once blockers, as specified, are detected, the ADC operates in the blocker suppression mode and the blockers would be suppressed. Thus, the feedback path would carry attenuated blockers, and the OTA input nodes of the first active-RC integrator can maintain a good virtual ground. Overall ADC loop-gain would help stabilize the first integrator virtual ground. Consequently, an additional linearity requirement is unnecessary for the input transistors in the OTA.

The schematic of the OTAs used in the remaining loop filter is shown in Fig. 2.40b. Because noise and distortion contributions of the second and third stages are reduced by the preceding gain stage, the gain boosting amplifiers are removed and the bias currents are scaled down by a factor of 2.

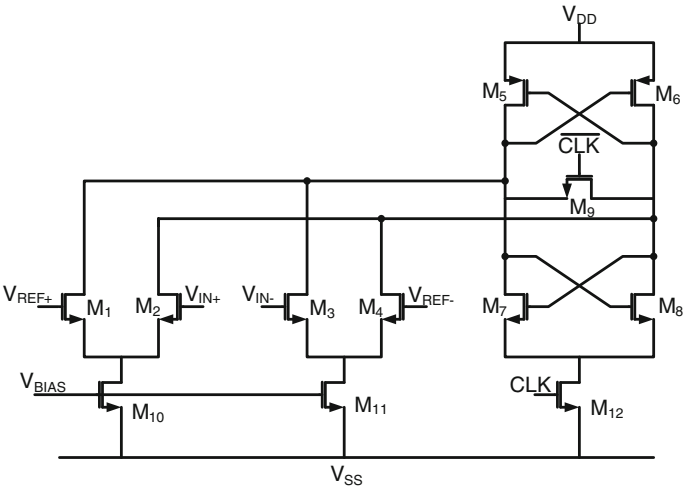

Fig. 2.43 Schematic of the comparator

2.8.2 Quantizer

For the Quantizer, the 13-level flash ADC is employed and its schematic is shown in Fig. 2.42. For reference generation, a resistor ladder is used and fully differential comparators are employed. The D flip-flop block is placed after the comparator to fix the large excess loop delay and this delay is compensated for by digital differentiator technique.

For comparators, a latched comparator with a preamplifier is designed and its schematic is shown in Fig. 2.43.[26] The preamplifier is added to reduce metastability and kick-back noise. Since the quantizer is the least critical block, the comparators are designed for low-power consumption.

Fifty Monte-Carlo simulations are performed to estimate input referred offset voltage of the comparator. Figure 2.44 shows the histograms of the input referred offset voltage. The mean value of the offset is 20 mV and the standard deviation is 10 mV. Since the LSB of the quantizer is about 83 mV, the offset voltage is well below a third of the LSB. Moreover, it is attenuated by the gain of the loop filter when it is referred to the ADC input and thus the ADC performance would not be degraded by the quantizer offset voltage.

[26] Razavi, B.: Principles of Data Conversion Systems Design. IEEE Press, Piscataway (1995)

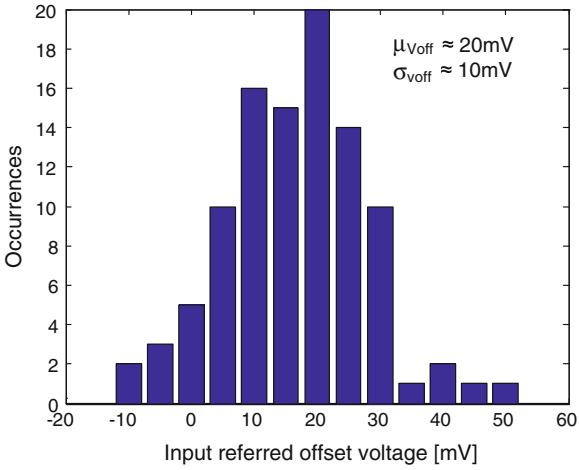

Fig. 2.44 Histograms of simulated input referred offset voltage obtained from 100 Monte-Carlo simulations

2.8.3 Feedback DAC

Figure 2.45a shows the schematic of a conventional current steering DAC unit cell. There are several critical design issues associated with feedback DAC design; nonlinear output impedance, glitch energy caused by clock feedthrough due to parasitic capacitor C_{gd} and voltage fluctuations at the source node of the switch transistors M_1 and M_2, resulting from charging and discharging the parasitic capacitor C_p. The first stage DAC should minimize these problems, since all of these non-idealities translate to the output without any noise shaping.

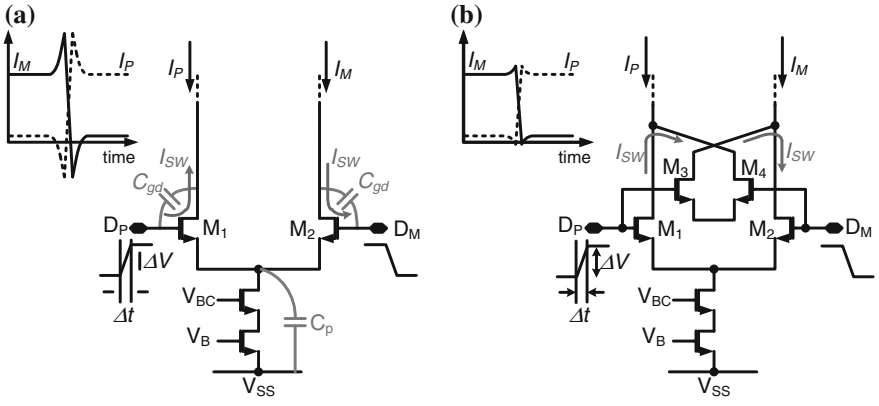

Fig. 2.45 Schematic of **a** conventional and **b** the proposed current steering DACs

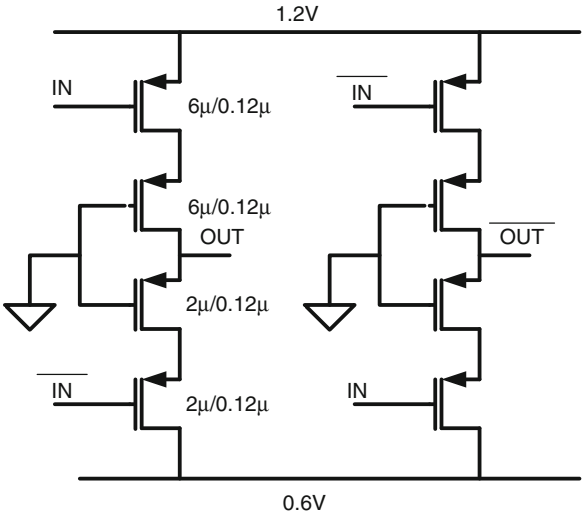

Fig. 2.46 Low-swing, high-cross over signal generation for current steering DACs

Figure 2.46 shows a reduced-swing and high-crossover DAC driver. It can reduce glitch energy by guaranteeing either one of the DAC switches closed and minimize clock feedthrough effects with reduced swing.[27] In addition, it can increase the output impedance by operating M_1 and M_2 in the saturation region, reducing nonlinearity of the output impedance.

The switching current I_{SW} generated by clock feedthrough is given by:

$$I_{SW} = \frac{dQ_{c_{gd}}}{dt} = C_{gd}\frac{dv}{dt}, \tag{5.1}$$

where dV and dt are the amplitude and transition time of the switch control signals, D_p and D_m. In high-speed applications, the clock feedthrough effects would be more prominent and degrade SNDR performance. To further reduce clock feedthrough effects, the current steering DAC unit cell employs two additional cross-coupled transistors, M_3 and M_4, as shown in Fig. 2.45b. If M_3 and M_4 have the same size of M_1 and M_2, the switching currents through the C_{gd} of M_3 and M_4 cancel the current injection of the main transistor pair, further minimizing spikes.

Figure 2.47 shows the block diagram configuration of the current steering DAC chain. It consists of a retiming flip-flop to synchronize with other DAC cells, a reduced-swing high-crossover driver stage, and the proposed current steering DAC cell. Figure 2.48 shows the transistor-level simulation of the unit current DAC cell with this configuration.

[27] Wu, T.-Y. et al.: A low glitch 10-bit 75-MHz CMOS video D/A converter. IEEE J. Solid-State Circuits **30**, 68–72 (1995)

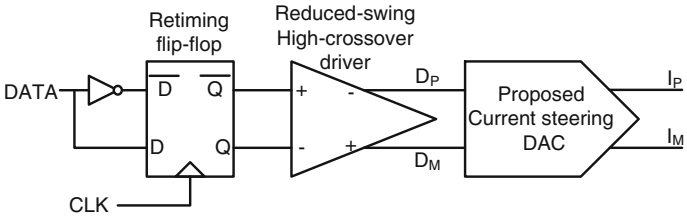

Fig. 2.47 Current steering DAC with the driver and retiming block

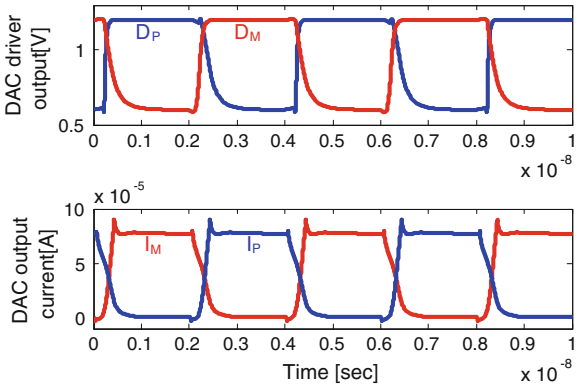

Fig. 2.48 Transistor-level simulation of the unit current DAC cell and the DAC driver

2.8.4 Self-Calibration Technique

Unit cell mismatches in multi-bit DACs limit the overall ADC linearity. In order to maintain system linearity, the first DAC should have at least 11-bit linearity even though a 3.5-bit DAC is used. To improve the linearity, data weighted averaging (DWA) or self-current calibration techniques can be used. [28,29] In this design, the self-current calibration technique is employed instead of DWA because it does not add further excess loop delay. Figure 2.49 shows the schematic of the self-current calibration technique where the two cross-coupled transistors are not shown for simplicity. 95–97 % of the reference current I_{REF} is assigned to the coarse current source M_1, I_{COARSE}. During the calibration phase, M_4 and M_5 are open and M_6 and M_7 are closed so that the fine current source M_2 can compensate the difference between I_{REF} and I_{COARSE}. M_8 and M_9 are added to reduce charge injection caused by M_7. The parasitic capacitance C_{gs} of M_2 holds its bias voltage until the next calibration phase, and this current cell can generate the calibrated current I_{REF}

[28] Li, Z., Fiez, T.S.: A 14 bit continuous-time delta-sigma A/D modulator with 2.5 MHz signal bandwidth. IEEE J. Solid-State Circuits **42**(9), 1873–1883 (2007)

[29] Geerts, Y., Steyaert, M., Sansen, W.: Design of Multi-Bit Delta-Sigma A/D Converters. Kluwer Academic, Norwell (2002)

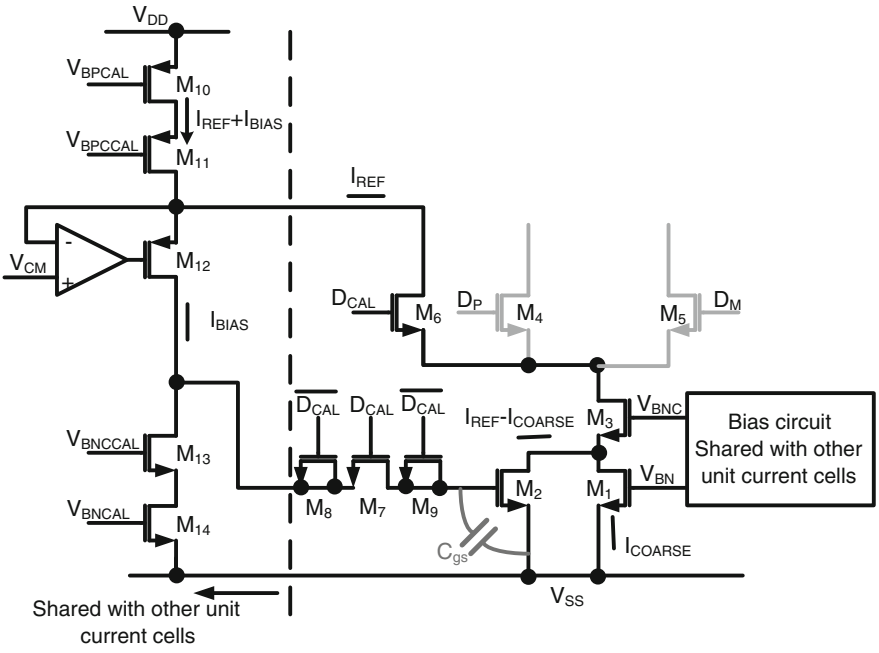

Fig. 2.49 Schematic of the self-current calibration technique

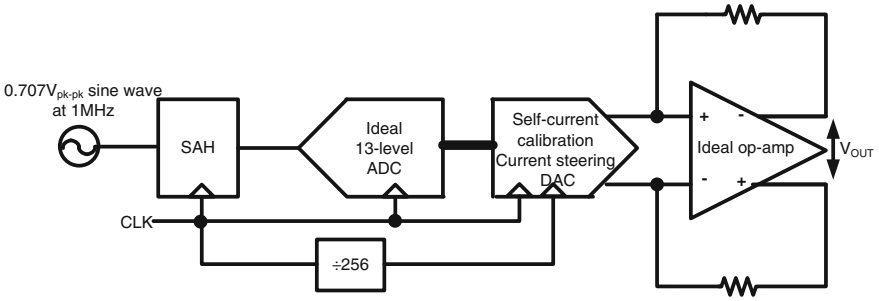

Fig. 2.50 Test setup for estimating performance of the self-current calibration DAC

during the normal operation phase. 1 μs is assigned to calibrate each unit current cell, and a total of 13 unit current cells are used for the first stage DAC. This rotational calibration is performed continuously at every 13 μs.

To estimate performance of the self-current calibration current steering DAC, the DAC which has 10 % of the unit current is driven by ideal ADC output and Fig. 2.50 shows the test setup. Figure 2.51 shows the simulated output PSD of the DAC when the self-current calibration is on and off. When the self-current calibration is off, the DAC has 30 dB of HD3 but when it is on, linearity of the DAC is improved significantly and the HD3 is not visible.

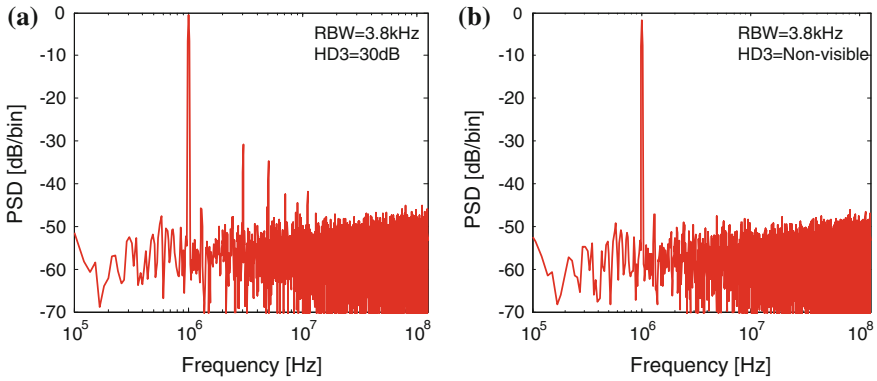

Fig. 2.51 Output PSD of the first stage DAC driven by the ideal 13-level flash ADC when self-current calibration is **a** on and **b** off

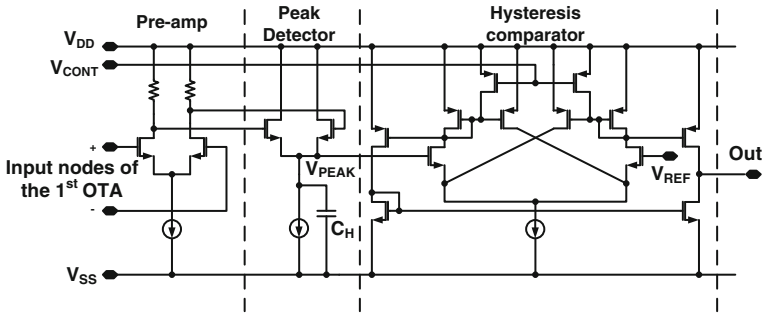

Fig. 2.52 Schematic of the blocker detector

Blocker Detector

A typical blocker detector employs a high-pass filter (HPF) followed by an amplitude detector. In this design, virtual ground at the first active-RC integrator's inputs is exploited to obtain a HPF characteristic.[18] Therefore power consumption and silicon area can be saved. To increase accuracy of blocker detection, low-noise pre-amplifier is added in front of the amplitude detector which is implemented by an NMOS-based rectifier. The detector output is compared with the hysteresis comparator and its output controls operation mode of the modulator.

Figure 2.52 shows the schematic of the blocker detector. It consists of a low-noise amplifier, peak detector and hysteretic comparator. A low-noise amplifier is added before the peak detector to increase detector accuracy. An NMOS rectifier and capacitor C_H achieves blocker peak detection. An important point to make is that quantization noise and tonal content at the quantizer output also undergoes the high-pass characteristic at the virtual ground nodes of the first integrator. Therefore, the hysteretic characteristic in level detection is required to avoid erroneous toggling of the comparator output due to quantization noise. The hysteresis level

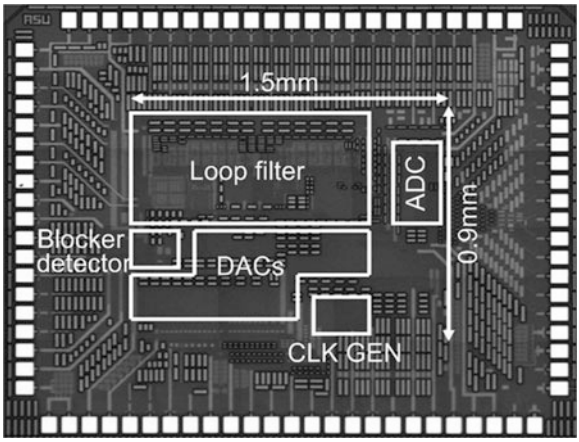

Fig. 2.53 Chip micrograph

and the accuracy of the blocker level detection are obtained through on transistor level simulations. When a −40 dBFS input signal is applied with a 20 dBc adjacent channel blocker, the ADC in the normal mode has lower SNDR than the blocker suppression mode. At this point, the peak detector generates V_{PEAK} of 700 mV, and this value is set as the threshold (V_{REF}) for changing between ADC modes. A ± 1 dB change in blocker power around its nominal value causes ±5 mV change in the peak detector output, setting the overall accuracy. A hysteresis level of 20 mV is determined to avoid false triggers due to quantization noise and tonal content. For testing purposes the hysteresis points are analog programmable through control voltage V_{CONT}.

A DC offset or low-frequency input signal could generate tonal content at high frequencies, and these tones can also cause erroneous toggling of the comparator output. From behavioral simulations, the worst case DC related tonal content is measured to be around −25 dBFS, which generates 600 mV V_{PEAK}. Since the hysteresis level is set at 700 mV, the worst case tonal content is safely below the trip threshold of the comparator.

2.8.5 Floor Plan and Layout

A floor plan and layout of the ADC must be carefully considered because performance of the ADC is strongly depends on routing of critical signal paths, noise coupling from digital sections to analog sections, and etc. Figure 2.16 shows the floor plan of the proposed ADC. The analog sections including the loop filter, the feedback DACs, and the blocker detector are separated from the digital sections consisting of the quantizer, the clock generator, the digital signal path for DAC control. For further isolation between the analog and digital sections, both sections are enclosed by double guard rings. Also power supply and ground for the analog sections are separated from ones for the digital sections to protect the sensitive

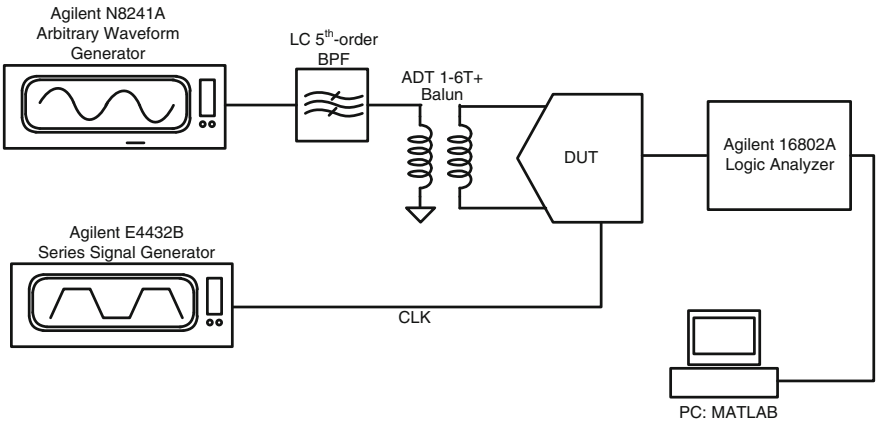

Fig. 2.54 Test setup for evaluation of the prototype ADC

analog building blocks from high speed switching current noise caused by the digital circuits. The proposed ΣΔ ADC is designed using 1.2 V 130 nm CMOS process which has 8 metal levels and MIM capacitors. The active occupies 1.5×0.9 mm^2 silicon area, as shown Fig. 2.53.

2.9 Measurement

2.9.1 Test Setup

Figure 2.54 shows the test setup used to evaluate the prototype ADC. A test input signal is generated by the arbitrary waveform generator (Agilent N8241A AWG)

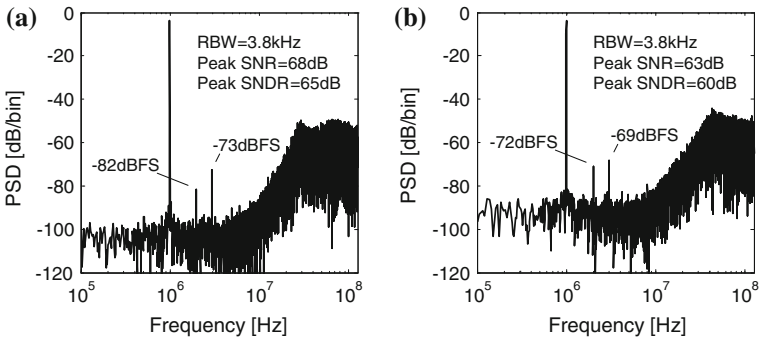

Fig. 2.55 Measured output PSD for an input signal 4 dB below full scale at 1 MHz for **a** the normal mode and **b** the blocker suppression mode

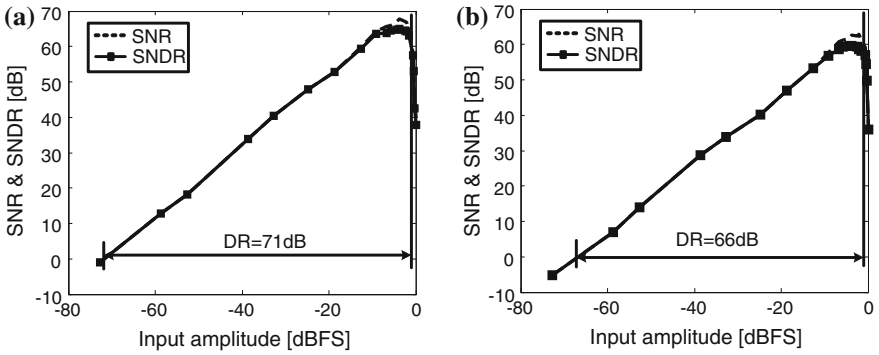

Fig. 2.56 Measured SNR and SNDR versus the normalized input signal amplitude for **a** the normal mode and **b** the blocker suppression mode

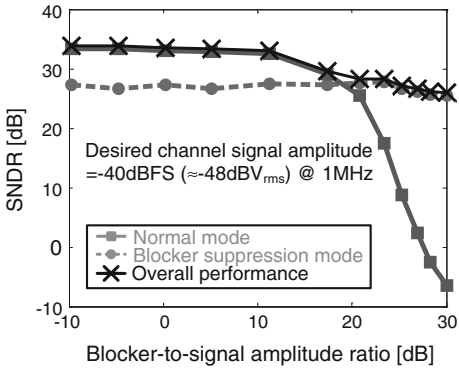

Fig. 2.57 Measured SNDR for the normal and blocker suppression mode at different blocker levels with −40 dBFS desired channel input signal

and it passes through the LC 5th-order BPF to suppress its harmonics. Then, the filter output signal is applied to the balun (ADT 1-6T+) for single to differential conversion. The differential input signal is fed to the prototype ADC, clocked by a 250 MHz pulse which is generated by clock generator (Agilent E4432B Series Signal Generator). The ADC's output is captured by the logic analyzer (Agilent 16802A Logic analyzer) and the captured data is downloaded to PC for post-processing.

2.9.2 Single-Tone Test

The proposed ΣΔ ADC is fabricated on a 1.2 V 130 nm CMOS technology, which features 8 metal levels and MIM capacitors. The die occupies a 1.5 × 0.9 mm^2 silicon area, as shown in Fig. 2.55.

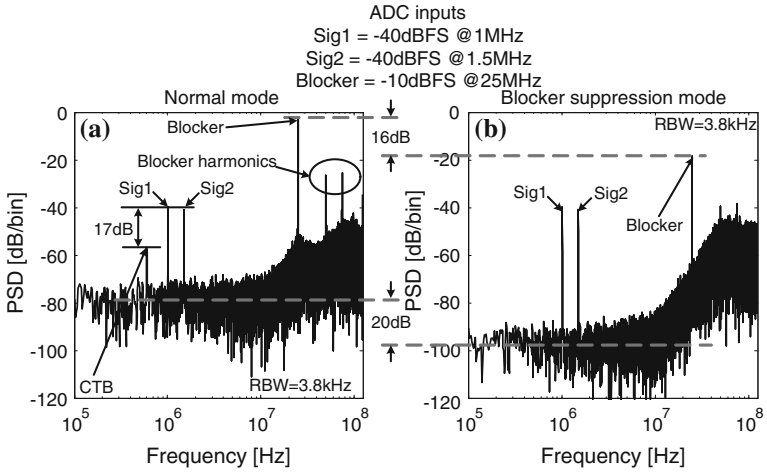

Fig. 2.58 Measured two-tone in-band tests with a 30 dBc extra adjacent channel blocker applied at the ADC input for **a** the normal mode and **b** the blocker suppression mode

Figure 2.56 shows the measured output PSD for an input signal −4 dB below full scale at 1 MHz for both operating modes. Figure 2.57 shows the measured SNR and SNDR versus the normalized input signal amplitude for both modes. Over a 10 MHz signal bandwidth, the ADC achieves 68 dB peak SNR, 65 dB peak SNDR, and 71 dB DR in the normal mode with 18 mW power consumption while the blocker suppression mode obtains 63 dB peak SNR, 60 dB peak SNDR, and 66 dB DR, consuming the same power. In Fig. 2.56, the raised noise around the band-edge smears the notch because the loop is close to instability as the second and third integrators get closer to saturation.

2.9.3 ADC Test under Blocking Conditions

2.9.3.1 Single-Tone Test with Blockers

Figure 2.58 shows SNDR performance at different blocker levels at 25 MHz offset. The amplitude of the desired channel signal is set to −40 dBFS (≈ -48 dBV$_{\text{rms}}$) at 1 MHz because it represents the minimum input signal level amplified by 35 dB RF front-end gain. When the blocker to signal amplitude ratio is less than 20 dB, the normal mode operation has better performance than the blocker suppression mode. However, the normal mode starts decreasing SNDR performance when the blocker is greater than 20 dBc while the blocker suppression mode keeps its SDNR performance around 26 dB. With reconfigurable operation between the two modes, at least 26 dB SNDR performance is guaranteed even with the 30 dBc blocker applied at the adjacent channel.

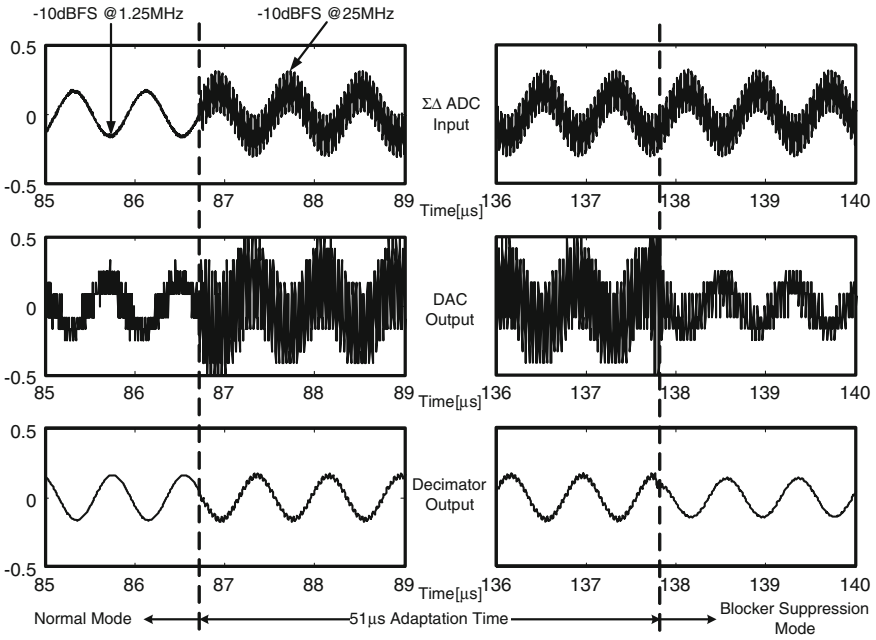

Fig. 2.59 ΣΔ ADC measured transient response with 25 MHz interferer applied to the system

2.10 Transient Measurement Under Blocking Condition

Figure 2.59 shows the measured output transient after a 25 MHz interferer appears at the ADC input during normal reception. The ADC can reconfigure to the blocker suppression mode in 51 μs. For the WiMAX standard, the symbol duration is 102.9 μs and the frame duration is 5 ms (48 symbols) for a 10 MHz bandwidth

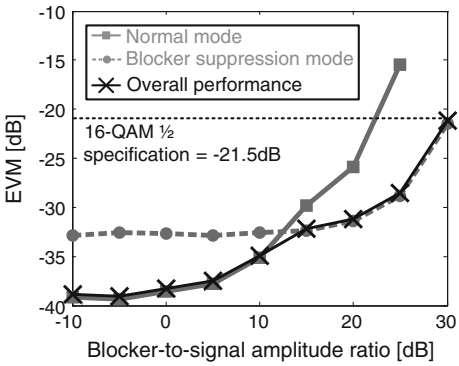

Fig. 2.60 Measured EVM of the normal and blocker suppression modes at different blocker levels

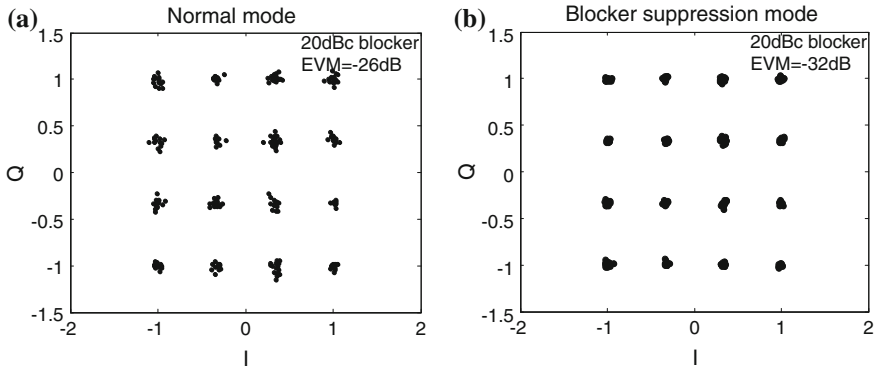

Fig. 2.61 Measured constellations for the normal and blocker suppression modes with 20 dB blocker to signal amplitude ratio

Table 2.4 Summary between the normal and blocker suppression modes

		Normal mode	Blocker suppression mode
DR (dB)		71	66
Composite triple beat (dBc)		17	N/A
SNDR (dB)	Weak blockers (<10 dBc)	34	27
	Strong blockers (30 dBc)	−6 (Unstable)	26
EVM (dB)	Weak blockers (<10 dBc)	−39	−33
	Strong blockers (30 dBc)	N/A	−22
Power consumption (mW)		18	
Integrators		7	
DACs		3	
Blocker detector		1	
Digital blocks		7	

modulation mode.[30] Since the reconfiguration time is 51 μs, only 1 % of a frame would be affected as a worst case. Furthermore, as long as the blocker does not appear during the preamble and frame-map-symbols, the error correction code will fix a corrupted data bit. Because the probability of interferers appearing specifically during the preamble period is about 2 %, the reconfiguration time would have minor effects in data reception. Moreover, because of the availability of interfame gap of the WiMAX standard, the ADC mode can be initialized with the blocker suppression mode in this gap, and then switched to the normal mode if the jammer is not present before the frame starts. This ensures that the preamble is received without an SNR impact.

[30] Mobile WiMAX: Part I: A technical overview and performance evaluation. WiMAX Forum (2006)

2.10.1 EVM Test with a 24 MBPS 16-QAM Signal

Figures 2.60 and 2.61 show the measured EVM performance and constellations in the presence of the adjacent channel interferer. Both of the desired channel signal and interferer are generated from 24 Mbps 16-QAM signal and the channel power is set to −40 dBFS. When the blocker-to-signal amplitude ratio is below 10 dB, the ADC achieves −39 dB EVM in the normal mode against −33 dB EVM in the blocker suppression mode. However, in the blocker suppression mode, the ADC can tolerate a 30 dBc blocker with −22 dB EVM, fulfilling the system requirements.

The performances of the two modes are summarized in Table 2.4. The overall performances are little bit lower than transistor-level full-chip simulation results due to imperfect ground plane and also noise coupling on the printed circuit board.

2.11 Conclusions

In this chapter, sampling rate, dynamic range, and bandwidth adaptation techniques for pipelined and continuous-time ΣΔM ADCs have been introduced. The first part of this chapter presents a power scalable 12 b pipeline ADC that enables or disables OTAs connected in parallel to scale the settling response of Multiplying DAC (MDAC) and Sample/Hold (S/H) amplifiers in order to achieve constant SNDR performance over a range of sampling rates. The proposed technique facilitates optimal power consumption over the entire sampling rate range and reduces design complexity by maintaining constant DC bias conditions in the scaled analog blocks. The reduced design complexity allows for an earlier optimal design to be quickly reconfigured for changed specifications without requiring extensive re-design of the ADC analog core. In the second section an adaptive-blocker-rejection CT ΣΔ ADC for mobile WiMAX receivers, implemented on a 130 nm digital CMOS process, is demonstrated. A key contribution of this research is that it develops a new ADC architecture that can adaptively suppress interferers based on their power level at the ADC input. This topology can reduce the design requirements of analog-baseband filters and VGAs without increasing ADC DR, a challenging task in state-of-the-art deep-submicron technologies. Another contribution is the design of an analog domain blocker-detection circuit with negligible power consumption and die area overhead. The proposed blocker detector can ensure agile estimation of interferers' level and control the reconfigurable loop filter without significant latency. This guarantees stable operation of the modulator even with sudden high blockers applied. To validate this theory, the prototype ADC is tested with various blocking conditions. First, the ADC achieves 65 dB SNDR and 71 dB DR over a 10 MHz signal bandwidth with 250 MHz sampling frequency and 18 mW power consumption. With the integrated blocker detector, the measurement results show that reconfigurable operation can be

obtained to optimize the system performance based on the blocker level at the ADC input. In the normal mode, the modulator is optimized for highest quantization noise suppression, while the blocker-suppression mode is designed to minimize the blocker interference. In the blocker-rejection mode, the ADC can achieve 8 dB and 15 dB blocker attenuation at the adjacent and alternate frequencies, which is almost equivalent to a third-order LPF. This argument proves that the enhanced blocker-rejection performance can improve system selectivity and stability without a base-band channel-select filter, simplifying the receiver's architecture. The ADC can tolerate a 30 dBc blocker at 25 MHz offset with a −40 dBFS desired channel signal, achieving −22 dB EVM. Further, the measured transient behavior shows that the modulator can change its operation mode within 51 s under blocking condition, which is much shorter than the frame duration of the WiMAX standard.

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