

Preface

The main goal of writing this book was to present a methodological and algorithmic perspective on the field-solver-based parasitic extraction of integrated circuits (ICs). Specifically, we present advanced techniques based on three-dimensional (3-D) boundary element method and floating random walk method for the problems of resistance and capacitance (RC) calculation. With the feature size scaling down and mixed-signal interference in modern ICs, the research of parasitic extraction has gained much concern in recent years and promoted the utilization of field-solver methods for tackling the challenge of accuracy.

Now, the field solver which directly solves the electrostatic equations is becoming more and more important for the RC extraction of ICs. It is a necessary supplement, or even a replacer, of the existing parasitic extraction methodology. On accurately capturing the complex interconnect geometry and the substrate coupling in mixed-signal IC, the field-solver method has distinct advantages. The major obstacle for its application is the excessive computational expense. The complexity of interconnect structure and even tighter performance margin for designing nanometer-technology ICs have urged the extensive usage of field solvers. The random process variations also add significance to this request. All these have pushed the related research for 20 years. Various accelerating approaches have been proposed to reduce the computational expense while preserving accuracy. Until recently, the achievements of these works have been applied successfully in industrial tools. They are daily used for settling the sign-off timing and verification issues in various IC designs. These achievements in field-solver-based RC extraction are the object of this book. We hope we have succeeded in providing a unique and comprehensive treatment on them.

The works presented in this book are mostly from research projects undertaken by the Parasitic Extraction Group, Tsinghua University, China. Chapter 3 and Chaps. 5, 6, and 7 are contributed by Xiren Wang, mostly from his Ph.D. work at the Parasitic Extraction Group. The remaining chapters are written by Wenjian Yu, based on his research work. Many of those original publications can be found at <http://learn.tsinghua.edu.cn:8080/2003990088/index.htm>.

We want to emphasize that the book is by no means intended to be comprehensive. The absence of coverage of related works should by no means diminish their value and contribution. Many academic groups and experts from industry have made significant contributions in the field, and the reader is encouraged to investigate their works. Key contributors to progress in RC field-solver techniques include: Jacob White (MIT), Weiping Shi (TAMU), Lawrence T. Pileggi (CMU), Ali Niknejad (UC Berkeley), Dan Jiao (Purdue Univ.), Vikram Jandhyala (Univ. Washington), Luca Daniel (MIT), Yannick L. Le Coz (RPI), Sheldon X.-D. Tan (UC Riverside), Lei He (UCLA), Ranjit Ghapurey (UT Austin), Charlie Chung-Ping Chen (National Taiwan Univ.), Wayne Dai (UCSC), Nick van der Meijs (TU Delft), Luis Miguel Silveira (Technical University of Lisbon), Ibrahim Elfadel (Masdar Institute of Science and Technology), Nasser Masoumi (Univ. Waterloo), Madhav P. Desai (Indian Institute of Technology, Bombay), Angelo Brambilla (Politecnico di Milano), Alkiviades A. Hatzopoulos (Aristotle Univ. Thessaloniki), Ruben Specogna (Univ. Udine), Xuan Zeng (Fudan Univ.), Zeyi Wang (Tsinghua Univ.), Wei Hong (Southeast Univ.), Junfa Mao (Shanghai Jiaotong Univ.), Martin Bachtold (Swiss Federal Institute of Technology), Sharad Kapur (Integrand Software Inc.), Joel R. Phillips (Cadence Inc.), Xiaoning Qi (Intel), and Zhuoxiang Ren (Mentor Graphics Inc.).

Beijing, China
San Jose, CA, USA

Wenjian Yu
Xiren Wang

Advanced Field-Solver Techniques for RC Extraction of
Integrated Circuits

Yu, W.; Wang, X.

2014, XV, 246 p. 104 illus., Hardcover

ISBN: 978-3-642-54297-8