

Contents

1	Introduction	1
1.1	CMOS Scaling: Evolutionary Era	1
1.2	CMOS Scaling: Revolutionary Era	3
1.2.1	Strain Engineering (90 and 65 nm Technology Nodes)	4
1.2.2	High-k Metal Gate Technology	4
1.2.3	Tri-Gate (finFET) Technology	5
1.3	High Mobility Channels for Future CMOS Technology Nodes	8
1.4	Reliability Limitations	12
1.5	Variability Issues	13
1.6	Objectives and Structure of this Work	15
1.7	Summary of this Chapter	16
	References	16
2	Degradation Mechanisms	19
2.1	Introduction	19
2.2	Negative Bias Temperature Instability	20
2.2.1	First-Order Phenomenological Observations	22
2.2.2	Basic Interpretation: Why does the V_{th} Shift?	26
2.2.3	NBTI Relaxation	27
2.2.4	Reaction–Diffusion Model	29
2.2.5	NBTI Relaxation: A Crucial Benchmark for Degradation Models	33
2.2.6	Recent NBTI Observations: Small-Area Devices	36
2.2.7	Extended Shockley–Read–Hall Trapping Models	42
2.2.8	Nonradiative Multiphonon Theory	44
2.2.9	A Defect Model for RTN and NBTI	48
2.2.10	A Two-Stage Model for NBTI	50
2.3	Hot Carriers	53
2.3.1	Hot Carrier Typology	54
2.3.2	First-Order Modeling of Channel hot Carrier Generation	55
2.3.3	Hot Carrier Degradation	57

2.4	Time-Dependent Dielectric Breakdown	59
2.5	Summary of this Chapter	63
	References	64
3	Techniques and Devices	67
3.1	Introduction	67
3.2	Advanced NBTI Measurement Techniques	67
3.2.1	Measure-Stress-Measure Techniques	68
3.2.2	On-the-fly Measurement Techniques	70
3.3	Techniques and Methodologies used in this Work	72
3.3.1	eMSM Implementation	72
3.3.2	From eMSM Data to Lifetime Extrapolation and Benchmarking	73
3.3.3	Empirical Analytical Description of NBTI Relaxation Traces: Extraction of the So-Called ‘Recoverable’ and ‘Permanent’ Components	76
3.3.4	NBTI Experiments in Nanoscaled Devices	77
3.3.5	The Charge Pumping Technique	80
3.4	Devices used in this Work	83
3.4.1	Ge Fraction	86
3.4.2	QW Thickness	87
3.4.3	Si Cap Thickness	89
3.5	Structures used in this Work	89
3.5.1	Standard SiGe Device Structures	89
3.5.2	Special Structures: Poly-Si Heaters	90
3.6	Summary of this Chapter	97
	References	97
4	Negative Bias Temperature Instability in (Si)Ge pMOSFETs	99
4.1	Introduction	99
4.2	Impact of the Individual Gate Stack Parameters	99
4.2.1	Ge Fraction	100
4.2.2	SiGe Quantum Well Thickness	100
4.2.3	Si Cap Thickness	100
4.3	Gate Stack Optimization: Demonstrating Sufficient NBTI Reliability at UT-EOT	102
4.4	Process- and Architecture-Independent Results	104
4.5	Detailed Discussion of the Experimental Results	106
4.5.1	Power-Law Time Exponent and E_{ox} -Acceleration	106
4.5.2	Temperature Activation	107
4.5.3	Interface State Creation (ΔN_{it}) and Hole Trapping (ΔN_{ot})	108
4.5.4	Faster NBTI Relaxation	109
4.5.5	Summary of the Experimental Observations	110

4.6	Body Bias and NBTI	110
4.6.1	Body Bias During NBTI Stress Only	113
4.6.2	Body Bias During NBTI Stress and Relaxation	115
4.7	Model	117
4.7.1	Disqualified Models	117
4.7.2	Reduced P (ΔN_{it})	119
4.7.3	Reduced R (ΔN_{ot})-A Model for the Superior NBTI Reliability of (Si)Ge Channel pMOSFETs	121
4.8	Final Considerations: Performance Versus Reliability	125
4.9	Summary of this Chapter	127
	References	127
5	Negative Bias Temperature Instability in Nanoscale Devices	129
5.1	Introduction	129
5.2	NBTI on Nanoscale SiGe Devices	130
5.2.1	Individual Discharge Events	131
5.2.2	Average Number of Active Defects per Device $\langle N_T \rangle$	133
5.2.3	Average ΔV_{th} Impact per Charged Defect η	133
5.2.4	Average Charged Defect Emission Time	135
5.2.5	Summary of the Experimental Observations	136
5.3	Implications for the Time-Dependent Variability	136
5.4	Model	138
5.5	Impact of Single Charged Gate Oxide Defects: Area Scaling	141
5.6	Impact of Single Charged Gate Oxide Defects on the Entire FET Current Characteristics: V_G -Dependence	143
5.6.1	Experimental Results	143
5.6.2	Discussion	144
5.7	Impact of Single Charged Gate Oxide Defects: Body Bias Dependence	150
5.8	Summary of this Chapter	156
	References	157
6	Channel Hot Carriers and Other Reliability Mechanisms	159
6.1	Introduction	159
6.2	Experimental Methodology for Studying the Interplay of CHC and NBTI	160
6.3	Interaction of CHC and NBTI in pMOSFETs	162
6.3.1	Recoverable Component	162
6.3.2	Permanent Component	165
6.3.3	Consequences for Si Channel Devices	167
6.3.4	Summary of this Section	168

6.4	CHC in SiGe pMOSFETs	168
6.4.1	Impact of the Si Cap Thickness.	169
6.4.2	CHC Lifetime of the NBTI-Optimized SiGe Gate Stack	170
6.4.3	Summary of this Section	171
6.5	CHC in Ge pMOSFETs	171
6.5.1	Halo Engineering.	172
6.5.2	Summary of this Section	176
6.6	Other Reliability Mechanisms	177
6.6.1	Low-Frequency Noise	177
6.6.2	Time-Dependent Dielectric Breakdown	177
6.7	Summary of this Chapter	178
	References	179
7	Conclusions and Perspectives	181
7.1	Conclusions	181
7.2	Perspectives	183
	Further Reading	184

Reliability of High Mobility SiGe Channel MOSFETs for
Future CMOS Applications

Franco, J.; Kaczer, B.; Groeseneken, G.

2014, XIX, 187 p. 219 illus., Hardcover

ISBN: 978-94-007-7662-3