

Chapter 2

Electrical Modeling of a Through Silicon Via

Joohee Kim, Jun So Pak and Jounggho Kim

Abstract 3D IC is emerging as a powerful solution for the next-generation system packaging and integration technology to achieve low power consumption, high channel bandwidth and high density integration capability simultaneously. As for the vertical interconnect for a 3D IC, through-silicon via (TSV) is a key component which can provide a significant performance improvement with greatly reduced physical length of channels among vertically integrated chips. In this chapter, the scalable and analytic electrical model of a TSV is proposed and the high-frequency electrical behavior and signaling performance of a TSV is analyzed in frequency and time domains.

Keywords Differential signal TSV • Equivalent circuit model • Single-ended signal TSV • Scalable model • TSV channel • 3D IC

2.1 Introduction

As technology advances in the nanometer era, the packaging density and system performance of individual chips improve. However, the scaling of the minimum feature size of the transistor slows due to the limitations from leakage power

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consumption, process variation, and cost issues [1–3]. In addition, many electronic devices, such as tablets, laptops, and smart phones, have become more compact, and, they must achieve multi-function and high-throughput computing performance simultaneously. As a new powerful paradigm for next-generation system integration and packaging technology, 3-dimensional integration emerges as a promising solution. With 3D integration, many chips can be integrated in a vertical axis, thus improving the system bandwidth by reducing the physical lengths of the channels among the integrated chips. The conceptual scheme of 3-dimensional integrated circuits (3D ICs) is shown in Fig. 2.1. As shown in Fig. 2.1, various functional dies, such as memory, RF, and processor dies, are vertically and horizontally integrated on a silicon-based interposer to be integrated in one package. A through-silicon via (TSV) forms the vertical interconnect between stacked dies, which enables a pure 3D IC to be realized and satisfies the small form factor, low power consumption and high bandwidth system requirements simultaneously. As shown in Fig. 2.1, a TSV is a via hole passing through the silicon substrate, which is filled with a conductor such as copper (Cu), tungsten (W) or polycrystalline silicon (poly-Si) for the electrical connection between dies [4]. An insulation layer surrounding the via is used to electrically isolate the conductive silicon substrate and TSV. Figure 2.2 shows SEM image of one test vehicle which includes TSV, RDL, and insulation layer. Even then, the low fabrication yield from TSV and 3D IC fabrication processes such as high-aspect-ratio via drilling/filling, thin silicon-dioxide sidewall deposition, and die stacking with micro-bumps is an issue [5]. However, a TSV-based 3D IC is the way to go because it overcomes the critical bottlenecks of 2-dimensional ICs in many ways, providing higher system bandwidth and lower power consumption from the reduced chip-to-chip channel parasitics, higher design flexibility and design freedom for multi-functional systems, and highly dense packaging to achieve a smaller form factor. In addition, a TSV, which has a diameter of several μm , can widen the bus width for the higher system bandwidth without consuming more die area than wire bonding or flip-chip bonding integrations. As a result, wide I/O design could be achieved more efficiently by using TSVs and the number of I/Os of a TSV-based 3D IC will keep increasing. Thus, understanding the electrical behavior of a TSV, which can greatly impact on the overall 3D IC system performance is very important.

To design high-speed I/O channels with TSVs and perform signal integrity analysis for the advanced 3D IC design, the TSVs must be electrically modeled using design parameters such as geometric and material information up to the GHz range. Then, the electrical model can be combined with other circuitry so that the overall electrical performances of the system can be easily computed. Therefore, the modeling and analysis of a TSV have been extensively researched as detailed in [6–15]. With various targets or applications of 3D IC designs, the model has to estimate the electrical behavior of a TSV, even if given different physical dimensions and material properties. Thus, a scalable model of the TSV incorporating analytic equations must be proposed. Then, if the physical structure or the material changes, the model can be scaled to estimate the electrical behavior of the TSV channel based on the changes in the design parameters. Furthermore, a model

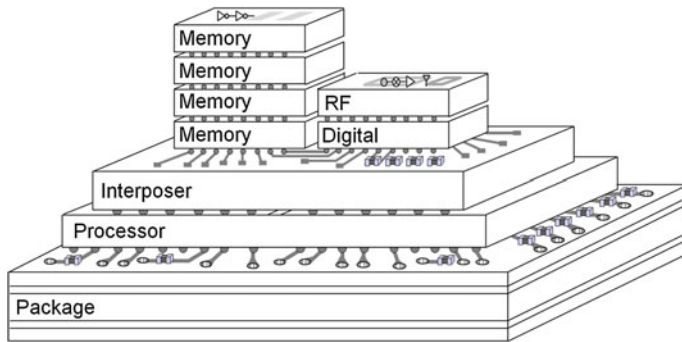
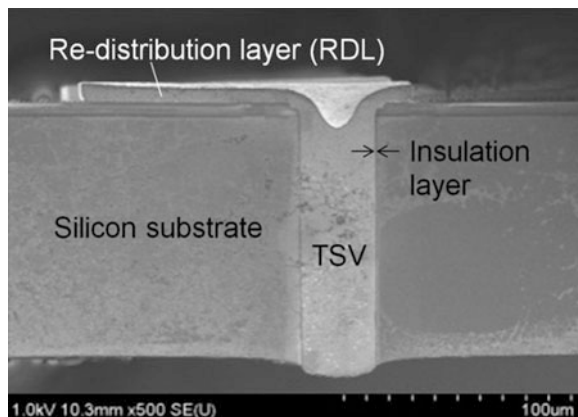


Fig. 2.1 A 3-dimensional integrated circuit (3D IC); a vertical integration of homogenous and heterogeneous dies, such as memory, RF, digital, processor die, and interposer, for realizing highly dense packaging for high-speed integrated circuit systems [15] © 2011 IEEE

Fig. 2.2 A scanning electron microscopy (SEM) picture of a through silicon via (TSV), which is a via hole through the silicon substrate, filled with metal, and surrounded by an insulation layer between the substrate and via [15] © 2011 IEEE



with analytic closed-form equations can be expanded to evaluate electrical performances such as power consumption, delay, and skew along the TSV-based interconnect. In addition, the model provides insight into a TSV by including the physical meaning of each parasitic component. Therefore, modeling with analytic closed-form equations is very powerful.

In this chapter, the high-frequency scalable electrical model of a TSV with analytic *RLGC* equations is proposed. The electrical behaviors of a TSV are analyzed with the proposed model. The analytic equations of the scalable model are proposed in terms of design parameters, such as physical dimensions and material properties. Thus, each analytic equation fully represents the physical meaning of a parasitic component of a TSV. The scalability of the proposed model for a TSV is verified by simulation with parametric variations from the 3D field solver. As a result, a high-frequency scalable electrical model of the TSV channel is proposed. To experimentally verify the proposed model, a series of test vehicles of a TSV

channel are fabricated. The proposed model is experimentally verified with S-parameter measurements up to 20 GHz. Therefore, the electrical characteristics of a TSV channel are analyzed in the frequency domain with the verified scalable model and with variations in design parameters. From this analysis, the capacitive and resistive electrical behaviors of a TSV channel are characterized. In addition, the design parameters that dominantly affect the TSV channel characteristic are analyzed in various frequency ranges. Furthermore, the overall electrical behavior of the TSV channel is analyzed with fabricated test vehicles in the time domain. The time-domain analysis of the TSV channel is performed using eye diagram measurements for up to 10 Gbps input signals of pseudo-random bit data patterns.

2.2 Equivalent Circuit Model of a TSV

In this section, the electrical circuit model of a TSV, which is a physics-based equivalent circuit model, is presented. This electrical model is proposed with analytic *RLGC* equations based on the lumped model. Because the model is derived from the physical structure, it fully expresses the physical meaning of each parasitic component with the proposed closed-form equations. For the scalability of the model, the model is proposed with structural parameters and material properties as variables of the analytic *RLGC* equations. The structure and parameters of a TSV are shown in Fig. 2.3.

Figure 2.3 shows the structure and parameters of a signal TSV, a ground TSV and bumps in a single-ended signaling configuration with the via-last process. A via-last TSV is a type of TSV that is formed after metallization. Thus, a via-last TSV passes through not only the substrate but also the inter-metal dielectric (IMD) layer. Because a TSV has to connect between top and bottom dies, it passes through the silicon substrate vertically and the via is filled with metal for the electrical conduction. Copper (Cu), tungsten (W), and polycrystalline silicon (poly-Si) are used as conductive fill materials. Among them, copper fill becomes the mainstream approach today. For the substrate material, silicon is generally used to support semiconductor devices; however, glass or other organic substrates are also considered as the substrate material to improve insulating performance [16].

For the current technology, the diameter of a TSV is several μm ($<10\ \mu\text{m}$) and the height of a TSV is less than $50\ \mu\text{m}$. With the help of the greatly reduced length of the interconnect between chips, TSV-based 3D IC has a significant advantage over to 2D or 2.5D integration with wire bonding or flip chip packaging. In addition, TSV-based 3D IC enables wide I/O application, because TSV consumes much smaller die area per I/O. For the TSV-to-TSV pitch, the diameter to pitch ratio is approximately 1:2.5 to 1:4 and depends on the fabrication technology and the keep-out zone around a TSV. The thickness of the thin insulating layer surrounding via is in the 0.1 to $0.5\ \mu\text{m}$ range. There is another insulation layer that forms on the bottom side of the silicon substrate, and this layer is referred to as the bottom oxide layer. This insulation layer is necessary to provide insulation

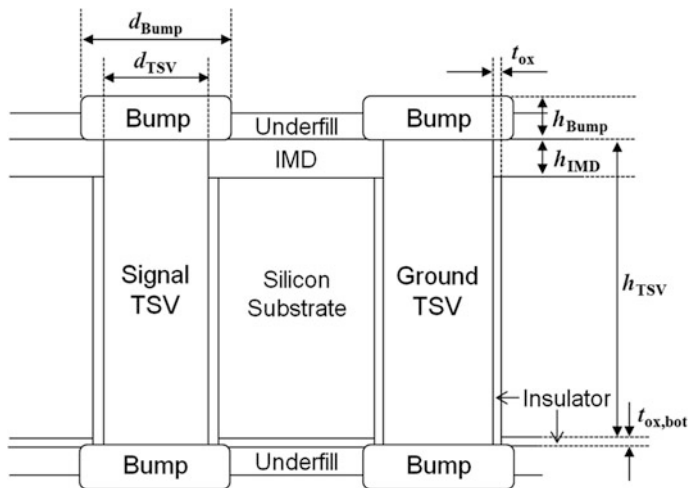


Fig. 2.3 A single-ended signal TSV structure and design parameters for the scalable modeling [15] © 2011 IEEE

between the conductive silicon substrate and the metallic bump and also has a thickness in the 0.1 to 0.5 μm range.

With this structure, a high-frequency scalable electrical model of TSVs with bumps is proposed in Fig. 2.4. Each of the *RLGC* components corresponds to a structure of a TSV. The analytic *RLGC* equations are derived from the physical configuration with the design parameters. Therefore, each *RLGC* equation is a function of the variables from the design parameters. As shown in Fig. 2.4, the scalable electrical model is proposed by lumped components. The total lengths of the TSV interconnect including the TSV and bump decrease to tens of μm as the process technology advances. Because this length is sufficiently short compared to the wavelength of the several or tens of GHz operating frequency, the lumped approximation is valid and a single lumped stage is sufficient for the TSV model.

In the case of the via-first or middle process, the parasitic capacitances such as the capacitance of IMD layer (C_{IMD}) should be neglected or other parasitic capacitances has to be additionally considered to accurately estimate the electrical behaviors of a TSV. In addition, if there are active circuits between TSVs, the assumed field distribution can be changed. However, the main electrical characteristics and the loss mechanism of a TSV channel are valid with the proposed model.

In a practical design, many TSVs, such as array-type TSVs, are designed, instead of a single GS pair of TSVs. However, the equivalent circuit model of a TSV among TSV array is equivalent to the proposed model shown in Fig. 2.4, differing in that different weights have to be applied for each *RLGC* component. Thus, we can perform array-type TSV modeling by extracting or modeling the weights of the *RLGC* components.

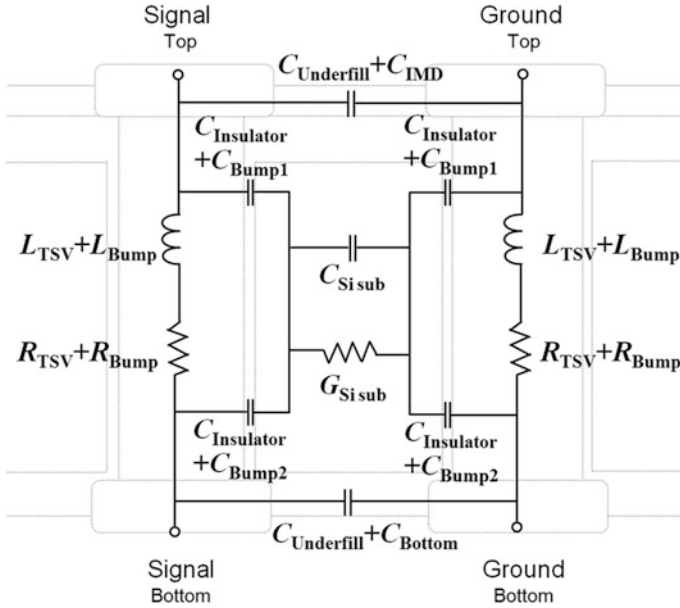


Fig. 2.4 An equivalent circuit model of a pair of signal and ground TSVs with bumps with *RLGC* lumped elements assuming that the silicon substrate is floated [15] © 2011 IEEE

2.2.1 Electrical Modeling of a TSV with the Analytic Equations

In this chapter, analytic *RLGC* components of the proposed equivalent circuit model of a TSV are proposed and electrically modeled with analytic equations which are functions of material properties, structural parameters, frequency, and etc. The proposed equivalent circuit model is derived based on the physical structure of a TSV. Among various TSV parasitics, the capacitance of a TSV is the most important factor which determines the overall electrical behavior of a TSV. To electrically isolate the TSV from the conductive silicon substrate, an insulation layer surrounding the TSV is necessary. Due to this insulation layer, there is an insulator capacitance, $C_{Insulator}$, as shown in Fig. 2.5. In this work, the substrate is assumed to be floated. If the substrate is fully biased to the ground, then the depletion capacitance has to be added to $C_{Insulator}$ in series [13]. Since the TSV is filled with metal and the silicon substrate is conductive, the insulator capacitance can be derived from the coaxial-cable capacitance model [17, 18]. This equation is originally obtained by solving Poisson's equation in a cylindrical coordinate system. Thus, $C_{Insulator}$ is a function of d_{TSV} , h_{TSV} , and t_{ox} , as shown in (2.1). Since the insulator capacitance of a TSV is separated into two parallel parts, as shown in Fig. 2.5, the equation of $C_{Insulator}$ is expressed as half of the insulator capacitance

Fig. 2.5 A top view and a perspective view of a TSV which passes through the silicon substrate vertically. The TSV is surrounded by an insulator to be isolated from the conductive silicon substrate. Thus, $C_{Insulator}$ is derived from the coaxial-cable capacitance model which is determined by d_{TSV} , t_{ox} , h_{TSV} , and h_{IMD} [15] © 2011 IEEE

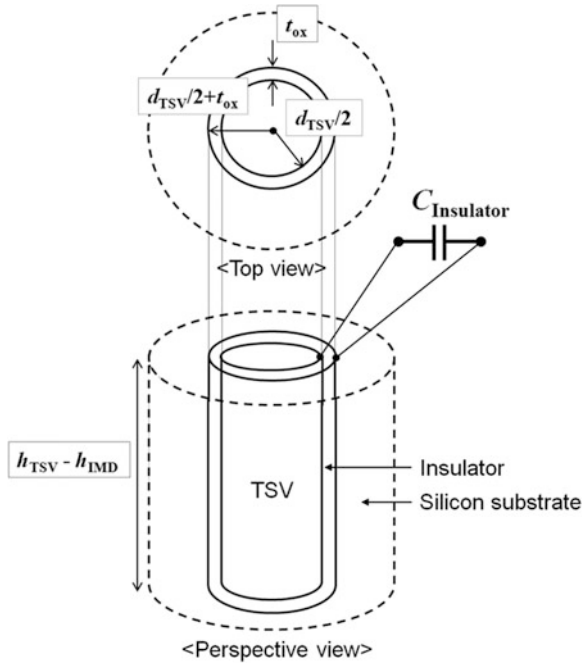
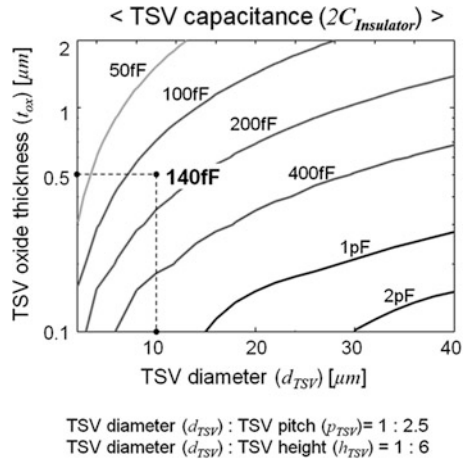


Fig. 2.6 TSV capacitance values from the proposed analytic equations of $C_{Insulator}$ depending on variations of TSV diameter (d_{TSV}) with the fixed ratio of d_{TSV} to TSV pitch (p_{TSV}) as 1:2.5 and d_{TSV} to TSV height (h_{TSV}) as 1:6



of a TSV. The calculated $C_{Insulator}$ is plotted in Fig. 2.6. Since the absolute value of the TSV capacitance is not even 1 pF with the default dimension presented in Fig. 2.6, this capacitance is the most dominant parasitic capacitance which determines the overall electrical behavior of a TSV.

$$C_{Insulator} = \frac{1}{2} \left\{ 2\pi \times \epsilon_0 \epsilon_{r,Insulator} \times \frac{h_{TSV} - h_{IMD}}{\ln \left(\frac{\frac{d_{TSV} + t_{ox}}{2}}{\frac{d_{TSV}}{2}} \right)} \right\} [F] \quad (2.1)$$

Because TSV has 3-dimensional structure in the lossy silicon substrate, there is a leakage through the substrate when there is a ground TSV near a signal TSV. The amount of leakage current through the substrate is determined by the impedance of the leakage path between signal and ground TSVs, thus, the impedance of the $C_{Insulator}$ significantly affect to the insertion loss of a TSV due to the leakage through the silicon substrate. As a result, as $C_{Insulator}$ increases, the insertion loss of a TSV increases. If we decrease TSV diameter and increase TSV oxide thickness, we can reduce TSV capacitance as shown in Fig. 2.6.

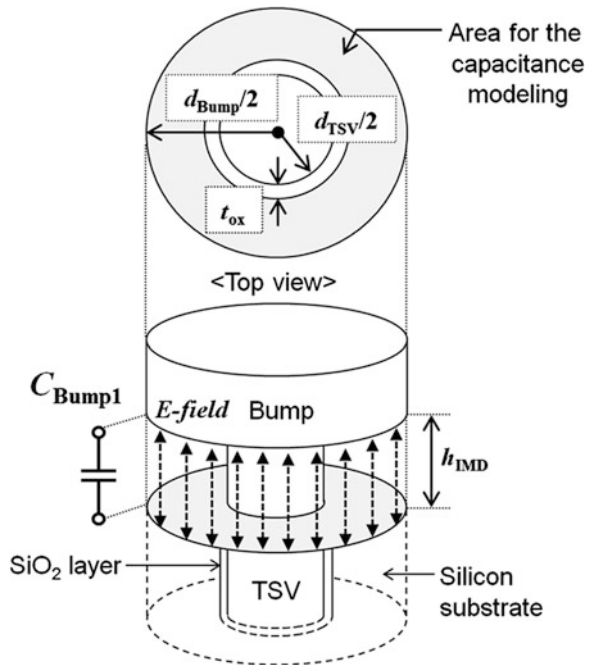
In addition, the conductance due to the loss tangent of the oxide insulator is ignored in the proposed model since it does not affect the insertion loss of a TSV considering the silicon substrate with the conductivity of 10 S/m. If the conductivity of the silicon substrate becomes very small like as high-resistivity silicon substrate, the loss of a TSV is not dominantly dependent on the silicon substrate conductance any more. Then, TSV resistance or the dielectric loss due to the loss tangent of the oxide insulator become dominant which affect the insertion loss of a TSV, and thus, we cannot ignore dielectric loss terms. For example, when the material of the substrate is glass, the dielectric loss of the insulation layer has to be considered for the accurate high-frequency modeling of a through-glass via (TGV). Furthermore, if the temperature increases, the relative permittivity of the dielectric material decreases which results in the smaller parasitic capacitance. The temperature effect on electrical behavior of a TSV is analyzed with analytical temperature-dependent modeling a TSV in Chap. 5.

One of the bump-to-silicon substrate capacitances of the upper side of the silicon substrate, C_{Bump1} , has to be added to $C_{Insulator}$ of the proposed equivalent circuit model, as shown in Fig. 2.7. This capacitance can be modeled as a parallel-plate capacitor [19]. As shown in Fig. 2.7, the area, where the electric fields are formed, corresponds to where the bump overlies the silicon substrate through the inter-metal dielectric (IMD) layer. Thus, C_{Bump1} is proportional to this area and inversely proportional to the IMD height, h_{IMD} . As a result, C_{Bump1} can be calculated with (2.2), which depends on d_{TSV} , d_{Bump} , and h_{IMD} .

$$C_{Bump1} = \epsilon_0 \epsilon_{r,IMD} \times \frac{\pi \left\{ \left(\frac{d_{Bump}}{2} \right)^2 - \left(\frac{d_{TSV}}{2} + t_{ox} \right)^2 \right\}}{h_{IMD}} [F] \quad (2.2)$$

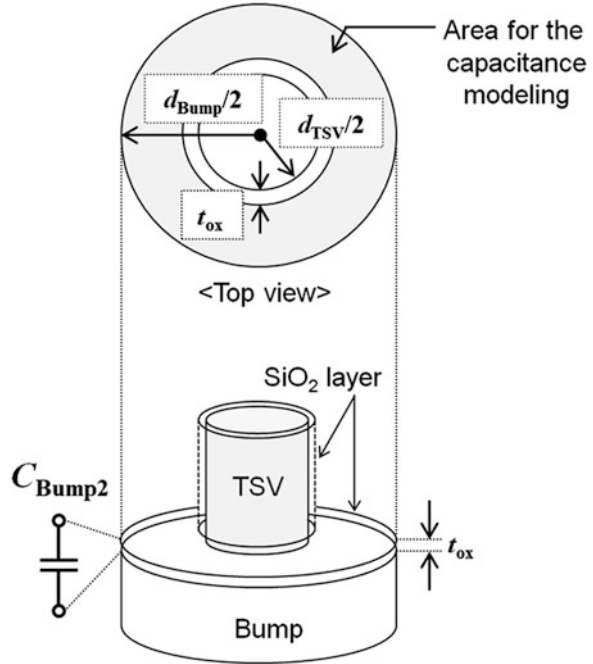
In a similar manner, another bump-to-silicon substrate capacitance due to the bottom oxide layer on the bottom side of the silicon substrate, C_{Bump2} , has to be added to $C_{Insulator}$. This bottom oxide layer is formed by the oxidation after back-grinding of the silicon substrate. This process is necessary to expose the TSV and

Fig. 2.7 A top view and a perspective view of the upper part of a TSV with a bump to calculate the area where the electric fields are formed between the bump and the silicon substrate to model C_{Bump1} which has parallel-plate capacitor configurations [15] © 2011 IEEE



connect it with another die. In general, the bottom oxide thickness is very thin under $0.5 \mu m$ so that the value of C_{Bump2} is considerable to the overall parasitic capacitance of a TSV. C_{Bump2} is also derived from the parallel-plate capacitor model, as shown in Fig. 2.8. Therefore, d_{TSV} , d_{Bump} , h_{Bump} , and the bottom oxide thickness, $t_{ox,bot}$, determines C_{Bump2} , as shown in (2.3). From (2.3), if the bump diameter increases, C_{Bump2} increases. Since the oxide thickness of the back-side of the silicon is in 0.1 to $0.5 \mu m$ range, if the bump diameter is much bigger than the TSV diameter, the impact of C_{Bump2} on the capacitive characteristic of a TSV becomes very significant as much as that of $C_{Insulator}$. As the TSV technology advances, fine-pitch TSVs are preferred since it can reduce capacitive parasitic as well as die area consumption even with large number of I/Os. However, if the micro-bump directly contacted to a TSV does not shrink as much as TSVs, there will be still a significant amount of parasitic capacitance due to the C_{Bump2} even with the reduced parasitic capacitance from the reduced TSV diameter effect. Therefore, not only TSV diameter but also bump diameter has to be decreased in order to effectively reduce the parasitic capacitance of a TSV. If both sides of the silicon substrate are used for metal layers for signal routing or power distribution network, then this capacitance can be removed from the equivalent circuit model of a TSV.

Fig. 2.8 A top view and a perspective view of the bottom part of a TSV with a bump to calculate the area where the electric fields are formed between the bump and the silicon substrate to model C_{Bump2} which has parallel-plate capacitor configurations [15] © 2011 IEEE



$$C_{Bump2} = \epsilon_0 \epsilon_{r,ox} \times \frac{\pi \left\{ \left(\frac{d_{Bump}}{2} \right)^2 - \left(\frac{d_{TSV}}{2} + t_{ox,bot} \right)^2 \right\}}{t_{ox,bot}} \text{ [F]} \quad (2.3)$$

With the via-last process, the capacitance between the signal and ground bumps from the underfill, $C_{Underfill}$, the capacitances between the signal and ground TSVs from the IMD layer, C_{IMD} , and the bottom oxide layer, C_{Bottom} , have to be modeled. As shown in Fig. 2.9, the cross-sectional areas of the TSV and bump are circular. Hence, $C_{Underfill}$, C_{IMD} , and C_{Bottom} are derived from the model of the parallel-wires capacitance [19]. The capacitances are determined by the distance between the signal and ground TSVs or bumps, p_{TSV} , the diameter of the TSV and bump, d_{TSV} and d_{Bump} , and the height of the underfill, IMD layer and bottom oxide, h_{Bump} , h_{IMD} , and $t_{ox,bot}$. If d_{TSV} and d_{Bump} are very small in comparison with the distance of separation, $\frac{p_{TSV}}{d_{TSV}}$ (or $\frac{p_{TSV}}{d_{Bump}}$) $\gg 1$, the natural logarithm replaces the inverse hyper cosine to simplify the calculation. However, since the TSV in 3D IC is for denser integration with fine pitch, we assume that the ratio of p_{TSV} and d_{TSV} or d_{Bump} , $\frac{p_{TSV}}{d_{TSV}}$ (or $\frac{p_{TSV}}{d_{Bump}}$), is less than 10. Therefore, $C_{Underfill}$, C_{IMD} , and C_{Bottom} are modeled as shown in (2.4–2.6) (Fig. 2.10).

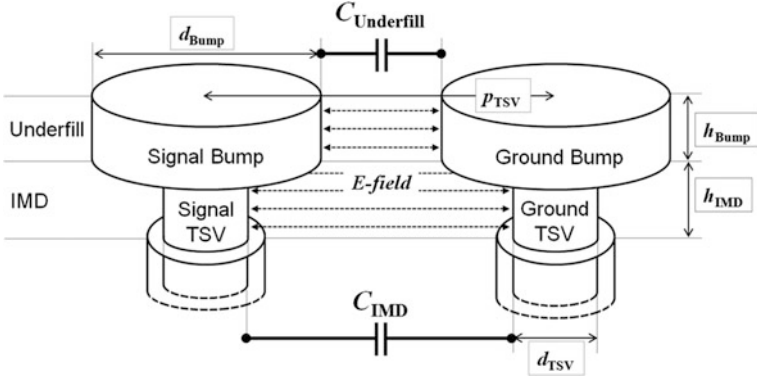


Fig. 2.9 The upper part of a TSV and a bump with electric fields formed between the signal and ground TSVs and bumps to model $C_{\text{Underfill}}$ and C_{IMD} . The TSV/Bump signal and ground pairs are in a parallel-wire capacitor configuration. $C_{\text{Underfill}}$ is formed due to the underfill between bumps, and C_{IMD} is formed due to the IMD between TSVs [15] © 2011 IEEE

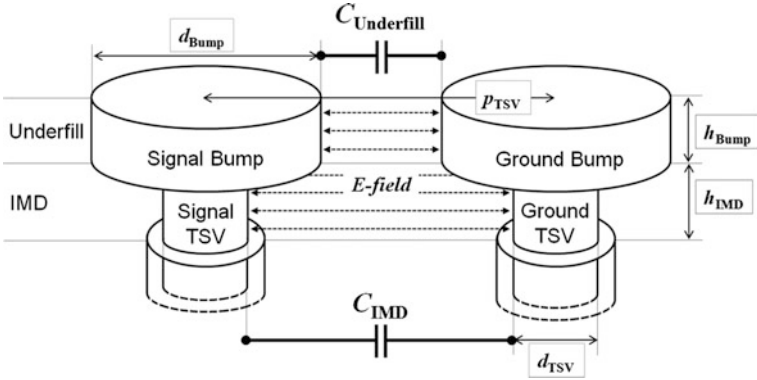


Fig. 2.10 The bottom part of a TSV and a bump with the electric fields formed between signal and ground TSVs to model C_{Bottom} , which are in the parallel-wire capacitor configuration. C_{Bottom} is formed due to the bottom oxide layer between TSVs [15] © 2011 IEEE

$$C_{\text{Underfill}} = \frac{\pi \times \epsilon_0 \epsilon_{r, \text{Underfill}}}{\cosh^{-1} \left(\frac{p_{\text{TSV}}}{d_{\text{Bump}}} \right)} \times h_{\text{Bump}} \text{ [F]} \quad (2.4)$$

$$C_{\text{Underfill}} = \frac{\pi \times \epsilon_0 \epsilon_{r, \text{Underfill}}}{\cosh^{-1} \left(\frac{p_{\text{TSV}}}{d_{\text{Bump}}} \right)} \times h_{\text{Bump}} \text{ [F]} \quad (2.5)$$

$$C_{\text{IMD}} = \frac{\pi \times \epsilon_0 \epsilon_{r, \text{IMD}}}{\cosh^{-1} \left(\frac{p_{\text{TSV}}}{d_{\text{TSV}}} \right)} \times h_{\text{IMD}} \text{ [F]} \quad (2.6)$$

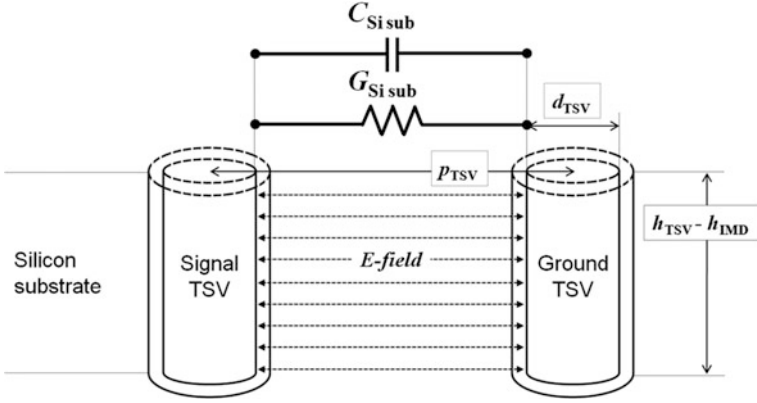


Fig. 2.11 A TSV passing through the silicon substrate with the electric fields formed between signal and ground TSVs to model $C_{Si\ sub}$ and $G_{Si\ sub}$. The parallel-wire capacitor configuration is implemented [15] © 2011 IEEE

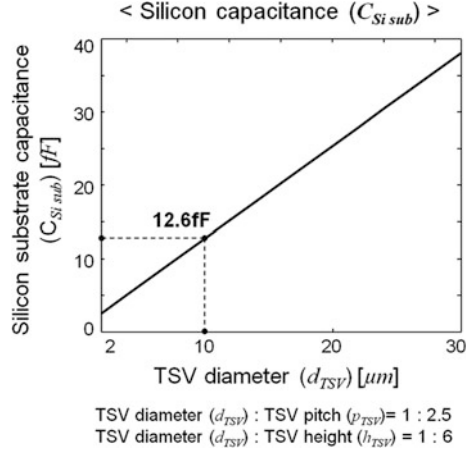
There is another parasitic capacitance contributed to the lateral side of the bump. This capacitance is formed between the lateral side of the bump and the conductive silicon substrate. It has to be added to $C_{Insulator}$ of the proposed model. It can be calculated from the conformal mapping method of the vertical plate. This method transforms a 3-dimensional interconnect into a parallel plate configuration [20]. With d_{TSV} of 30 μm , d_{Bump} of 70 μm , h_{Bump} of 10 μm and h_{IMD} of 6 μm , this capacitance is about 10 fF. This parasitic capacitance is not included as in parallel with $C_{Insulator}$ in this proposed model, but, this fringe capacitance cannot be ignored if the value of this capacitance becomes tens of fF.

Since the silicon is a semiconductor, there are capacitance and conductance between the signal and ground TSVs, as shown in Fig. 2.11. In a similar manner as modeling $C_{Underfill}$, C_{IMD} , and C_{Bottom} , the capacitance of the silicon substrate, $C_{Si\ sub}$, is modeled by applying the parallel-wires capacitance model in (2.7). Thus, $C_{Si\ sub}$ is expressed as a function of d_{TSV} , p_{TSV} , h_{TSV} , and h_{IMD} . The $h_{TSV} - h_{IMD}$ term expresses the valid height where the electric fields are formed between the signal and ground TSVs in the silicon substrate. In addition, a material property, the relative permittivity of the silicon substrate, $\epsilon_{r,Si}$, is also a variable of $C_{Si\ sub}$. Depending on dimension variations, the calculated $C_{Si\ sub}$ is plotted in Fig. 2.12.

$$C_{Si\ sub} = \frac{\pi \times \epsilon_0 \epsilon_{r,Si}}{\cosh^{-1}\left(\frac{p_{TSV}}{d_{TSV}}\right)} \times (h_{TSV} - h_{IMD})[\text{F}] \quad (2.7)$$

In most circuit designs, the dielectric losses can be ignored since the conductor losses are dominant. However, as frequencies increase, it is important to consider the dielectric losses which vary with frequency. When dielectric losses are accounted for, the dielectric constant of the material becomes complex: $\epsilon = \epsilon' - j\epsilon''$. Since the imaginary portion represents the losses, $\frac{1}{\rho} = 2\pi f \epsilon''$ becomes the equivalent loss

Fig. 2.12 Silicon substrate capacitance values from the proposed analytic equations of $C_{Si\ sub}$ depending on variations of TSV diameter (d_{TSV}) with the fixed ratio of d_{TSV} to TSV pitch (p_{TSV}) as 1:2.5 and d_{TSV} to h_{TSV} as 1:6



mechanism, where ρ is the effective resistivity of the dielectric material and f is the frequency. Thus, the loss tangent can characterize the loss in dielectrics with $\tan|\delta d| = \frac{1}{2\rho\pi f\epsilon} = \frac{\epsilon''}{\epsilon'}$ and then the relationship between capacitance and conductance can be established as $G = \frac{\epsilon'}{\epsilon''}(2\pi fC)$, resulting in the relationship in (2.8) [21]. Thus, the conductance of the silicon substrate, $G_{Si\ sub}$, is proposed in (2.9).

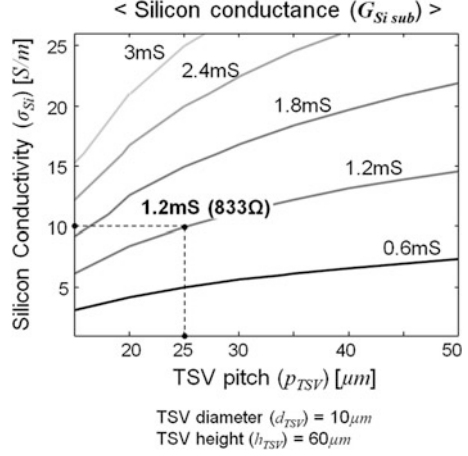
$$\frac{C_{Si\ sub}}{G_{Si\ sub}} = \frac{\epsilon_{Si}}{\sigma_{Si}} \quad (2.8)$$

$$G_{Si\ sub} = \frac{\pi \times \sigma_{Si}}{\cosh^{-1}\left(\frac{p_{TSV}}{d_{TSV}}\right)} \times (h_{TSV} - h_{IMD})[S] \quad (2.9)$$

The physical origin of $G_{Si\ sub}$ is the silicon conductivity, σ_{Si} , which is predominantly determined by the majority carrier concentration. Therefore, it is another significant design parameter, which dominantly affects the insertion loss of a TSV. As shown in Fig. 2.13, silicon conductance increases as silicon conductivity increases. Thus, high-resistivity substrate may decrease silicon conductance which reduces the insertion loss. In addition, increasing TSV-to-TSV pitch can be another way to reduce the leakage through the lossy silicon substrate to the ground by decreasing $G_{Si\ sub}$.

The resistances of the TSV and bump, R_{TSV} and R_{Bump} , are also modeled with structural parameters, as shown in (2.10) and (2.11). High-frequency current flows close to the surface of the conductor due to the formation of the eddy current, which is called the “skin effect”. To model R_{TSV} and R_{Bump} with a non-uniform current distribution at high frequencies, the depth of penetration, which is the skin depth, has to be determined to calculate the resistance of the TSV and bump. The skin depth is defined by material properties, such as the permeability in H/m and

Fig. 2.13 Silicon substrate conductance values from the proposed analytic equations of $G_{Si\ sub}$ depending on variations of silicon conductivity (σ_{Si}) and TSV diameter (d_{TSV}) with d_{TSV} of 10 μm and h_{TSV} of 60 μm



the conductivity in S/m, and also the frequency in Hz [21]. Therefore, the analytic equations of R_{TSV} and R_{Bump} are presented in (2.10) and (2.11).

$$R_{TSV} = \sqrt{R_{dc,TSV}^2 + R_{ac,TSV}^2} [\Omega] \quad (2.10)$$

where

$$R_{dc,TSV} = \rho_{TSV} \times \frac{h_{TSV}}{\pi \times \left(\frac{d_{TSV}}{2}\right)^2} [\Omega]$$

$$\delta_{skin\ depth,TSV} = \frac{1}{\sqrt{\pi f \mu_{TSV} \sigma_{TSV}}} [\text{m}]$$

$$R_{ac,TSV} = k_p \left(\rho_{TSV} \times \frac{h_{TSV}}{2\pi \times \frac{d_{TSV}}{2} \times \delta_{skin\ depth,TSV} - \pi \delta_{skin\ depth,TSV}^2} \right) [\Omega]$$

In addition, there is another effect that induces current flow on the surface of the conductor, but is non-uniformly distributed around the perimeter by attracting currents to the inside-facing surfaces of the conductors, so called “proximity effect” [22]. This effect begins to appear after the skin effect on-set frequency. The proximity factor, k_p , increases as round conducting wires such as TSVs are brought closely together. For TSVs and bumps, the magnitude of the proximity factor, k_p , is determined by the ratio $\frac{\rho_{TSV}}{d_{TSV}}$ or $\frac{\rho_{Bump}}{d_{Bump}}$ [22]. If other TSVs are located near the single-ended signal TSV, then this proximity effect between two TSVs or bumps does not have to be considered. Then, k_p is removed from the proposed equations.

And the calculated R_{TSV} are shown in Fig. 2.14. As shown in Fig. 2.14, the skin effect starts at around several hundred MHz and TSV resistance increases as frequency increases. And TSV resistance is tens of m Ω and this parasitic is less significant than other parasitics of a TSV such as TSV oxide capacitance, silicon substrate capacitance and silicon substrate conductance.

Fig. 2.14 TSV resistance values from the proposed analytic equations of R_{TSV} depending on frequencies up to 20 GHz with the TSV diameter (d_{TSV}) of 10 μm and TSV height (h_{TSV}) of 60 μm

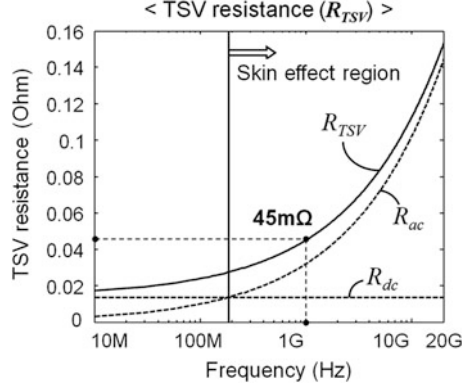
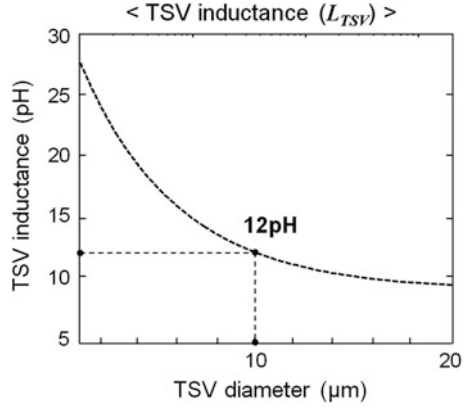


Fig. 2.15 TSV inductance values from the proposed analytic equations of L_{TSV} depending on frequencies up to 20 GHz with the TSV diameter (d_{TSV}) of 10 μm and TSV height (h_{TSV}) of 60 μm



As the operating frequency increases, the impedance of the inductance becomes more dominant than that of the resistance. And, the inductances of the TSV and bump, L_{TSV} and L_{Bump} , are modeled in (2.11) and (2.12) [17, 18].

$$L_{TSV} = \frac{1}{2} \left(\frac{\mu_0 \mu_{r,TSV}}{2\pi} \times h_{TSV} \times \ln \left(\frac{p_{TSV}}{\frac{d_{TSV}}{2}} \right) \right) [\text{H}] \quad (2.11)$$

$$L_{Bump} = \frac{1}{2} \left(\frac{\mu_0 \mu_{r,Bump}}{2\pi} \times h_{Bump} \times \ln \left(\frac{p_{TSV}}{\frac{d_{Bump}}{2}} \right) \right) [\text{H}] \quad (2.12)$$

They are derived from the loop inductance model between two parallel conducting wires. The L_{TSV} and L_{Bump} terms are equivalently separated into the signal and ground TSV/bumps. L_{TSV} and L_{Bump} are also calculated using structural parameters, such as d_{TSV} , p_{TSV} , h_{TSV} , d_{Bump} , and h_{Bump} and material properties, such as the permeability of the TSV, $\mu_{r,TSV}$. L_{TSV} values depending on dimension variations are plotted in Fig. 2.15 based on the proposed equations. As shown in

Fig. 2.15, TSV inductance is 12 pH when diameter of 10 μm and the height of 60 μm which has much lower inductance than the inductance of a bond wire which has nH order.

2.2.2 Simulation and Measurement-Based Verification of the Proposed Equivalent Circuit Model

To verify the proposed scalable model of a TSV channel, S-parameters from the proposed model and a 3D field solver are compared in this section. From the comparison with variations of d_{TSV} , h_{TSV} , and p_{TSV} , the scalability of the proposed model is successfully validated up to 20 GHz. The proposed model is also experimentally validated by fabricating a series of fabricated test vehicles, which include TSVs, bumps, and RDLs.

2.2.2.1 Simulation-Based Verification of the Proposed Scalable Model of a TSV with Bumps

The scalability of the proposed TSV channel model is verified by simulation with the 3D field solver, HFSSTM of Ansoft. Among many design parameters, d_{TSV} , h_{TSV} , and p_{TSV} are swept to validate the scalability of the proposed model up to 20 GHz. As shown in Fig. 2.16, the scalability of the proposed model is successfully verified.

As shown in Fig. 2.16a, the proposed scalable model is verified with d_{TSV} variations. As d_{TSV} varies from 10 to 30 μm , the S_{21} magnitude increases over the entire frequency range. The proposed scalable model estimates the change of the S_{21} magnitude and S_{21} phase well as compared to those computed from the 3D field solver with d_{TSV} variation. Even TSV diameter keeps shrinking as technology advances, TSVs on silicon interposer, which redistribute signals from the chip to the package do not have to be very small whose diameter is under 10 μm . Thus, the variation range of the TSV diameter in this simulation covers the dimension of not only on-chip TSV but also on-interposer TSV.

The proposed model with h_{TSV} variation is also validated, as shown in Fig. 2.16b. As h_{TSV} increases, the insertion loss, as shown by the S_{21} magnitude, increases. These results are due to the increased capacitance and conductance of the silicon substrate, resulting in the decreased impedance between signal and ground TSVs. It makes the insertion loss of the channel increase. The proposed scalable model estimates the S_{21} magnitude and S_{21} phase well as compared to the 3D field solver when h_{TSV} is varied from 30 to 70 μm .

As shown in Fig. 2.16c, the proposed scalable model with p_{TSV} variation is also validated. As p_{TSV} varies from 100 to 140 μm , there is a good agreement between the proposed scalable model and the 3D field solver up to 20 GHz.

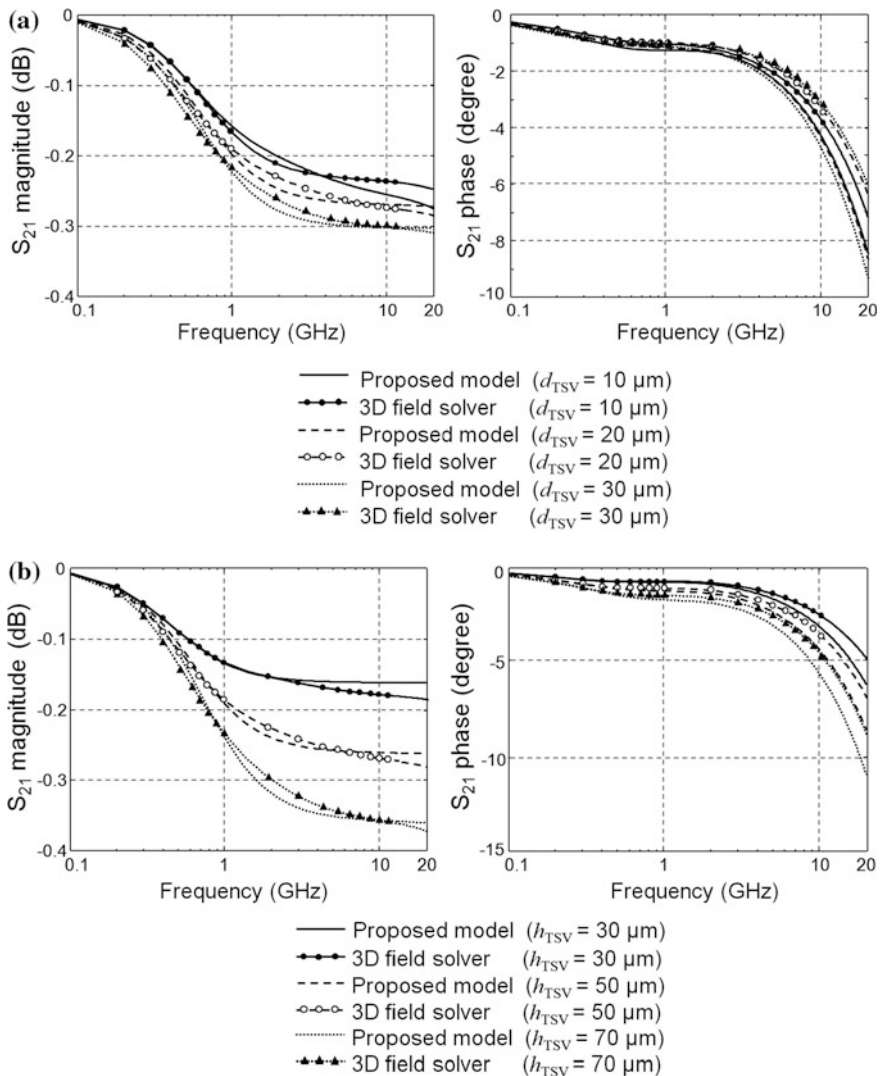


Fig. 2.16 S_{21} magnitudes and phases for the verification of the proposed scalable model of TSVs with bumps by comparing the proposed model to the simulation with a 3D field solver: **a** TSV diameter (d_{TSV}) **b** TSV height (h_{TSV}), and **c** TSV-to-TSV pitch (p_{TSV}). The other TSV and bump dimensions are fixed as d_{TSV} of 30 μm , h_{TSV} of 50 μm , p_{TSV} of 100 μm , t_{ox} of 0.5 μm , d_{Bump} of 50 μm , h_{Bump} of 10 μm , and h_{IMD} of 10 μm [15] © 2011 IEEE

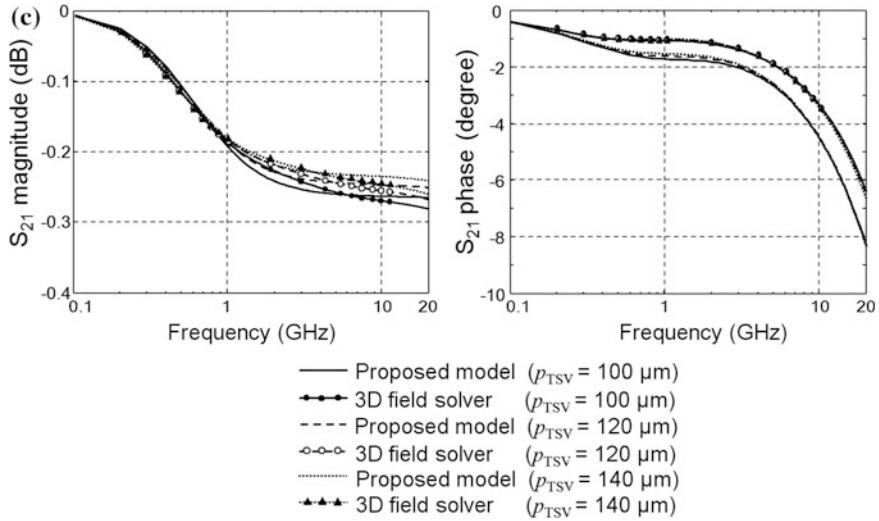


Fig. 2.16 continued

It should be observed, however, that there is an additional inductive effect from the inductance of the lumped ports when simulating with the 3D field solver, which causes increments of the slope of the S_{21} magnitudes over 10 GHz. Thus, there are some discrepancies between the calculated results from the proposed model and the simulation results from the 3D field solver over 10 GHz, as shown in Fig. 2.16a–c.

2.2.2.2 Experimental Verification of the Proposed Model of a TSV with Bumps and RDLs

To experimentally verify the proposed model, TSV channels are fabricated as for the test vehicles. The top view and the cross-sectional view of the fabricated TSV channel are shown in Fig. 2.17a, b, respectively. In order to measure the insertion loss through the TSV channel, TSVs are connected by stacking two dies. And the detailed dimensions are shown in Fig. 2.17c. There are two pairs of signal and ground TSVs on each side and each pair are connected each other by RDLs which are fabricated on the of the bottom die.

For the S-parameter measurements, on-chip cascade probes and a vector network analyzer (VNA), the Agilent N2530A, are used. Measurement results are compared to those from the proposed equivalent circuit model of the fabricated test vehicle.

The comparisons of the magnitudes and phases of both the S_{21} and S_{11} from the proposed model and measurement are shown in Fig. 2.18. The proposed model and the measurement are well correlated up to 20 GHz. As a result, we

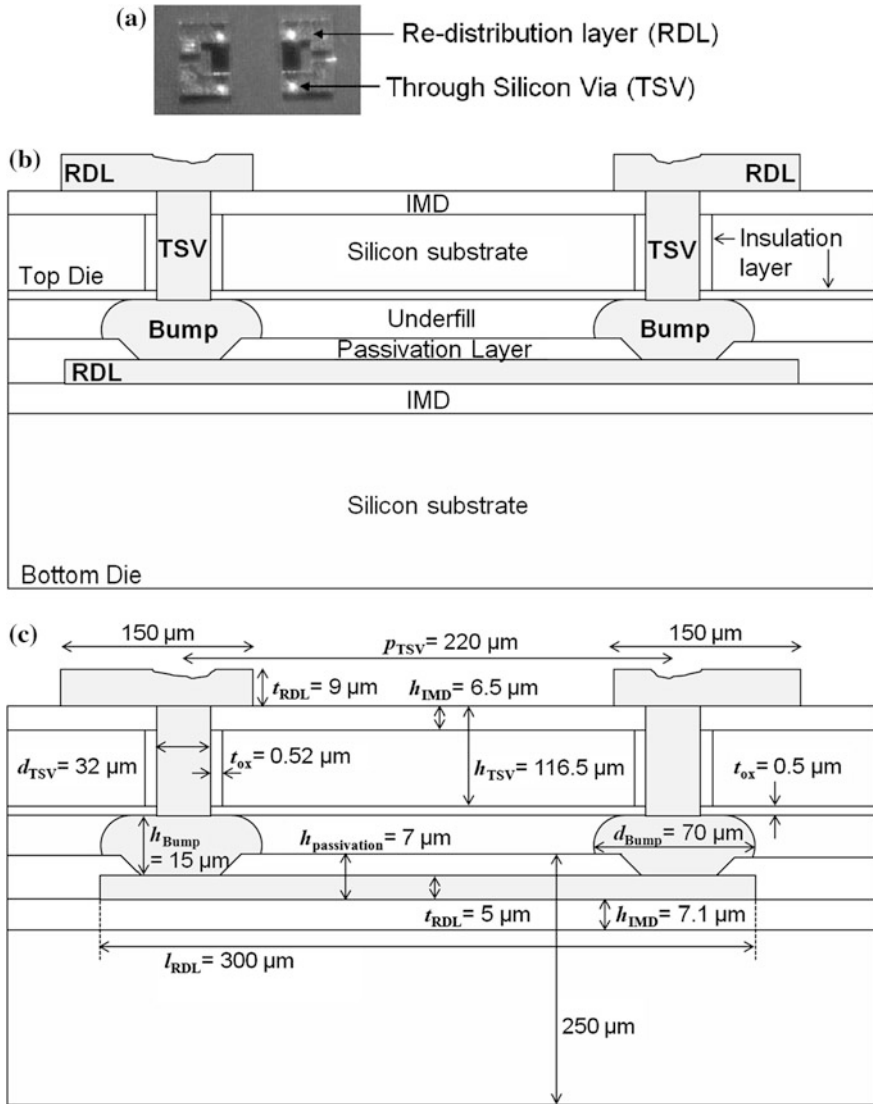


Fig. 2.17 a A top-view photograph of the test chip b the cross-sectional view and c the detail dimensions of the fabricated test vehicle, which is the TSV channel including the TSVs, bumps, and RDLs. The RDL on the bottom die provides horizontal connection between TSVs on the top die [15] © 2011 IEEE

experimentally verified the proposed electrical model of the TSV channel. It should be noted that the model for the verification includes the mutual effect between two TSV pairs on the top die.

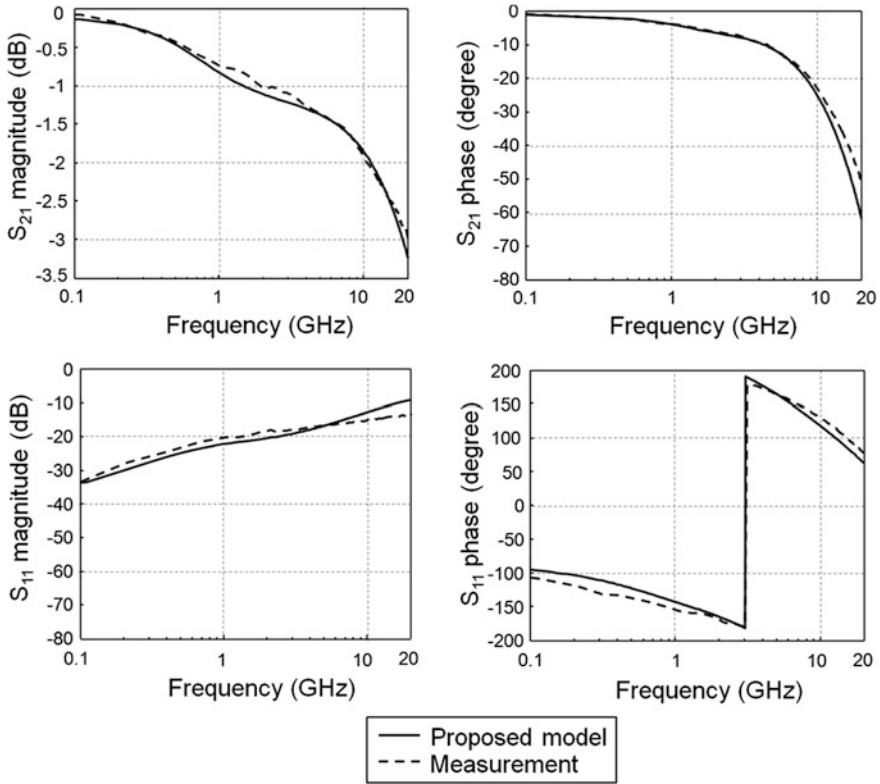


Fig. 2.18 Verification of the proposed model by comparing the measured S parameters with the calculated S parameters from the model [15] © 2011 IEEE

With the verified model, the electrical behavior of a TSV channel can be analyzed; the proposed analytic and closed-form equations can be used to estimate the power consumption, propagation delay, and timing skew of a TSV channel. The equations can also be combined with other circuits to evaluate the signal performance in 3D IC design. Since the model is scalable, it can estimate the electrical behavior depending on design parameters.

In Sect. 2.3, the electrical characteristics of the TSV channel are analyzed with the experimentally verified scalable model. Since the proposed model has scalability, the impact of each design parameter on the electrical behavior of the TSV channel can be easily analyzed. Then, the dominant *RLGC* components are analyzed which dominantly determine the insertion losses of the TSV channel in different frequency ranges.

2.3 Electrical Characterization and Analysis of a TSV Channel

In this section, the electrical characteristics of a TSV channel are analyzed with the proposed scalable equivalent circuit model, which is experimentally verified in Sect. 2.2.2.2. The configuration of the TSV channel, which is used for the analysis in this section, is the same as that of the fabricated test vehicle. The TSV channels are analyzed as varying t_{ox} , d_{TSV} , p_{TSV} , h_{TSV} , RDL length (l_{RDL}), and σ_{Si} . In the frequency-domain analysis, the dominant design parameters are determined in specific frequency ranges by analyzing the insertion losses with S_{21} magnitudes. In addition, the frequency-dependent loss of the TSV channel is analyzed by categorizing the measured frequency range into three parts: region [A] for 0–2 GHz, region [B] for 2–10 GHz and region [C] for 10–20 GHz. In addition, eye diagram measurements with data rates up to 10 Gbps are conducted for the time-domain analysis of the TSV channel.

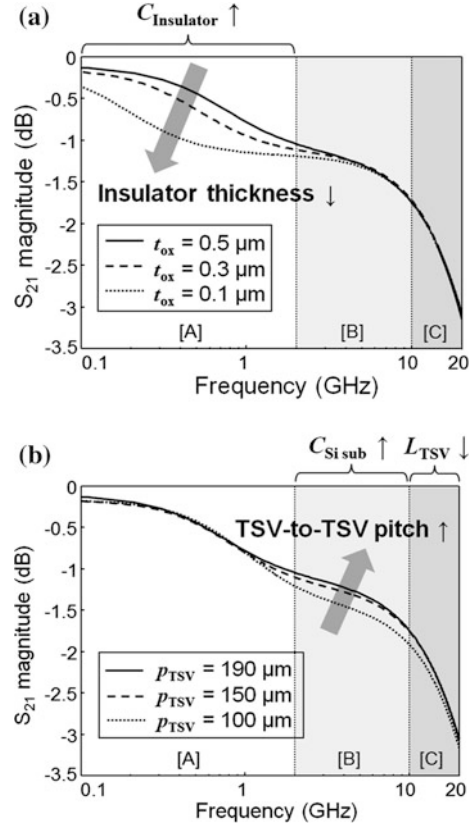
2.3.1 Frequency-Domain Analysis for Electrical Characterization of a TSV Channel

For the TSV structure, an insulation layer has to be formed to isolate the TSV from the conductive silicon substrate. The capacitance, $C_{Insulator}$ is directly affected by variation in t_{ox} which is explained in the proposed equation in Sect. 2.2.1. Thus, $C_{Insulator}$ increases as t_{ox} decreases. As t_{ox} decreases from 0.5 to 0.1 μm , $C_{Insulator}$ increases from 0.8 pF to 3.9 pF. The insertion loss through the TSV is dominated by the leakage through the conductive silicon substrate after passing through the insulator. As a result, an increase of $C_{Insulator}$ results in increased insertion loss due to the lowered impedance along the leakage path to the silicon substrate given by the equation, $Z = 1/j\omega C$. Therefore, the insertion loss through a TSV can be reduced by increasing the thickness of the insulator.

However, with current technology to form an insulation layer around a TSV, the thickness of the insulator, which is generally SiO_2 , is limited to under 0.5 μm . This is due to process limitations in oxidizing a via with a high aspect ratio, which is also related to cost. In addition, the value of $C_{Insulator}$ is relatively big as compared to that of other parasitic capacitances of a few fF such as the $C_{Underfill}$, C_{IMD} , and C_{Bottom} . In a similar manner, if the thickness of the bottom oxide, $t_{ox,bot}$, decreases, the impedance of C_{Bump2} rapidly decreases as frequency increases. With $t_{ox,bot}$ of 0.5 μm , C_{Bump2} is 0.2 pF. Thus, if $t_{ox,bot}$ decreases and d_{Bump} increases, C_{Bump2} can bring more significant impact than $C_{Insulator}$ in region [A].

Therefore, the capacitive effect due to the insulation layer dominates the capacitive characteristic in the low frequency range, region [A], as shown in Fig. 2.19a. In this region, the insertion loss rapidly increases as frequency increases due to the decreasing impedance of $C_{Insulator}$.

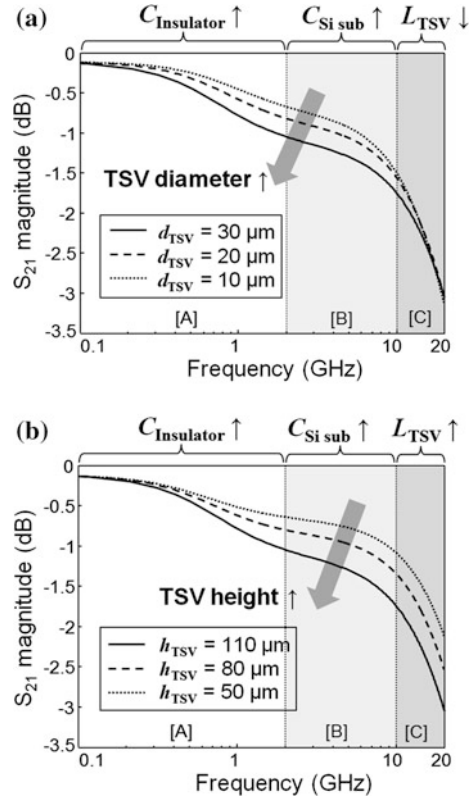
Fig. 2.19 S_{21} magnitudes from the proposed equivalent circuit model of a TSV channel with (a) TSV Insulator thickness variation and (b) TSV-to-TSV pitch variation [15] © 2011 IEEE



In addition, there is another loss term from the silicon substrate under the RDL, G_{sub} [15]. It also contributes to the insertion loss through the TSV channel. If the height between the RDL and the silicon substrate becomes smaller and the length of the RDL increases, the effect from G_{sub} increases [23, 24]. Thus, the resistive losses from the RDL itself and the silicon substrate under the RDLs become significant as the length of the RDL increases beyond a mm, and the width and thickness of the RDL decreases in 3D IC design. The significant factor that determines the amount of resistive loss through a TSV is the silicon substrate because it is conductive and TSVs are formed passing through it vertically.

There is one another resistive loss factor from the TSV itself, R_{TSV} . The resistive loss from R_{TSV} , in the case that it is made from copper, is negligible due to the comparatively small value of resistance, which is a few $\text{m}\Omega$. If the metal filling the TSV is tungsten or poly silicon, which has a higher resistivity than copper, the resistive loss due to R_{TSV} will contribute more to the overall resistive loss through the TSV interconnect. There is no significant change in the insertion loss for region [C], even with the decrease of p_{TSV} resulting in an increase of $C_{\text{Si sub}}$ and $G_{\text{Si sub}}$, which dominantly affect the loss term. This is due to the decrease in inductances

Fig. 2.20 S_{21} magnitudes from the proposed equivalent circuit model of a TSV channel with (a) TSV diameter variation and (b) TSV height variation [15]
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such as L_{TSV} , L_{Bump} , and L_{RDL} , as p_{TSV} decreases. A decrease in the inductance of the TSV channel reduces the insertion loss in region [C]. Thus, the effects on the insertion loss from the decreased inductance and increased $C_{Si sub}$ and $G_{Si sub}$ compensate each other in region [C] and make the loss steady even with the p_{TSV} varying. As a result, pitch variation dominantly affects the electrical characteristic of a TSV channel in region [B]. In addition, this effect is gradually reduced as frequency increases over 10 GHz due to the increased inductance effect from the TSVs, bumps, and RDLs.

Variation in d_{TSV} changes almost all the $RLGC$ components of the proposed equivalent circuit model of a TSV channel. With increasing d_{TSV} , the effective distance between the signal and ground TSV decreases, when p_{TSV} is fixed. Therefore,

$C_{Si sub}$ and $G_{Si sub}$ increase, which increases the insertion loss. In addition, $C_{Insulator}$ increases due to an increase of the effective area where the TSV faces the silicon substrate through the insulation layer. Therefore, overall insertion loss in region [A] and [B] increases as d_{TSV} increases, as shown in Fig. 2.20a.

In a similar manner with the previous analysis for p_{TSV} variation, the decreased inductance effect from L_{TSV} , which makes the insertion loss constant even with the

increase of $C_{Si\ sub}$ and $G_{Si\ sub}$, is shown in region [C], Fig. 2.20a. As d_{TSV} increases from 10 to 30 μm , L_{TSV} decreases from 20.8 pH to 14.7 pH. Thus, there are no big insertion loss changes even with d_{TSV} variation in region [C]. In addition, R_{TSV} also decreases as d_{TSV} increases. However, this resistance is too small to be considered as discussed in the previous analysis for p_{TSV} variation.

Thus, the overall characteristic of the TSV channel with d_{TSV} increasing results in the increased insertion loss, which is dominantly determined by $C_{Si\ sub}$ and $G_{Si\ sub}$. In summary, d_{TSV} affects the frequency dependent loss of the TSV channel in almost all frequency ranges, but is dominant in regions [A] and [B].

As shown in Fig. 2.20b, the insertion loss of the TSV channel increases in all frequency ranges as h_{TSV} increases from 50 to 110 μm , because it not only increases $C_{Insulator}$ and $C_{Si\ sub}$, but also increases L_{TSV} . Therefore, the increasing h_{TSV} increases the insertion loss in all frequency ranges, regions [A], [B], and [C].

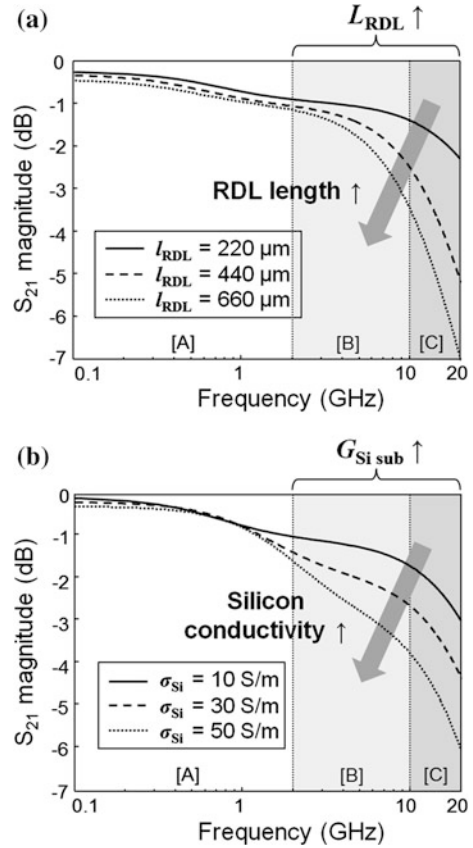
In a similar manner to the analysis of t_{ox} variation, $C_{Insulator}$ dominantly affects the insertion loss in region [A]. In region [B], $C_{Si\ sub}$ and $G_{Si\ sub}$ are the dominant factors that determine the insertion loss as analyzed for both p_{TSV} and d_{TSV} . In region [C], the inductances of the TSV channel start to affect the insertion loss.

As shown in Fig. 2.21a, as length of the RDL, l_{RDL} , increases from 220 to 660 μm , the insertion losses in regions [B] and [C] increase due to an increase in the inductance and the resistance of the RDL, L_{RDL} and R_{RDL} . From this analysis, it is apparent that regions [B] and [C] are dominantly affected by the inductive characteristic of the RDL. As l_{RDL} increases from 220 to 660 μm , L_{TSV} increases from 150 pH to 452 pH. As the operating frequency increases over a few Gbps, the RDL routing becomes a critical design issue for high-speed 3D IC channel design to guarantee the signal quality of the channel.

Silicon conductivity, σ_{Si} , is a material property that has a considerable influence on the electrical characteristics of the TSV channel. Because it changes $G_{Si\ sub}$ and G_{sub} , which determines overall insertion loss of a TSV channel. As σ_{Si} increases from 10 S/m to 50 S/m, $G_{Si\ sub}$ increases from 1.4 mS to 6.98 mS. As a result, the insertion loss of the TSV channel increases. The σ_{Si} change does not dominantly affect the insertion loss in region [A], however, in regions [B] and [C], it does. Therefore, the important design parameters of the TSV channel in 3D IC are not only the physical parameters but also the material properties.

In summary, the electrical characteristics of the TSV channel are analyzed with insertion loss data up to 20 GHz. The TSV channel has capacitive and resistive characteristics, and is also frequency dependent. The overall loss of the TSV channel is determined to be dominated by the conductance of the silicon substrate. If the RDL length increases to the mm range, the RDL contributes significantly to the loss of the TSV channel. The overall electrical behavior has a capacitive characteristic from the parasitic capacitances whose impedances change as frequency varies. However, the frequency dependence is determined to be dominated by the parasitic inductances of the TSV channel over 10 GHz. As a result, the capacitive TSV effect is dominant in the lower frequency range, and the inductive RDL effect becomes dominant in the higher frequency range.

Fig. 2.21 S_{21} magnitudes from the proposed equivalent circuit model of a TSV channel with (a) RDL length variation and (b) conductivity of the silicon substrate [15]
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With these analyses, we summarize the design parameters and $RLGC$ components which have a major impact on the frequency dependent loss of the TSV channel. As shown in Fig. 2.22, there are design parameters which dominantly determine the frequency dependent loss of the TSV channel; t_{ox} , $t_{ox,bot}$ and d_{TSV} in region [A], p_{TSV} and h_{TSV} in region [B], h_{TSV} and l_{RDL} in region [C]. Additionally, the dominant $RLGC$ components of the proposed model of the TSV channel are summarized; $C_{Insulator}$ in region [A], $C_{Si\ sub}$ in region [B], L_{TSV} and L_{RDL} in region [C]. Other $RLGC$ components which have a minor impact in each frequency range are summarized; C_{Bump2} have a minor impact in region [A], $C_{Underfill}$, C_{IMD} , C_{Bottom} , C_{RDL} , $C_{RDL_to_sub}$ and C_{sub} , have a minor impact in region [B] and [C] [15].

2.3.2 Time-Domain Analysis of a TSV Channel

For the time-domain analysis, eye diagram measurements are conducted on the fabricated TSV channel, which includes the TSVs, bumps, and RDLs. The input

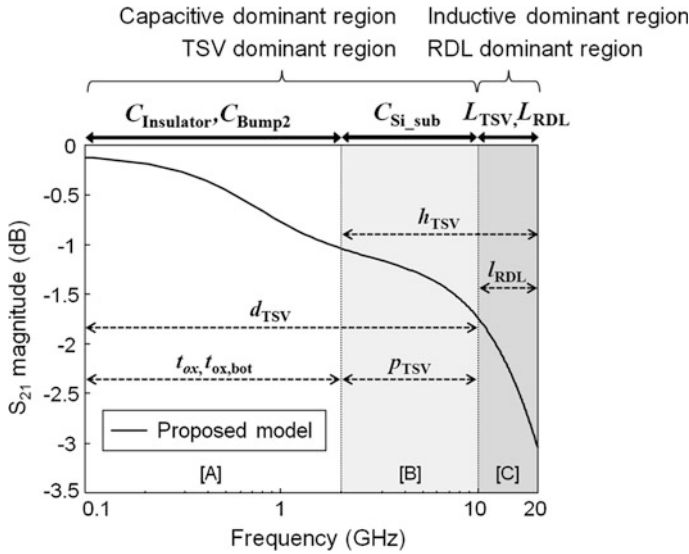


Fig. 2.22 S_{21} magnitude from the proposed model showing dominant design parameters and $RLGC$ components, which determine the insertion loss for the different frequency ranges: in the lower frequency range, the capacitive TSV effect dominates; in the higher frequency ranges, the RDL effect, which is inductive, becomes dominant [15] © 2011 IEEE

signal is a $2^{31} - 1$ pseudo-random bit sequence with an amplitude of 500 mV_{p-p}. The output waveforms are monitored using a digital sampling oscilloscope, Tektronix/TDS8000B, equipped with a 20 GHz sampling module.

The eye diagrams from the measurement and the proposed model with data rates of 1 Gbps, 5 Gbps, and 10 Gbps with random data of $2^{31} - 1$ bits transmitting through the fabricated TSV channel are shown in Fig. 2.23. The shapes of the eye diagrams from the measurement and the proposed model are matched well. However, there are some differences in the eye opening and the pk-pk jitter between the measurement and the proposed model. Those differences are due to the cables used for the measurement that bring additional 1.4 dB, 3.6 dB, and 4.3 dB losses at 500 MHz, 2.5 GHz, and 5 GHz, respectively. Therefore, the eye openings with 1 Gbps, 5 Gbps and 10 Gbps random data are smaller than that from the proposed model by several tens of mV.

In addition, the measured pk-pk jitter is larger than that from the proposed model by 6–7 ps, because there is random jitter produced from the measurement equipment, the pulse pattern generator (PPG), and jitter additionally caused by the two cables used for the measurements.

From the measured eye diagrams in Fig. 2.23, as the data rate increases, the voltage and timing margins decrease, which are presented with the normalized eye-opening and pk-pk jitter. The normalized eye-opening and pk-pk jitter are 83.4 % and 0.8 %, respectively, for data rates of 1 Gbps. As the data rate is increased to 5 Gbps and 10 Gbps, the normalized eye-opening decreases to 70.6 %

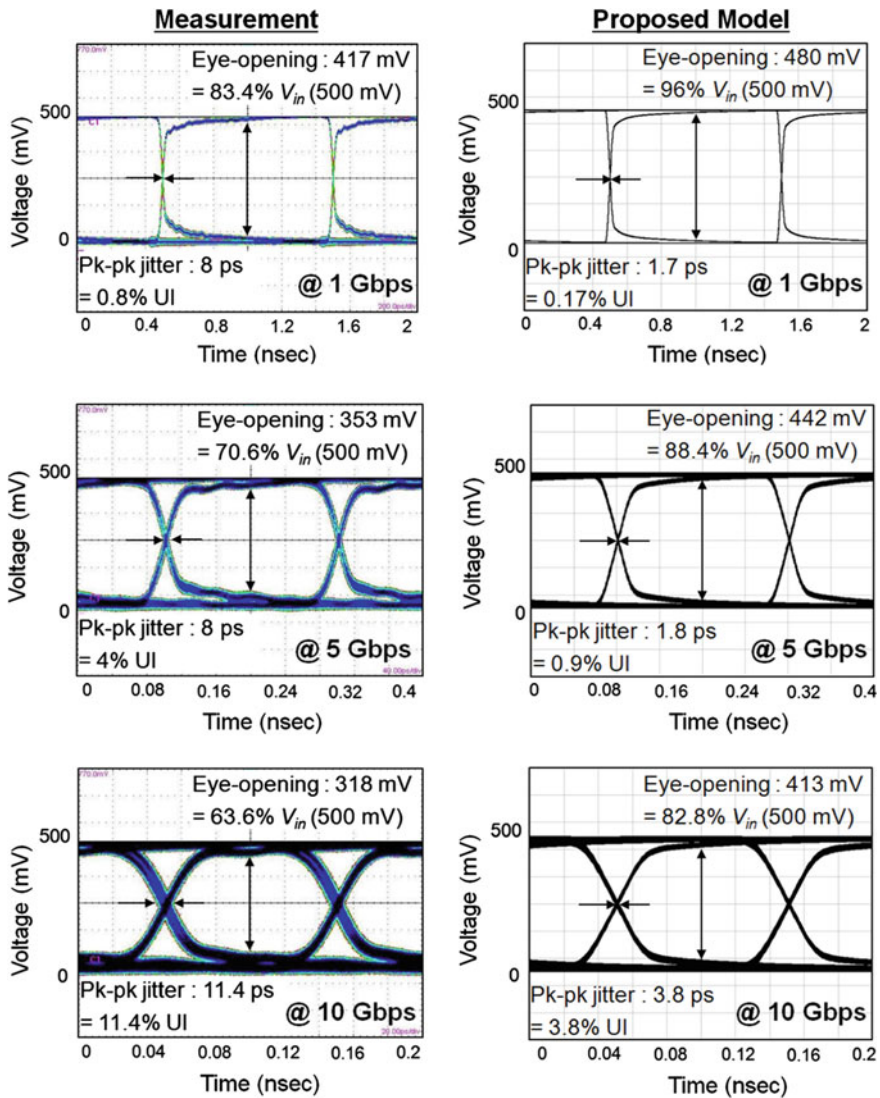


Fig. 2.23 Eye diagrams from the measurement and the proposed model with 1, 5, and 10 Gbps random data of $2^{31} - 1$ bits traveling through the fabricated TSV channel. As the data rate increases, the normalized eye opening decreases and the normalized pk-pk jitter increases due to the frequency dependent loss of the TSV channel, which are capacitive and resistive [15] © 2011 IEEE

and 63.6 % and the normalized pk-pk jitter increases to 4 % and 11.4 %. Signals through the TSV channel, however, have open eyes because of the short inter-connection length of the TSV and RDL, even with a data rate of 10 Gbps.

Since the TSV channel has capacitive and resistive characteristics as analyzed in Sect. 2.3.1 on the frequency-domain analysis, it has a frequency dependent loss. In addition, because the energy of the signal is predominantly concentrated at the Nyquist frequency, the insertion loss is not constant in frequency domain, however, increases as the data rate increases. Thus, the amount of signal degradation through the TSV channel increases as the frequency increases. For example, the energy of the signal with a data rate of 1 Gbps is mostly concentrated at 0.5 GHz. From the measurement results, the insertion loss at 0.5 GHz for the TSV channel is -0.5 dB. However, with a data rate of 10 Gbps, the TSV channel has insertion loss at the Nyquist frequency, 5 GHz, of -1.5 dB. Thus, the frequency dependent loss in the frequency domain directly results in the increase of the rise time of the signal in the time domain as operating frequency increases. Furthermore, if the frequency dependent loss of the TSV channel becomes severe, it can cause inter-symbol interference (ISI), which is the signal degradation of the timing and signal integrity margins.

However, as 3D integration density increases, the number of dies, which have to be vertically integrated in one system, increases. Thus, high-speed I/O signals pass through many TSVs. This can cause an additional capacitive load due to the increasing parasitic capacitances of the TSVs. It results in an increased timing delay, lowered slew rate and increased timing jitter of the signal. Based on the model and analysis of the TSV channel in the previous sections, as d_{TSV} and h_{TSV} becomes smaller or t_{ox} becomes thicker, the capacitive load due to the TSV can be reduced. Therefore, we can sharpen the rising edge of the signal for better system performance and increases the bandwidth of the TSV interconnect by optimizing d_{TSV} , h_{TSV} , and t_{ox} . In a similar manner, if there are more than two RDL layers and are densely routed, the capacitive load from the RDLs also increases and it will significantly affect to the overall signaling performance of the channel. In order to optimize the RDL design, it is necessary to minimize the capacitance due to RDLs by reducing w_{RDL} , increasing S_{RDL} , and minimizing the routed length of RDLs.

Since 3D IC design has still challenging issues in terms of yield and cost, many of industries currently focus on 2.5D integration using a silicon interposer which is a marginal silicon die enabling 2-dimensional multi-chip integration on a silicon die and provides RDLs as for the chip-to-chip interconnect on die and TSVs in order to redistribute the pins from the integrated chips to the package and the printed circuit board. In this case, the portion of RDLs along the 3D IC channel is very significant, and the length of RDLs has several mm order which may result in a severe signal degradation due to the increased RC delay, insertion loss and crosstalk effect. Therefore, the impact on high-speed signaling, I/O power consumption and routability issues from the RDL design have to be also carefully concerned for the advanced 3D IC channel design.

Eye diagrams which are computed with the proposed model are shown in Fig. 2.24, for signals passing through a different number of TSV pairs and RDLs. As the number of TSVs that the signal is traveling increases from two to eight, and the length of RDL increases from 500 to 2 mm, the eye-opening decreases 10 % and the pk-pk jitter increases 0.2 %. We can confirm the effect from the increased

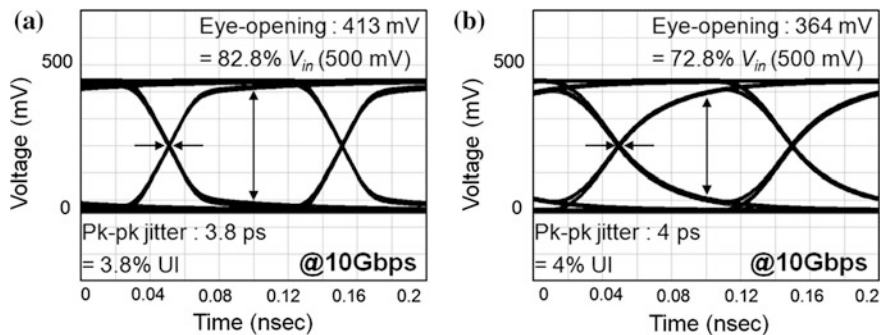


Fig. 2.24 Eye diagrams of the proposed model with 10 Gbps pseudo-random data traveling through (a) two TSV pairs and RDLs; and (b) eight TSV pairs and RDLs [15] © 2011 IEEE

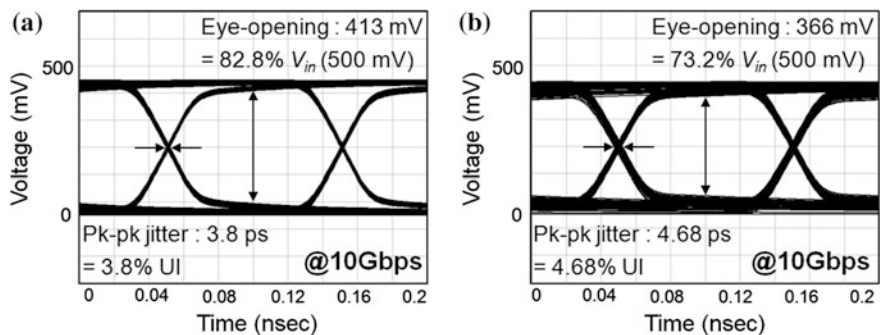


Fig. 2.25 Eye diagrams of the proposed model with 10 Gbps random data traveling through two TSV pairs and RDLs with (a) t_{ox} of 0.5 μm ; and (b) t_{ox} of 0.1 μm [15] © 2011 IEEE

capacitance of the TSV channel with these computed eye diagrams from the proposed model. Even though the eye is still clearly open, if the coupling ratio among the TSVs increases significantly or the RDL coupling increases from the long and dense routing, the eye can become more degraded.

In addition, as analyzed in the frequency-domain analysis, if the thickness of the insulator, t_{ox} , becomes thinner, the insertion loss of the low frequency components, especially under 2 GHz, increases, even though the high frequency components almost does not change. Hence, as shown in Fig. 2.25, the slope of the rising edge, where the high frequency components are concentrated, does not change, when the t_{ox} is decreased from 0.5 to 0.1 μm .

Therefore, we analyzed and confirmed the frequency-dependent loss of a TSV channel in the time domain, which was characterized in the frequency domain in Sect. 2.3.2 (Fig. 2.26).

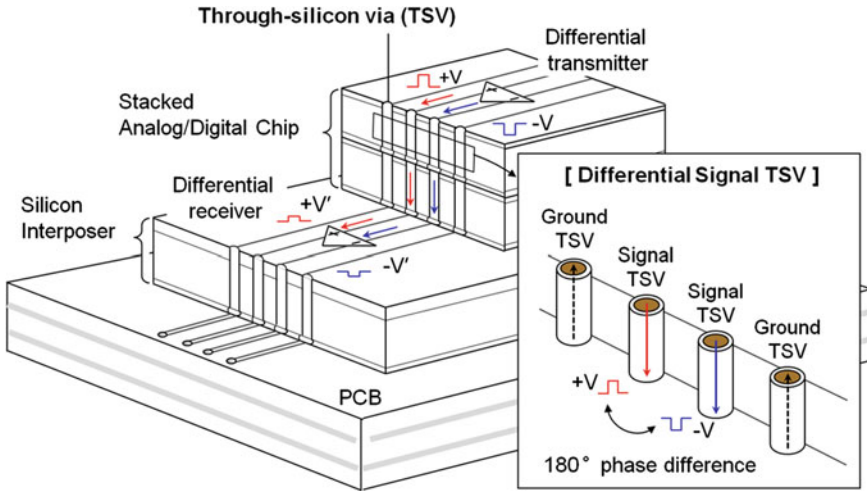


Fig. 2.26 A conceptual 3-dimensional integrated circuit (3D IC), which includes vertical integration of dies with differential signal through-silicon vias (TSVs). For differential signaling, there are two signal TSVs, which transfer the signals with the same amplitude but are out-of-phase [25]

2.4 Electrical Analysis of a Single-Ended and Differential Signal TSV Channel

For reliable high-speed signaling with high noise immunity, a differential signaling scheme is generally preferred for higher system performance than a single-ended signaling scheme. However, based on the simulation results from Sect. 2.3.2, differential signal TSVs also have frequency-dependent loss and capacitive-dominant characteristics, which can degrade the high-speed signal transmission. Thus, a differential signaling scheme (GSSG-type) is compared to a single-ended signaling scheme (GSG-type) by analyzing the insertion loss, characteristic impedance, TDR waveform, and eye diagram in this section. Then, the pros and cons of using differential signaling rather than single-ended signaling with TSVs are analyzed.

For the differential signaling scheme, a GSSG-type differential signal TSV is modeled and analyzed in this paper. The electrical behavior is compared with a single-ended signaling scheme by selecting a GSG-type configuration. The dimensions and material properties of the TSVs, bumps, and metal lines are described in Tables 2.1 and 2.2. The top views of the fabricated test vehicles of the GSSG-type and GSG-type are illustrated in Fig. 2.27. The performance analysis and comparison are conducted with frequency domain measurements including insertion loss and characteristic impedance, and time domain measurements such as a TDR waveform and eye diagram of the two signaling schemes.

Table 2.1 Design parameters and the corresponding dimensions of the fabricated differential signal TSV [25]

Design parameter	Dimension (μm)
TSV diameter (d_{TSV})	45
TSV height (h_{TSV})	60
TSV oxide thickness (t_{ox})	0.25
TSV-to-TSV pitch (p_{TSV})	250
Bump diameter (d_{bump})	120
Bottom metal line length (l_{RDL})	360
Bottom metal line width (w_{RDL})	100
Metal line thickness (t_{RDL})	2
Metal via diameter	30
Metal via height	4
Metal pad diameter	40
Metal pad thickness	2

Table 2.2 Material parameters with symbols and values for the fabricated differential signal TSV [25]

Material parameter	Value
Conductivity of Silicon substrate (σ_{Si})	10 (S/m)
Resistivity of TSV (ρ_{TSV})	1.68×10^{-8} ($\Omega\cdot\text{m}$)
Resistivity of bump (ρ_{Bump})	1.09×10^{-7} ($\Omega\cdot\text{m}$)
Resistivity of RDL (ρ_{RDL})	1.68×10^{-8} ($\Omega\cdot\text{m}$)
Relative permittivity of Silicon substrate ($\epsilon_{r, si}$)	11.9
Relative permittivity of insulator ($\epsilon_{r, Insulator}$)	4
Relative permittivity of IMD ($\epsilon_{r, IMD}$)	2.6
Relative permittivity of underfill ($\epsilon_{r, Underfill}$)	1
Relative permeability of TSV ($\mu_{r, TSV}$)	1
Relative permeability of bump ($\mu_{r, Bump}$)	1
Relative permeability of RDL ($\mu_{r, RDL}$)	1

2.4.1 Frequency-Domain Measurement and Analysis of Single-Ended and Differential Signal TSV Channel

Figure 2.28 shows the measured insertion losses, which are differential mode S_{21} magnitude for a differential signal TSV and S_{21} magnitude for a single-ended signal TSV up to 20 GHz. From comparing the results, we noticed that the GSSG-type has larger insertion loss than that of the GSG-type over almost all of the frequency range up to 20 GHz. This difference is due to the equivalent capacitance and conductance difference that a signal encounters. Because a silicon substrate has losses, if the capacitance and conductance of the silicon substrate increase, the insertion loss increases. For the GSG-type, a signal TSV has two ground TSVs near a signal TSV with a pitch of p_{TSV} . However, for the GSSG-type, the mutual capacitance and conductance between the signal TSVs is effectively double the value of the GSG-

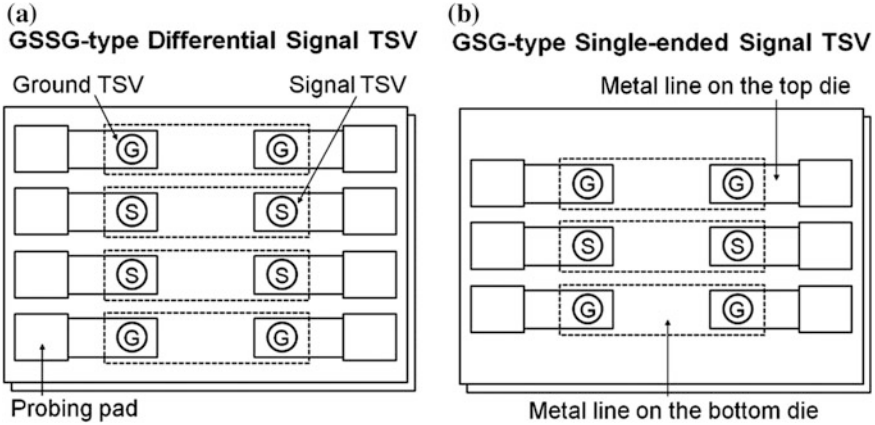
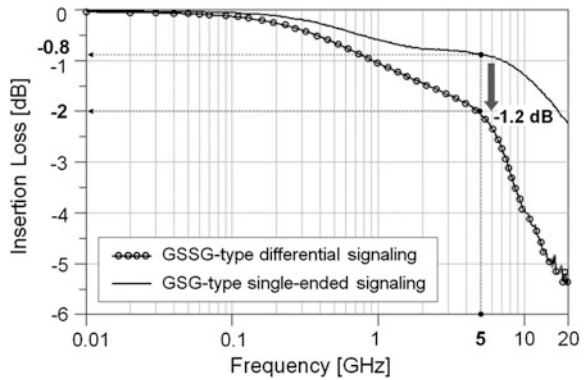


Fig. 2.27 Top view of the fabricated test vehicles of a (a) GSSG-type differential signal TSV and (b) GSG-type single-ended signal TSV for performance comparison and analysis. Two dies are stacked to connect the TSVs on the top die with metal lines on the bottom die [25]

Fig. 2.28 Insertion losses from measured differential-mode S_{21} magnitude of the GSSG-type differential signal TSV and S_{21} magnitude of the GSG-type single-ended signal TSV up to 20 GHz. At 5 GHz, insertion loss of the GSSG-type is 1.2 dB larger than that of the GSG-type [25]

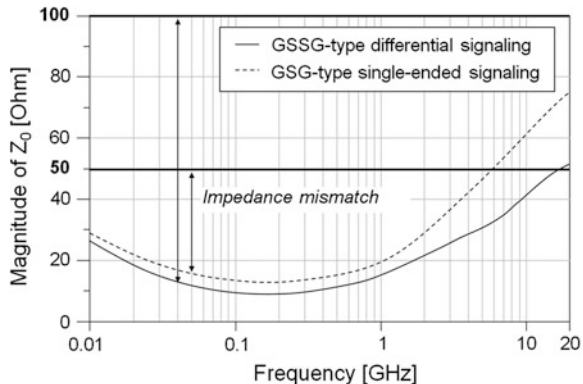


type due to the virtual ground effect. Thus, the GSSG-type has a larger capacitance and conductance than GSG-type. Thus, the GSSG-type has 1.2 dB larger insertion loss than the GSG-type at 5 GHz.

Next, we analyze the characteristic impedances from both signaling schemes. The characteristic impedance is computed from the measured S-parameters in Fig. 2.29.

From the Fig. 2.29, the odd-mode impedance of the GSSG-type has lower characteristic impedance than the GSG-type for all frequencies. This phenomenon is because the GSSG-type has a larger equivalent capacitance and conductance than the GSG-type. Since there is a virtual ground between two signal TSVs in case of differential signaling, the effective parasitic capacitance to the ground which affects to the loading capacitance for the signal is larger than the

Fig. 2.29 The characteristic impedances of a GSSG-type differential signal TSV and a GSG-type single-ended signal TSV and the amount of the impedance mismatches from 100 Ohm for the differential signaling and 50 Ohm for the single-ended signaling [25]



single-ended signaling case. Additionally, the characteristic impedances of the GSSG-type and the GSG-type are less than 100 Ohm and 50 Ohm, respectively. Because a TSV has a thin insulation layer surrounding a via and has a short height, the capacitive characteristic of a TSV is more dominant than the inductive factor on the overall electrical behavior of a TSV. In terms of the characteristic impedance of TSV channels, even there's a large impedance mismatch due to TSVs along the channel, it does not result in serious signal degradation since the electrical length of a TSV is short enough.

However, if the operating frequency increases to hundreds of GHz and the number of stacked dies increases, the impact of the impedance mismatch cannot be ignored any more since the TSV channel becomes electrically long enough which has to be considered as a transmission line. The impedance of a differential signal TSV and a single-ended signal TSV can be controlled by optimizing the design parameters of a TSV. For example, a TSV with smaller via diameter, thinner oxide thickness, longer TSV-to-TSV pitch and shorter via height has the higher characteristic impedance. These design guidelines are the way to decrease the parasitic capacitance and also to increase the parasitic inductance of a TSV. Since the characteristic impedance varies as frequency increases, it is necessary to consider the Nyquist frequency of the target data when determining the target characteristic impedance of the TSV channel in order to minimize the impact of the impedance mismatch.

2.4.2 Time-Domain Measurement and Analysis of Single-Ended and Differential Signal TSV Channel

In this section, time-domain measurement and analysis of single-ended and differential signal TSV channel are presented with eye diagram and TDR measurements. In real design phases, the maximum timing and voltage margins of the channel are specified and have to be evaluated in order to guarantee the system

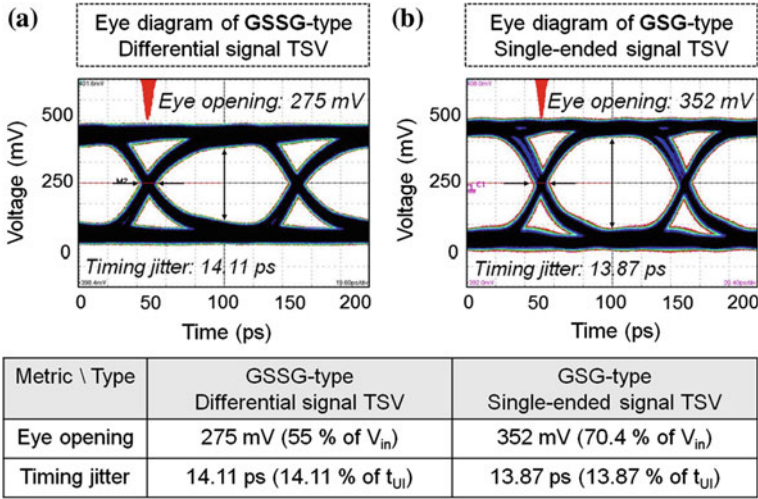


Fig. 2.30 Eye diagrams from measurements with a 10 Gbps pseudo-random bit sequence (PRBS) of data with $2^{31} - 1$ bits traveling through (a) the GSSG-type single-ended signal TSV and (b) the GSG-type differential signal TSV of the fabricated test vehicles. The measured eye diagram includes the cable effect [25]

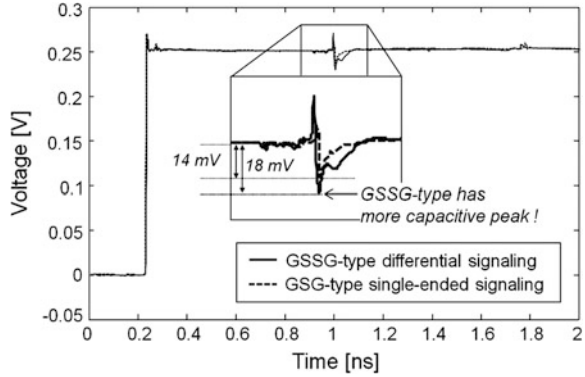
operation. Thus, it is necessary to analyze and evaluate the impact of the channel performance in time domain to meet the system requirements.

Based on the previous discussions on the frequency-domain analysis, it can be expected that the eye-diagrams of the signal passing through the GSSG-type differential signal TSV is worse than that of GSG-type single-ended signal TSV as shown in Fig. 2.30. The eye diagram is measured with 10 Gbps pseudo-random bit sequence (PRBS) of data with $2^{31} - 1$ bits with a PPG and TDS 8000B. For the GSG-type, eye opening and timing jitter are 352 mV and 13.87 ps, respectively. For the GSSG-type, eye opening and timing jitter are 275 mV and 14.11 ps, respectively, which is a tighter voltage and timing margin than the GSG-type.

From the TDR waveforms, we can compare the capacitive or inductive characteristics of the channel. Figure 2.31 includes the measured TDR waveforms from the GSSG-type and the GSG-type. For the TDR measurements with GSSG-type, differential step pulses are injected, which have the same amplitudes but are out-of-phase, to obtain the differential reflected voltages. The straight line in Fig. 2.31 shows the TDR waveform from the GSSG-type and the dotted line shows that from the GSG-type. The capacitive peak from the GSSG-type is lower than that from the GSG-type. Thus, we confirm that the equivalent capacitance of the differential signal TSV (GSSG-type) is greater than that of the single-ended signal TSV (GSG-type), which was previously discussed in the modeling section.

Next, the coupled noise voltages with the GSSG-type and the GSG-type are measured. Figure 2.32 illustrates the top view of the fabricated samples for the measurements. The thinned dies with two pairs of GSSG-type and two pairs of

Fig. 2.31 TDR waveforms from the time-domain measurements with a 500 mV p-p step pulse with the GSSG-type differential signal TSV (*straight line*) and the GSG-type single-ended signal TSV (*dashed line*) [25]



GSG-type signal TSVs are fabricated. The dimensions of the structure are the same as those from the previous samples. However, the die is not stacked but is instead thinned to make TSVs open-ended.

For the measurement of a GSSG-type, differential clock signals with 250 mV peak-to-peak amplitude that are out-of-phase are used for the noise source at the aggressor, which is a pair of GSSG-type. The coupled noise voltages are measured at the opposite side of a GSSG-type signal TSV pair. Then, we subtract output voltages from the two signal TSVs of a GSSG-type signal TSV pair to obtain the differential output voltage. For the noise coupling measurement with the GSG-type, the measurement environment is similar. The input source is the clock signal with a 500 mV peak-to-peak amplitude and the coupled noise voltage is measured at the opposite side of a GSG-type signal TSV pair with an oscilloscope. The clock frequency is 1 GHz.

The measured coupled noise voltage waveforms are shown in Fig. 2.33. For the GSSG-type, the peak-to-peak noise voltage is 16 mV. For the GSG-type, the peak-to-peak noise voltage is 34 mV. From the measurements, a differential signal TSV (GSSG-type) is better in noise immunity than a single-ended signal TSV (GSG-type). Although differential signaling with TSVs results in a greater insertion loss and tighter voltage and timing margins, it still has the advantage of higher noise immunity for sensitive and high-speed systems.

Table 2.3 includes a comparison between a differential signal TSV (GSSG-type) and a single-ended signal TSV (GSG-type) based on the performance metrics, such as the number of TSVs, insertion loss, characteristic impedance, eye opening, timing jitter, and coupled noise voltage. Even with the advantage of a higher noise immunity for differential signaling, differential signaling with TSVs results in a more degraded signal transmission than single-ended signaling. Because a TSV is a capacitive interconnect due to the thin oxide layer and has leakage through the silicon substrate, the electrical behavior of differential signaling with TSVs is worse than that of a single-ended signaling with TSVs. To use differential signaling with TSVs in 3D ICs, we must consider these electrical behaviors.

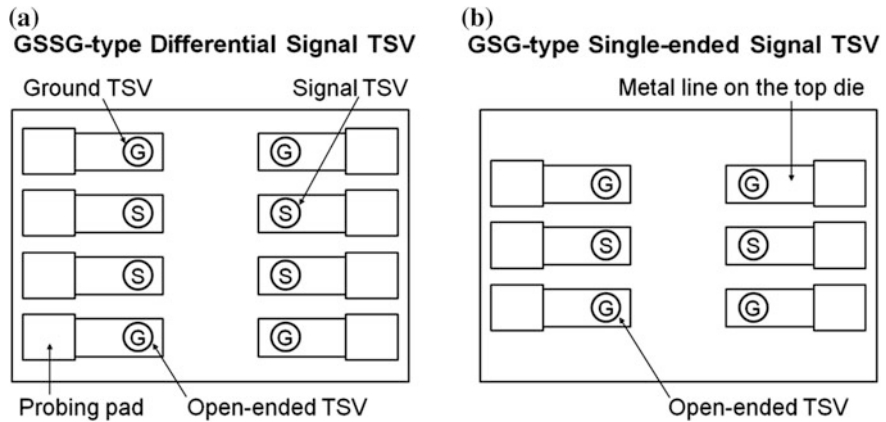


Fig. 2.32 Top view of the fabricated test vehicles of (a) a GSSG-type differential signal TSV and (b) a GSG-type single-ended signal TSV for performance comparison and analysis. The TSVs in the test vehicles are open-ended for the noise coupling measurements [25]

Fig. 2.33 The measured coupled noise voltage waveforms of the GSSG-type and GSG-type signal TSVs, which have peak-to-peak voltages of 34 mV and 16 mV, respectively [25]

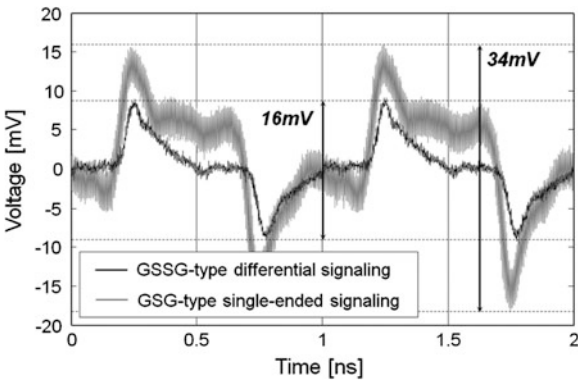


Table 2.3 A comparison of various electrical characteristics for differential and single-ended signaling schemes [25]

Performance metrics	GSSG-type differential signaling	GSG-type single-ended signaling
Number of TSVs	4ea (GSSG)	3ea (GSG)
Insertion loss @ 5 GHz	−2 dB	−0.8 dB
Characteristic impedance (0.01–5 GHz)	27–52 Ω	28–78 Ω
Eye opening ($V_{in} = 500$ mV)	275 mV	352 mV
Timing jitter ($t_{UI} = 80$ ps)	14.11 ps	13.87 ps
Coupled noise voltage	16 mV	34 mV

2.5 Summary

In this chapter, the analytic scalable model of a TSV is proposed with closed-form equations which are functions of the design parameters, material properties and frequency. Based on the proposed model, the electrical characteristics of a TSV depending on design parameter variations are analyzed up to 20 GHz. The TSV channels are fabricated and measured for the model verification. The model is successfully verified by experimental results in frequency- and time-domain. In order to evaluate the signaling performance of single-ended and differential TSVs, the test vehicles are fabricated and measured for the analysis.

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Electrical Design of Through Silicon Via

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2014, IX, 280 p. 249 illus., Hardcover

ISBN: 978-94-017-9037-6