

Contents

1	Introduction to Network-on-Chip Design	1
1.1	The Physical Medium	2
1.2	Flow Control	4
1.3	Read–Write Transactions	5
1.4	Transactions on the Network: The Transport Layer	6
1.4.1	Network Interfaces	6
1.4.2	The Network: The Physical Layer	8
1.5	Putting It All Together	9
1.6	Take-Away Points	10
2	Link-Level Flow Control and Buffering	11
2.1	Elastic Buffers	12
2.1.1	Half-Bandwidth Elastic Buffer	13
2.1.2	Full-Bandwidth 2-Slot Elastic Buffer	15
2.1.3	Alternative Full-Throughput Elastic Buffers	16
2.2	Generic FIFO Queues	18
2.3	Abstract Flow Control Model	20
2.4	Credit-Based Flow Control	21
2.5	Pipelined Data Transfer and the Round-Trip Time	22
2.5.1	Pipelined Links with Ready/Valid Flow Control	24
2.5.2	Pipelined Links with Elastic Buffers	27
2.5.3	Pipelined Links and Credit-Based Flow Control	28
2.6	Request–Acknowledge Handshake and Bufferless Flow Control	31
2.7	Wide Message Transmission	32
2.8	Take-Away Points	35
3	Baseline Switching Modules and Routers	37
3.1	Multiple Inputs Connecting to One Output	38
3.1.1	Credit-Based Flow Control at the Output Link	41
3.1.2	Granularity of Buffer Allocation	42
3.1.3	Hierarchical Switching	43

3.2	The Reverse Connection: Splitting One Source to Many Receivers	45
3.3	Multiple Inputs Connecting to Multiple Outputs Using a Reduced Switching Datapath.....	46
3.3.1	Credit-Based Flow Control at the Output Link.....	47
3.3.2	Adding More Switching Elements	48
3.4	Multiple Inputs Connecting to Multiple Outputs Using an Unrolled Switching Datapath	49
3.5	Head-of-Line Blocking	52
3.6	Routers in the Network: Routing Computation.....	53
3.6.1	Lookahead Routing Computation	55
3.7	Hierarchical Switching.....	58
3.8	Take-Away Points	59
4	Arbitration Logic	61
4.1	Fixed Priority Arbitration.....	61
4.1.1	Generation of the Grant Signals.....	63
4.2	Round-Robin Arbitration	65
4.2.1	Merging Round-Robin Arbitration with Multiplexing	67
4.3	Arbiters with 2D Priority State	68
4.3.1	Priority Update Policies	69
4.4	Take-Away Points	71
5	Pipelined Wormhole Routers	73
5.1	Review of Single-Cycle Router Organization	75
5.1.1	Credit Consume and State Update	76
5.1.2	Example of Packet Flow in the Single-Cycle Router	76
5.2	The Routing Computation Pipeline Stage	77
5.2.1	Idle-Cycle Free Operation of the RC Pipeline Stage.....	80
5.3	The Switch Allocation Pipeline Stage	82
5.3.1	Elementary Organization	82
5.3.2	Alternative Organization of the SA Pipeline Stage	84
5.3.3	Idle-Cycle Free Operation of the SA Pipeline Stage.....	86
5.4	Pipelined Routers with RC and SA Pipeline Stages.....	88
5.4.1	Pipelining the Router Only in the Control Path	88
5.4.2	Pipelining the Router in the Control and the Datapath.....	89
5.5	Take-Away Points	91
6	Virtual-Channel Flow Control and Buffering	93
6.1	The Operation of Virtual-Channel Flow Control	94
6.2	Virtual-Channel Buffers	97
6.3	Buffer Sharing.....	99
6.3.1	The Organization and Operation of a Generic Shared Buffer	101
6.3.2	Primitive Shared Buffer for VCs: ElastiStore	103

6.4	VC Flow Control on Pipelined Links	105
6.4.1	Pipelined Links with VCs Using Ready/Valid Flow Control	106
6.4.2	Pipelined Links with VCs Using Credit-Based Flow Control	108
6.5	Take-Away Points	109
7	Baseline Virtual-Channel Based Switching Modules and Routers	111
7.1	Many to One Connection with VCs	111
7.1.1	State Variables Required Per-Input and Per-Output VC	112
7.1.2	Request Generation for the VC Allocator	113
7.1.3	Request Generation for the Switch Allocator	115
7.1.4	Gathering Grants and Moving to the Output	117
7.1.5	The Internal Organization of the VC Allocator for a Many-to-One Connection	117
7.1.6	The Internal Organization of the Switch Allocator for a Many-to-One Connection	119
7.1.7	Output-First Allocation	121
7.2	Many-to-Many Connections Using an Unrolled Datapath: A Complete VC-Based Router	121
7.2.1	Routing Computation	122
7.2.2	Requests to VC the Allocator	123
7.2.3	Requests to the Switch Allocator	123
7.2.4	Gathering Grants and Moving to the Output	126
7.2.5	The Internal Organization of the VC Allocator for a VC-Based Router	127
7.2.6	The Internal Organization of the Switch Allocator for a VC-Based Router	129
7.3	VA and SA Built with Centralized Allocators	131
7.4	Take-Away Points	133
8	High-Speed Allocators for VC-Based Routers	135
8.1	Virtual Networks: Reducing the Complexity of VC Allocation	136
8.2	Lookahead VA1	137
8.3	VC Allocation Without VA2: Combined Allocation	138
8.3.1	Combined Allocation with VA1 in Series to SA	139
8.3.2	Combined Allocation with VA1 in Parallel to SA	139
8.3.3	Combined Allocation with Lookahead VA1	141
8.4	Speculative Switch Allocation	141
8.4.1	Handling the Speculative and the Non-speculative Grants ...	143
8.5	VC-Based Routers with Input Speedup	145
8.6	Take-Away Points	147
9	Pipelined Virtual-Channel-Based Routers	149
9.1	Review of Single-Cycle VC-Based Router Organization	150
9.1.1	Example 1: Two Packets Arriving at the Same Input VC	151

9.1.2	Example 2: Two Packets Arriving at Different Input VCs	152
9.2	The Routing Computation Pipeline Stage	153
9.2.1	Pipelining the Router Only in the Control Path	154
9.2.2	Pipelining the Router in the Control and the Data Path	155
9.3	The VC Allocation Pipeline Stage	157
9.3.1	Example 1: Two Packets Arriving at the Same Input VC	158
9.3.2	Example 2: Two Packets Arriving at Different Input VCs	159
9.3.3	Obstacles in Removing the Deficiency of the VA Pipeline Stage	160
9.4	The Switch Allocation Pipeline Stage	161
9.4.1	Credit Consume and State Update	162
9.5	Multi-stage Pipelined Organizations for VC-Based Routers.....	163
9.5.1	Three-Stage Pipelined Organization: RC VA SA-ST	164
9.5.2	Three-Stage Pipelined Organization: RC-VA SA ST	166
9.5.3	Four-Stage Pipelined Organization: RC VA SA ST	167
9.6	Take-Away Points	169
References.....		171

<http://www.springer.com/978-1-4614-4300-1>

Microarchitecture of Network-on-Chip Routers

A Designer's Perspective

Dimitrakopoulos, G.; Psarras, A.; Seitanidis, I.

2015, XIV, 175 p. 134 illus., 77 illus. in color., Hardcover

ISBN: 978-1-4614-4300-1