

## Chapter 2

# Interconnection: The Joint

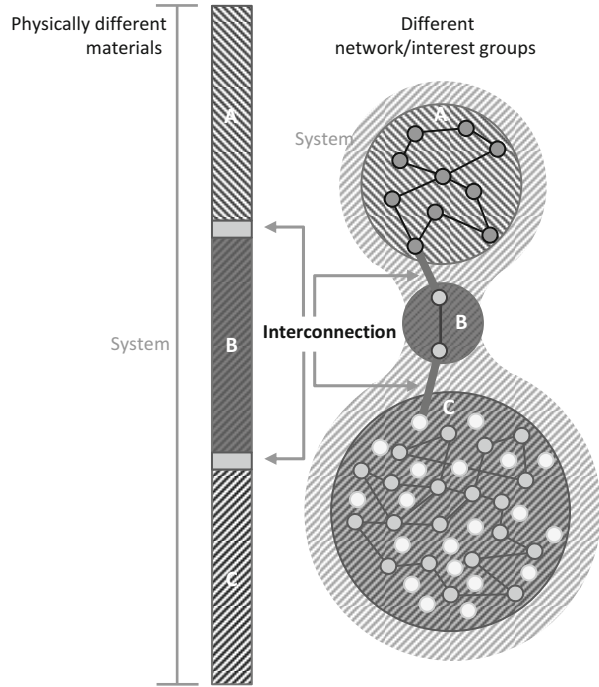
From power cord to the printed circuit board (PCB), from the PCB to components via each solder joint, from solder joints to substrate through silicon chips via wire or flip-chip solder bump, and then to another adjacent chip with a chip on top connected with microbumps, electronic devices are constructed with various interconnects through various material sets and thus various interfaces that are called interconnections. Chapter 2 describes the various types of packaging structures and the interconnections existing in industry products. Also, the base structure for each interconnect material set is described.

### What Is an Interconnect in Electronic Device

As with many words, the definition of interconnection varies according to the context in which the word is used. The overall general definition is a connection (physical or logical) between multiple things [1, 2]. In a more detailed sense for the telecommunication sector, it is the linking of two networks for the mutual exchange of traffic, as defined by the US Code of Federal Regulations [3]. In a smart grid sector, it means connecting renewable-energy systems to the power grid. But when thinking about the meaning of “interconnection,” it may also sound political and social because it connects not only physically different things but also needs to deal with different characteristics, sometimes a strong bond or weak link between two different physical or social groups. In any of these situations, an interface connects the whole, and a system is built (Fig. 2.1).

The bonding between different things, in the context of electronic devices, involves layers that are crucial because it provides structure stability to the component and, in a bigger picture, the stability of the system. An interesting phenomenon occurs once an interconnect or a joint is formed. If the bonding between the two material sets is strong, it may be stable, or it may cause a shift from one weak link to another weak interface. For example, an electric device can have very strong

**Fig. 2.1** Interconnection, a contact point for different material sets or different networks



solder joints, but the system can be unstable because fracture can occur *near* the solder joint interface inside the package substrate or in the dielectric material within the silicon die or even cause laminate cracking in the circuit board. Therefore, increasing strength in only one section of the interconnect is not enough, and strengthening the whole system is not simple, as a careful design that absorbs the distributed stress and shifts the excessive stress or strain to a place where it can be sustained is needed. This is a crucial design factor, which ultimately improves the stability of the interconnect as well as the whole system.

There are many types of interconnections in electronic systems: Starting from the electronic plug-in cord, there are pin connectors and solder joints between the PCB and modules, solder joints from modules to a component, wire bond interconnects or solder bumps (on a flip-chip joint) from the component substrate to the Si chip, and microbumps from a Si chip to another stacked Si chip. Each of the interconnection types has their own functionality and configuration within electronic systems.

To cover all of these interconnects, one book is definitely insufficient, not only because of the variety of interconnects, but also because interconnect technology is a fast moving technology, where every quarter year, a new technology is introduced to improve the functionality and the form factor. Thus, to identify the foundation for this fast moving technology sector, this book will focus on the structural interconnect between the PCB and the component. We will further consider the next-generation (smaller and more highly stressed) interconnects briefly in Chap. 8.

Figure 2.2 shows an overall diagram of what types of electronic packages exist. There are several approaches to connect the component to the board to make a system. One of the simplest ways is drilling a hole into the PCB and inserting the lead of the component for bonding, known as through-hole components. Capacitors or resistors are simple components with two or three channels to connect to the PCB circuitry. Such components with through-hole leads are soldered to the board using a wave soldering process. Another package type using through-hole leads are dual in-line packages (DIPs). DIPs are classic electronic packages, which are still widely used for memory or in a variety of IC devices. They are directly soldered to the board or sometimes placed into a socket, which is another type of connection to the board. But with increasing functionality and IO density, more and more leads are needed with a demand of smaller and thinner package size with more input and output channels to and from a single Si die. Thus, the DIPs are being changed to denser package types such as a quad flat no-lead (QFN), ball grid array (BGA), or board on chip (BOC) type packages. Since it is not efficient to drill hundreds of through holes in the PCB, the higher-density packages use smaller pads with solder paste or solder balls to make connections to the board. These components can also be attached to the PCB by simply using solder paste. A small amount of solder paste is printed using a stencil at the Cu pad location, and the component is placed on top of the solder paste right before going through a solder reflow process oven. This approach is defined as surface-mount technology (SMT). Designs that use only paste are QFNs and land grid arrays (LGA), and solder balls are used for FBGAs, PBGAs, and the FCBGAs (acronyms are defined in Fig. 2.2).

The surface-mount components can be as versatile as the function of each component requires. Packages that do not need a lot of signal pins have a lead package like the quad flat package (QFP) or thin small-outline package (TSOP), but when the number of signal pins needs to be increased, BGA components are needed. Among the BGA components, maybe the simplest component package with solder balls attached might be the wafer-level chip-scale package (WLCSP) since the silicon die is directly bonded to the PCB via solder balls. But having the bare silicon die on a board is often a risk since it can be easily damaged by external factors and the interconnects must be under the die area. The CTE mismatch between the silicon and the PCB is also a challenge to overcome, thus having a very large WLCSP is problematic. Due to these limitations, various electronic packaging technologies were introduced to place these silicon chips onto the board. Electronic packaging not only protects the silicon die but also provides the connection from the Si to the substrate and to PCB and other components to form an electronic system. The package types vary by the component function, and it is hard to categorize the whole packaging family into well-distinguished categories. Thus, in this book, we have selected a few representative package types (Fig. 2.2).

Within the component package there are also various methods of connecting the Si die to the substrate. As shown in Fig. 2.3, one of the novel connection methods is using thin metal wire. Gold wire was used in components for a very long time, but with the increasing price of gold, recently Cu and Ag alloy wires have been developed [4–6]. Each material has its own advantages and disadvantages, so the




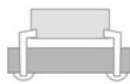




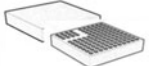



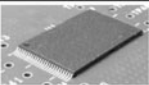






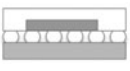

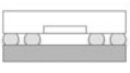
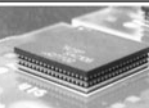

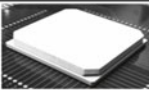

Through-hole	Transistor outline (TO)	wide range of small pin count packages often used for discrete parts like transistors or diodes.		
	Dual in-line packages (DIP)	commonly used for integrated circuits (ICs). Other devices in DIP packages include resistor, LED and electromechanical relays.		
Direct surface mount	Surface mount capacitor	Single package bulk component usually have each end as a contact pad with Sn plated surface.		
	Quad Flat No-lead package (QFN)	A leadframe-based, near-chip scale package with solderable lands instead of leads or balls		
	Land Grid array (LGA)	LGA is another term used for parts without solder balls. The same BOM (bill of material) is used when parts are assembled		
Leaded	Quad Flat package (QFP)	Quad Flat Pack. Lead/ Ball Count Range: 32-256		
	Thin small-outline package (TSOP)	Low-profile (about 1mm) with tight lead spacing, frequently used for RAM or Flash memory ICs		
Ball Grid array	Wafer Level Chip Scale Package (WLCSPP)	Si die directly BGA ball attached. Available in direct bump on pad and bump on repassivation and redistribution		
	Plastic Ball grid array (PBGA)	A plastic overmolded product using 2,4,6 and 8 layer substrate with die-up configuration and passive attach.		
	Fine Ball grid array (FBGA)	Die up wire bonded, overmolded configuration with ball pitches ranging from 0.4 mm - 1.0 mm. Thin core laminate and thin mold also called CTBGA or CABGA		
	Board on Chip (BOC)	Designed as a cost-effective CSP (chip scale package) solution specifically for high-frequency memory devices.		
	Package on Package (PoP)	Combine vertically discrete logic and memory ball grid array (BGA) packages. Two or more packages are installed atop each other		
	Ceramic Ball grid array (CBGA)	Ceramic substrates can endure much higher temperature without serious warpage but are also very stiff		

Fig. 2.2 Selected package designs

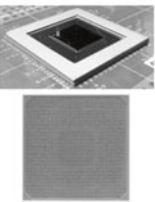

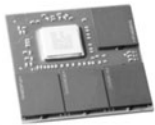



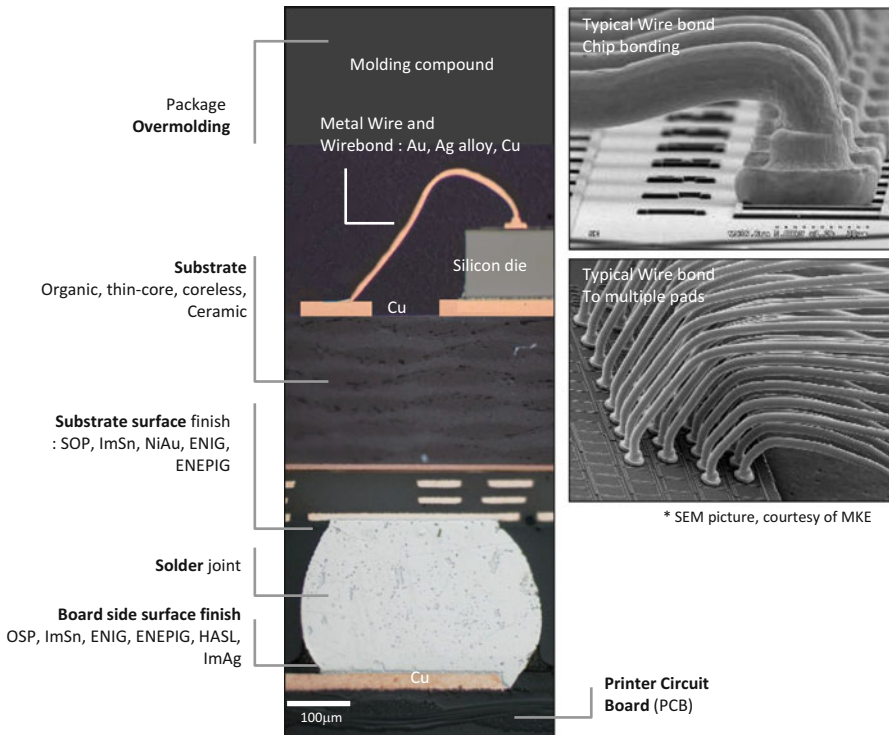
Ball Grid array with Area array	Flip Chip ball grid array (FCBGA)	Flip Chip technology use array interconnect of die to substrate as a replacement for wire bonding. The entire die surface is used for electrical connections to the substrate, exponentially increasing the I/O per unit area vs. perimeter interconnect technologies.		
	Multi chip module (MCM)	A fully functional system or subsystem in an IC package format. Multiple dies are placed onto a single substrate, boosting functionality and signal speed.		
	System on package (SoP)	System-On-Package (SOP) provides all the system functions in one single module, have multiple integrated ICs for analog, digital and optical functions		
	System in package (SiP)	A system-in-a-package (SiP), also known as a Chip Stack MCM (multi-component module). SiP dies are stacked vertically, compared to the horizontally placed MCMs		

Fig. 2.2 (continued)

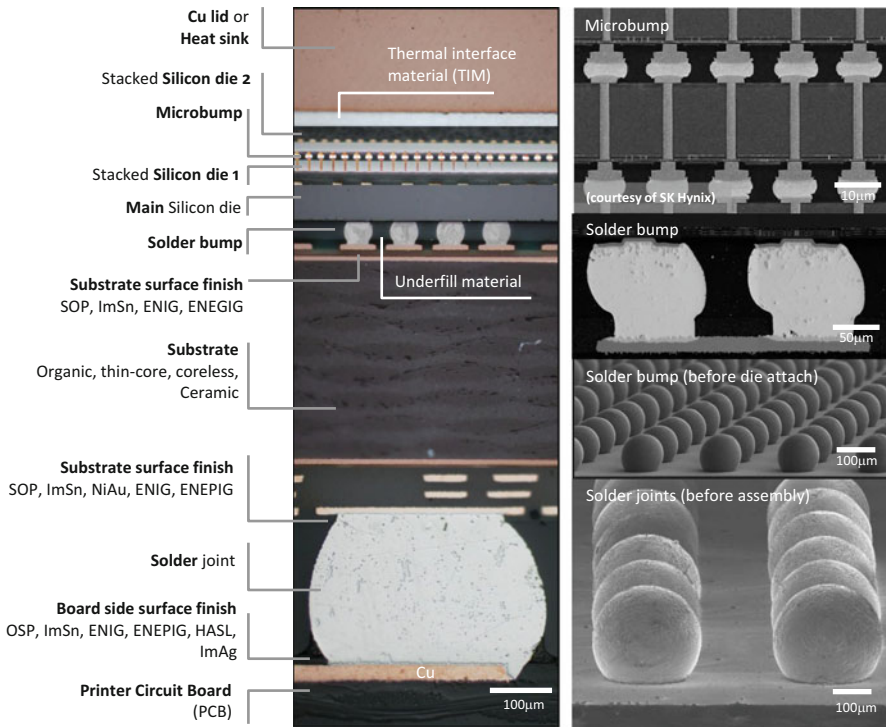
material properties required for each use condition need to be carefully considered. But with an increasing number of connections to be made, the available space around the perimeter of the die for wire bonding is getting denser and denser. Even with two rows of wire connections, space is limited, and a different interconnect technology is needed for higher density and more interconnection per unit area. In the early 1980s, a technology was developed, and it became well adopted by the industry called flip-chip technology. As shown in Fig. 2.4, instead of using wire, a miniaturized solder joint is placed between the Si die and the substrate. Since the joint, which is called a solder bump, can be small and is also placed under the die with a very fine pitch, this technology makes it possible for the electronic device to be more densely packed with more functions available, leading to much higher computing speeds, resulting from a shorter connection distance than wire connections. Flip-chip solder bumps are small and must endure the high CTE mismatch between the silicon and the organic or ceramic substrate, so to assist the accommodation of the CTE mismatch, a polymer underfill is injected after the solder bumps are formed to strengthen the interface. This underfill process is also used in WLCSP assembled boards, where additional strengthening is needed for both thermal and mechanical performance improvement. Recently a modified process technology called thermal compression bonding (TCB) was introduced, which combines the reflow of the solder bump and the underfill into one operation.



**Fig. 2.3** Wire bond package interconnections

With all of the above package types, there are also packages with multiple combinations of technologies. For example, two or three silicon die can be stacked up with Au wire connecting not only the Si die and the substrate but also providing connection between multiple Si dies, which are called multi-chip components (MCC). This concept can be also applied to a single substrate with several silicon die or components in parallel and are called multi-chip modules (MCM). Another type of package is the package on package (PoP), a stack-up of several independent BGA components.

The most recent new technologies need even higher density and functionality in a single device or component. Since the signal speed needs to be faster without sacrificing any signal loss, the distance between the silicon chips needs to be closer than ever, with not only one application-specific integrated circuit (ASIC) chip but with central processor unit (CPU) and memory chips installed together on one single substrate. This came to be possible with drilling a hole into the Si chip itself and connecting the top and bottom of the silicon chip. While it is conceptually simple, drilling a small hole into the Si and filling it with conductive metal like Cu, the technology itself, through-silicon via (TSV) technology, is a huge challenge, and



**Fig. 2.4** Flip-chip connected package with Silicon die stack-up with through silicon via (TSV) and microbump connection

the industry is still in the process of fine tuning. But with developing the process and assessing the reliability of these devices, these will appear in a wide range of high-function components. This technology enables a new form of package and interconnect, which is the interconnect between one Si die and another using an even more miniaturized solder joint, called microbumps.

With a roadmap for a design concept for a new technology, a new package category came to the industry, the MCM, system on chip (SoC), system on package (SoP), and system in package (SiP). All of these concepts are similar, but small differences between these terms exist based on structural aspects. SoC, for example, seeks to integrate numerous system functions on one silicon chip, meaning that the package remains the same among different SoC, because they are built on the same Si die. Fabricating one perfect Si chip with all the different component functions inside is a challenge and still a costly option. This technology will be revisited in Chap. 8 after the challenges for existing interconnect technology are discussed, to anticipate future challenges. An SiP is a fully functional system or subsystem in an IC package format. It contains one or more IC chips, plus other components traditionally found on the system board. These components may include passive components, RF shields, prepackaged ICs, connectors, antennas,



camera lenses, or other mechanical parts required to achieve full system functionality. This package type is also known as a chip stack MCM. SiP dies are stacked vertically, unlike a slightly less dense MCM, which places dies on the same plane alongside one another. It is considered an intermediate solution on the path to the SoC. The definitions of the MCM and the SiP overlap, but if the Si die are stacked, it is usually called an SiP, and if those components are placed horizontally, it is called an MCM.

From the power cord to microbumps, electronic devices are constructed with various interconnects through various material sets and thus various interfaces that are called interconnections.

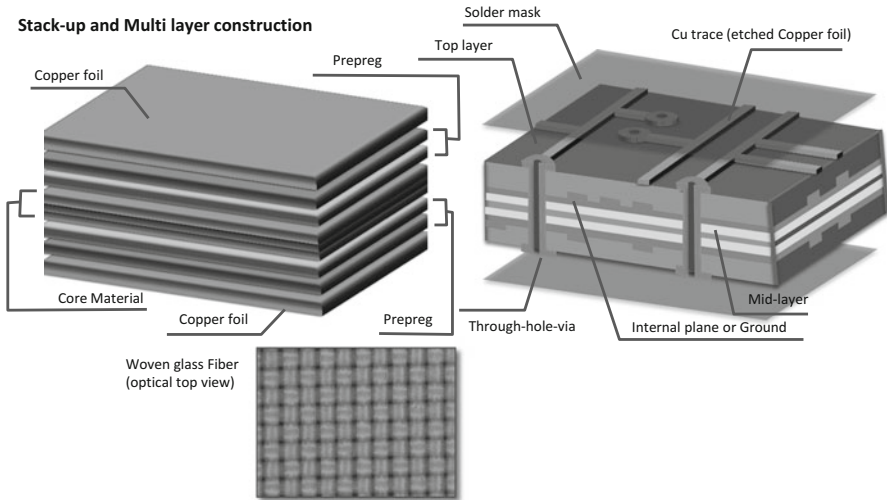
## Printed Circuit Board

As illustrated in Figs. 2.3 and 2.4, the interconnection from the Si to the substrate, whether it is via Au wire or a solder bump, needs to be connected to the board to connect the component functionality to the system. A PCB is used to mechanically support and electrically connect electronic components using conductive pathways, tracks, or signal traces etched from copper sheets laminated onto a nonconductive substrate [7, 8]. When the board has only copper tracks and features, and no circuit elements such as capacitors, resistors, or active devices have been manufactured into the actual substrate of the board, it is more correctly referred to as printed wiring board (PWB) or etched wiring board [8, 9]. Although more accurate and distinct from what would be known as a true printed circuit board, use of the term PWB or printed wiring board has generally fallen by the wayside for many people as the distinction between circuit and wiring has become blurred. Today, PCBs are used in virtually all but the simplest commercially produced electronic devices and allow fully automated assembly processes that were not possible or practical in the past. A PCB populated with electronic components is called a printed circuit assembly (PCA), printed circuit board assembly, or PCB assembly (PCBA). In informal use, the term “PCB” is used both for bare and assembled boards, the context clarifying the meaning [9].

A schematic presented in Fig. 2.5 shows the construction of a PCB. Circuit board materials available for multilayer construction are primarily of two types: core material that has copper laminated to both sides (cured laminate) and pre-preg material (uncured resin treated glass) used to fill the space between cores and out-layer foils that are used to bond all of the layers together. Copper foil of various weights (half ounce or greater) is available as well for outer layer construction. Pre-preg is a term for “pre-impregnated” composite fibers, where a material, such as epoxy, is already present. These usually take the form of a weave or are unidirectional. They already contain an amount of the matrix material used to bond them together and to other components during manufacture. The resin is only partially cured to allow easy handling.

The core material is the basis for the construction of the multilayered board. It is etched with the required circuitry and oxide treated to promote proper adherence to





**Fig. 2.5** Printed Circuit board stack-up and multilayer construction

the pre-preg layers that will be applied in the subsequent stack-up. Regarding the material for the core, for example, FR-4 is commonly used for PCBs. The abbreviation “FR4” means: F (for flame) and R (for retardant), and the 4 is a # 4 epoxy. FR4 features high-flexural, impact, and mechanical bond strength at temperatures up to 130 °C, which is the glass transition temperature ( $T_g$ ) for this material. With this  $T_g$ , it is possible to pass through two or three reflow processes. While FR4 is common, there are various  $T_g$  material options available for applications that require different properties.

## Solder Alloys

The components need to be mounted on the PCB. Connecting different materials at a very fine scale is a challenge because bonding needs to be made between components with different physical properties. Soldering is a process in which two or more metal items are joined together by melting a lower melting temperature solder alloy into the joint. There are numerous solder alloy compositions in the industry, which serve specific purposes. Figure 2.6 shows a span of alloy compositions based on their liquidus and solidus temperatures. Some are eutectic (have one low melting temperature), and some have a gap between the liquidus and solidus temperature that results in a mushy zone between being fully liquid and fully solid during cooling (based on the equilibrium assumptions). In reality, undercooling is required to solidify, which will be discussed in depth in Chaps. 3 and 4. Pb-based solder alloys have been used for at least 2,500 years (dating to the ancient Egyptians) or earlier during the early Bronze age. It was relatively easy to extract and form a good alloy with other elements at that time. Pb-based solders were used for jewelry and making

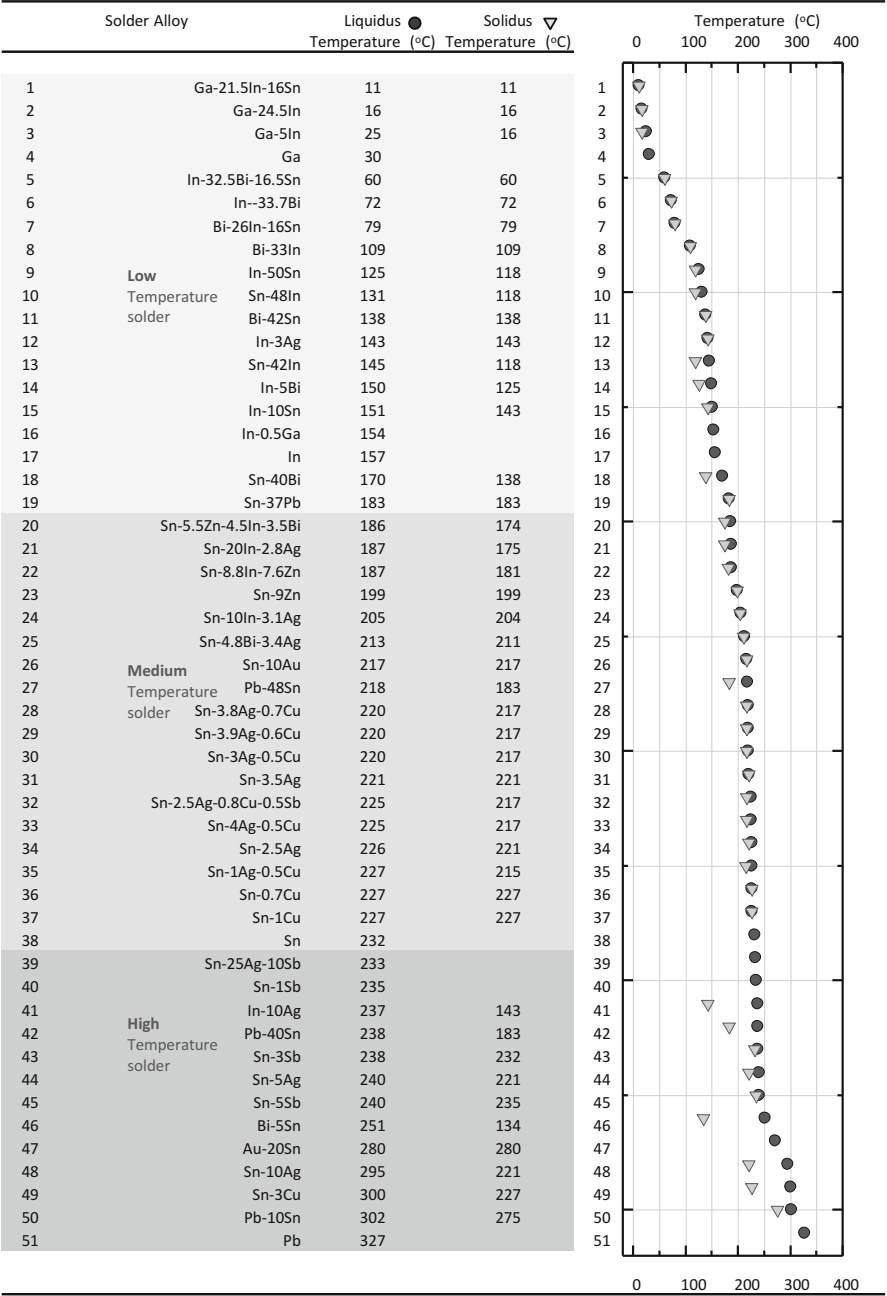


Fig. 2.6 Selected solder alloy compositions and liquidus/solidus temperature

bonds between metals including the ancient pipes in aqueducts [10–15]. Hence, in the periodic table, element symbol Pb comes from a Latin origin “plumbum” which is also the origin of plumbing, so it was natural to use Pb as an interconnect material. But since the ban on hazardous materials in consumer electronics since 2006, and beyond consumer electronics in the whole electronics industry nowadays, Sn-based solder alloys have replaced Pb-bearing solders in most applications [10–22]. Sn was also used in an alloy form since the Bronze Age, as it was the metal that made bronze. But replacing the Pb with Sn was not sufficient for solder joints, so alloying elements such as Cu and Ag to make Sn–Ag–Cu (SAC) alloys have brought performance necessary to meet requirements [23–36].

There are a number of SAC alloy compositions in current use, and many more have been developed in the past. The first recommendation for SAC family was made by both Soldertec and iNEMI in 2000, as a result of the IDEALS project in Europe. There are 33 alloys chronicled in the ELFNET/COST 531 database, but the property variation among these 33 alloys does not seem to be significant. The large variation in alloy compositions may be largely motivated by patenting and commercial issues. The IPC Solder Products Value Council studied the effect of this variation in a large collaborative program and concluded that there was very little performance difference between commonly used formulations. Low-silver alloys have nevertheless been an important new development, initially aiming at reducing costs of Ag but later for cultivating beneficial properties such as shock resistance, which will be discussed in depth in Chaps. 4–6 [37–39].

It is expected that more SAC alloys will be added to the existing family. Unlike previous motivations to win the market by differentiation, future development will be driven more by technology demand for tailored performance. While SAC solder is quickly replacing Pb–Sn solder in electronic packaging, packaging technology itself is rapidly changing with new directions. Overall miniaturization of existing packaging structure, such as flip-chip and BGA, is one direction, but another direction is 3D packaging where unusually small solder interconnects are essential. In such cases, as the solder amount is small compared to joining substrates, control of the intermetallic (IMC) bond layer growth is necessary. Excessive reaction with Cu in microbumps, for example, can result in a joint that is prone to failure by shock or fatigue. One notable development in this area is the microalloyed SAC system. SAC alloys containing a minute amount of Ni, Co, Mn, or Ge are now used as ball materials for BGA applications [27–32, 34, 36–44]. Similar alloys with Pd and Fe are also under investigation [30–45]. The beneficial effects of microalloying are becoming known, but the links between microstructure and reliability are not fully understood. Further, they may not provide enough protection against reliability issues stemming from excessive IMC growth. More ideal alloys may contain higher Cu to reduce reactivity with Cu without increasing brittleness of the solder alloy itself. Another reason for needing new SAC alloys for 3D packaging technology may be related to the process itself. The small volume of solder with large joint surface increases the likelihood of trapping cavities. This demands fluxless soldering or the use of flux that does not produce cavities. This will inevitably require different SAC solder alloys because existing alloys may not be compatible with a fluxless process or do not well work with new fluxes [46, 47].

The fact that SAC alloys prevail for present electronic packaging technology doesn't mean that alloy development is completed. There are continuing efforts to develop other alloy systems. Some of these efforts are motivated to adjust the strength (to lower it in many cases) of SAC alloys to improve reliability, while the other efforts will enable new packaging technologies. One of the most serious challenges to removing the Pb–Sn alloy system from the solder materials is the lack of suitable alloys for high-temperature applications. Many of the electronics used for automobile applications, for example, require solder alloys that can withstand operating temperatures near 150 °C [18, 19]. For such applications, solder alloys with melting temperature close to 300 °C or higher are essential. Previously, 95Pb–5Sn provided a reasonably high melting temperature as well as mechanical and chemical stability. Currently, there is no suitable Pb-free solder alloy that can provide such high-temperature application needs. One solder alloy that is qualified for such application is Sn–Au eutectic solder, but it is too expensive to be practical [48, 49]. A number of alloys currently considered and being developed include Sn–Sb and high Ag–Sn, but none of them provide properties comparable to 95Pb–5Sn [50]. Therefore, high-temperature solder is one area that is seeing an explosion of alloy development.

At the opposite end of the spectrum from high-temperature solders is low-temperature solder. There are two desired temperature levels for a low-temperature solder. The first is a melting temperature near 180 °C (the temperature of eutectic Sn–Pb), and the second is with 150 °C or lower. The purpose of the first type of alloy is to directly replace Sn–Pb eutectic alloy from the reflow temperature consideration. Since these alloys enable lower reflow temperatures than SAC alloys, they may look more eco-friendly and presumably provide a more reliable joint with lower residual thermal stress. These types of alloys include Sn–Zn, Sn–Bi, Sn–Zn–Bi alloys and their derivatives [37, 42, 51–55]. In fact, Sn–Zn alloys have been used in some applications but mainly in Japan. However, these alloys have one major weakness, that is, that they are prone to oxidation. Furthermore, for the same reason, they require the use of a strong flux and thus are not necessarily as eco-friendly as they appear. There are many studies in this area, but progress has been slow [56]. It is highly unlikely that this type of alloy will be as widely used as SAC alloys. Solder alloys with a melting temperature lower than 150 °C have also been pursued in the past. The need for low-temperature solder has risen mainly with the interest for solder-based 3D packaging and the die attachment. In order to enable 3D solder packaging process, it is necessary to have solder alloys with different reflow temperatures, so that already packaged interconnects are not disturbed by the subsequent reflow process. To this end, a handful of alloys have been investigated and developed, such as In–Sn, Sn–Bi and In–Sn–Bi. However, these alloys have multiple problems retarding their use for solder application, and their use is still very limited. One clear problem of low-temperature alloys is the fact that they are not stable against mechanical and chemical loads. Furthermore, the majority of them contain In, which is far more expensive than any other solder alloy element. This high cost also hinders their speedy adoption by the packaging industry.

Table 2.1 provides a summary of the mechanical properties in the current research database of the major lead-free solders [57]. All the data in the table were recorded at

**Table 2.1** Tensile properties of SAC alloys

Solder alloy	Elastic modulus, E (GPa)	UTS (MPa)	Yield strength (MPa)	Strain rate (s <sup>-1</sup> )	Specimen preparation	Testing method	References
Sn-3.9Ag-0.5Cu	50.3	36.2	31.9	$4.2 \times 10^{-5}$	Machined, cylindrical	Compression	[58, 59]
	54				Machined, cylindrical	Dynamic/acoustic	[58, 59]
		60		$1.78 \times 10^{-3}$	Cast, dog-bone, water quenched	Tension	[60, 61]
		41		$1.78 \times 10^{-3}$	Aged 35 days at 25 °C	tension	[60, 61]
Sn-3.8Ag-0.7Cu	43.1				Solder joints	Nano indentation	[62]
	45	40	35	$6.68 \times 10^{-4}$	Cast, cylindrical	Tension	[63]
	50	45		$1.67 \times 10^{-3}$	Cast, cylindrical	Tension	[64]
	44.4	39.6	35.1	$5.6 \times 10^{-4}$	Cast, dog-bone	Tension	[65]
	46			4-Oct	Cast, dog-bone	Tension	[66, 67]
	44.9				Solder joints	Nano indentation	[68]
	41	39	32	3-Oct	Cast, dog-bone	Tension	[69]
	46		47.1		Solder joints	Dynamic analyzer	[70]
Sn-4.1Ag-0.5Cu	43	36	33	$6.86 \times 10^{-4}$	Cast, cylindrical	Tension	[63]
Sn-4.0Ag-0.5Cu	40				Cast, dog-bone	Tension	[66]
	48.3				Solder joint	Nano indentation	[71]
	45				Bulk solder	Nano indentation	[72, 73]
		51		3-Oct	Cast, dog-bone	Tension	[74]
Sn-3.0Ag-0.5Cu	54	41.8	25.3	$4 \times 10^{-3}$	Machined, cylindrical	Tension	[75]
	37.4	43	37	$5 \times 10^{-4}$	Cast, dog-bone	Tension	[76]
Sn-3.1Ag-0.5Cu	45	49	40	$6.68 \times 10^{-4}$	Cast, cylindrical	Tension	[63]
Sn-3.2Ag-0.8Cu		32	28		Cast, cylindrical, quenched	Tension	[77]
		30	20		Air-cooled		
Sn-3.5Ag-0.7Cu		46.6			Cast, dog-bone	Tension	[66, 78]

**Table 2.2** Tensile properties of Sn-37Pb eutectic solder

Solder alloy	Elastic modulus, E (GPa)	UTS (MPa)	Yield strength (MPa)	Strain rate (s <sup>-1</sup> )	Specimen preparation	Testing method	References
Sn–Pb eutectic	33.5	33.9	30.2		Cast, cylindrical	Tension	[79]
	27	47	41	$6.86 \times 10^{-4}$	Cast, cylindrical	Tension	[63]
	32	39		$1.67 \times 10^{-3}$	Cast, cylindrical	Tension	[64]
	32		32.5		Solder joints	Dynamic analyzer	[70]
	36	54		$2 \times 10^{-2}$	Lap joints	Tension/shearing	[80]
	35	26		3-Oct	Machined, cylindrical	Tension	[81]
	29		29				[82]
	15.7	30.6	27.2				[83]
	32.1						[84]
		31–46					[85]

room temperature. There are large discrepancies in the tensile property values as well as the specimen preparation and testing approaches. The elastic modulus for SAC ranges from 30 to 54 GPa, although the majority of the values lie in the range of 40–50 GPa. The UTS values vary from 30 to 60 MPa, with the majority in the range of 35–45 MPa. The yield stresses range from 20 to 47 MPa, with the majority in the range of 25–35 MPa. All the differences in testing conditions, such as specimen geometry, testing methods, and testing strain rates, are likely to contribute to the variations.

Table 2.2 gives a summary of the mechanical properties of Sn–Pb eutectic solders, which also show large variations in the published mechanical properties [57]. The elastic modulus ranges from 16 to 36 GPa, the UTS values from 26 to 47 MPa, and the yield stress from 27 to 41 MPa. The large differences are reportedly due to the contribution of the inelastic deformation (plastic) from the slope of the stress–strain curve arising from the high homologous temperature of solders. The slope of the stress–strain curve therefore does not represent the true elastic modulus.

As the above data show, there are large discrepancies in the current database of mechanical properties for both lead-free and Sn–Pb solders. These discrepancies may have been caused by the lack of accepted standards for testing methods, specimen preparation, and testing conditions. However, none of the typical resources discuss the effect of room temperature aging, which may also lead to variations even for the same testing conditions due to the high homologous temperature of solder alloys. The room temperature aging effects have been known for decades, yet they may have played a significant role in the discrepancies in the published data.

Further assessment of details of selected solder alloys are found in Chap. 3 discussion of phase diagrams and the development of the microstructure in a joint in Chap. 4. Since the reliability of these interconnections are important in a product level configuration, it is important to have the system function as a whole and not to be concerned about each component, so the property and stability of the joint are crucial to understand. Chapters 5 and 6 will examine the evolution of thermal and mechanical performance, deformation mechanisms, and microstructure of these solder joints.

## Board Assembly

To assemble the component to the PCB, as shown in Fig. 2.7, solder balls are first attached to the component. Usually a flux is applied on top of the Cu pad surface then solder balls are placed on top of it, using a fixture, followed by a thermal reflow. After the component has the solder balls attached, the components are brought to an assembly station. A solder paste is placed on top of each Cu pad on the PCB, and the component is precisely placed on top of each Cu pad footprint using a component placing machine. Then the board goes through a reflow oven which has several heating zones set at different temperature to have a specific reflow temperature profile, as shown in Fig. 2.8.

The reflow profile is defined by the relationship of temperature versus time during heating. A typical profile consists of three heating slopes (the time vs. temperature relationship or rate of heating). Each solder paste has recommended heating slopes and time and temperature limits within each slope. The three-step heating profile slopes are called preheat, dryout, and reflow, but usually the word reflow is used to cover the whole process. For a good quality assembly process (and ultimately a reliable solder joint formation), the optimum temperature profile must be found. The heating and cooling rates must be compatible with the solder paste, components, and the overall PCB. The duration of time that the assembly is exposed to certain temperatures is a crucial factor in order to have a defect-free solder joint.

In the preheat section, the goal is to fully preheat the entire SMT assembly to temperatures between 100 and 150 °C in the case of Pb-free assembly. The most critical parameter in the preheat section is to control the heating rate to 1–4 °C/s, avoiding a thermal shock that can cause defects during reflow. The second heating section, referred to as the dryout, soak, or preflow zone, is used primarily to ensure that the solder paste is fully dried with full activation of the flux before reaching the reflow temperatures between 140 and 170 °C for a 60–120-s time period. Dryout also provides thermal stabilization of large and small components to ensure uniform heating as the assembly enters the reflow zone. Once the boards reached the reflow temperature heating section, the solder paste and the solder ball melt, forming a solder joint. The cooling section following the solidification of the joint is also a crucial section since it is important to have a suitable cooling rate to reduce the residual stress which was built during solidification. Convection ovens have reduced the need for the thermal stabilization, as



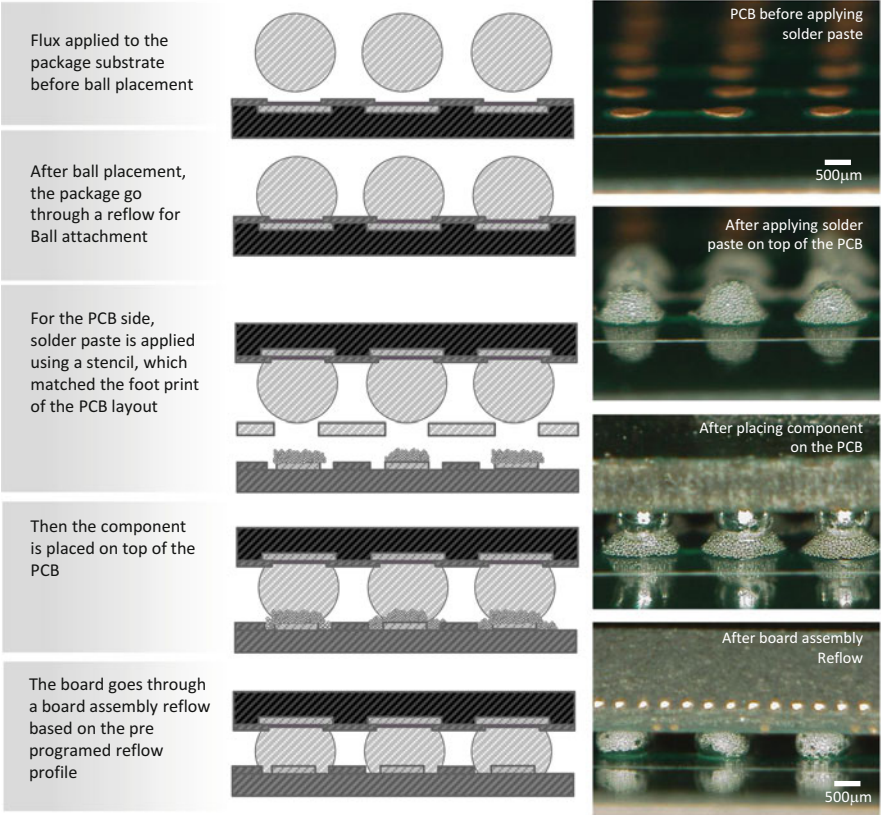


Fig. 2.7 Ball attachment and board assembly process diagram

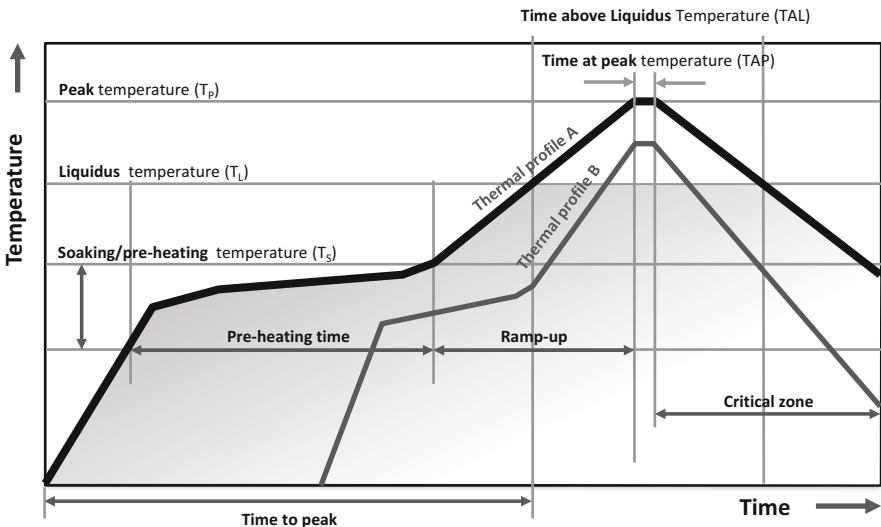


Fig. 2.8 Board assembly reflow profile

the temperature at all locations on the board tends to be uniform. Each component and board has its own unique design and hence, its own temperature distribution, so finding the right reflow profile for each product board is crucial to have a good quality board. A lot of defects can be produced when the profile is not right, as described in various publications with valuable information on SMT-related issues and defects [86].

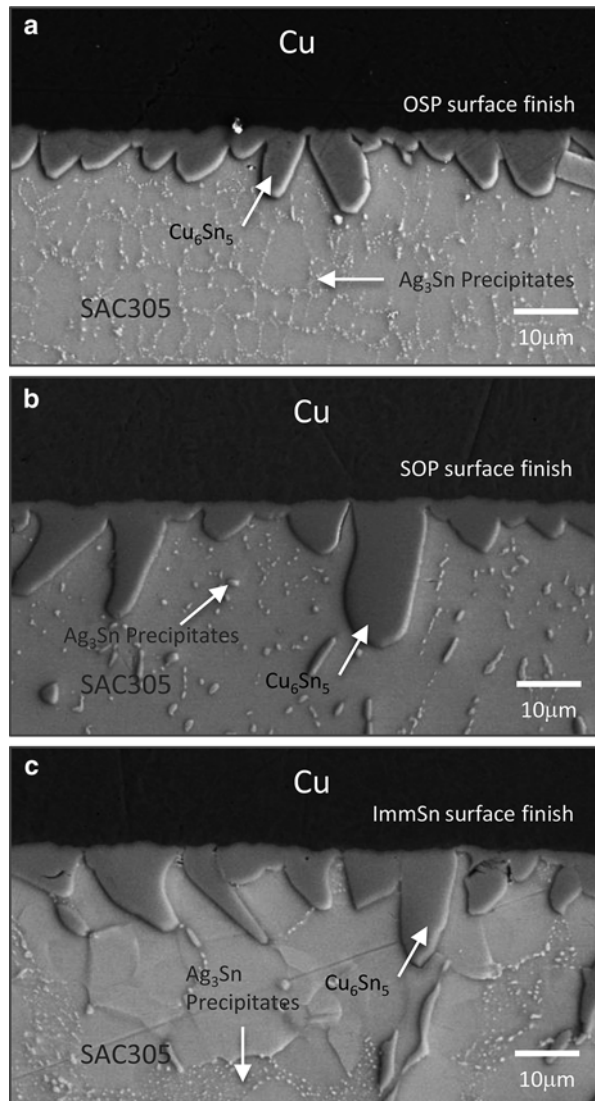
## Package Side and Board-Side Surface Finish

Cu is used for both package-side pads and the board-side PCB pads. Although it reacts well with Sn and forms a strong intermetallic compound bonding layer, exposure of Cu pads to air can easily oxidize the Cu and cause dewetting/solderability problems [87]. So, to prevent oxidation and provide a relatively long shelf life before assembly, a coating layer is applied on top of the Cu pads, which is called a surface finish. Surface finish is an important material layer for both board-side and package-side interfaces, not only because it prevents oxidation, but also because it provides a diffusion barrier between the Cu pad and solder and sometimes accelerates the wetting. As shown in Fig. 2.4, the surface finish at both interfaces of the solder joints has a variety of options. A few selected surface finishes, which are widely used in the industry, are listed below, which includes organic solderability preservatives (OSP), solder on pad (SOP), immersion Sn (ImSn), electrolytic Ni gold (NiAu), electroless nickel immersion gold (ENIG), and electroless nickel/electroless palladium/immersion gold (ENEPIG).

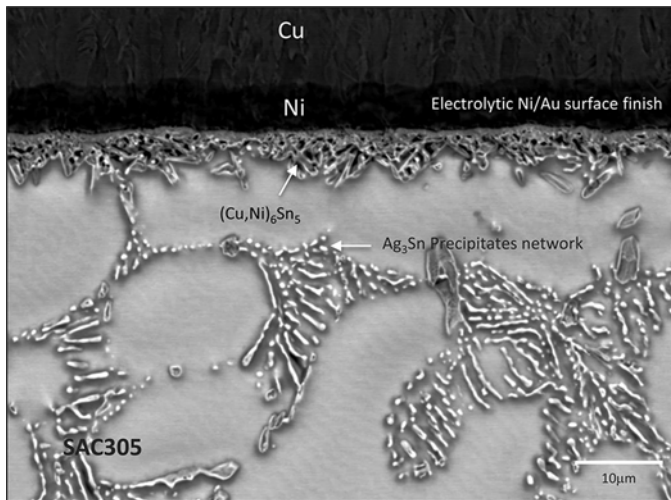
OSP contain an azole compound and are applied on top of copper pads to protect the copper surface from oxidation. The OSP is transparent and has angstrom range thickness. OSP is widely used on the board-side interface surface finish and also at the package-side interface in BGA components. Another common surface finish is SOP surface finish. SOP is more widely used at the package-side interface pads. A thin layer of solder is pre-applied to cover the exposed Cu via printing or using a microball followed with a reflow. The solder alloys used for SOP are the alloy, which is matched with the solder ball alloy to be attached later. For example, if the solder alloy for ball attachment is Sn–Pb, then the SOP is Sn–Pb; if the Sn–Ag–Cu solder ball is the target alloy then the SOP is Sn–Ag–Cu. This means that after ball attachment and reflow, the SOP layer is fully mixed into the solder alloy, resulting in only the Cu and solder interface.

A similar but different surface finish is ImSn surface finish. Instead of using a certain solder alloy composition as used for SOP, ImSn surface finish is simply Sn plated on Cu. The Sn layer is consumed into the bulk solder material right after ball attachment reflow and results in the same interface structure as the SOP or OSP. But, slightly different interface properties result, since the plated Sn often has a minor dopant in the system to mitigate Sn whiskers during storage (usually a few 100 ppm level of Ag).

**Fig. 2.9** Package side interface after board assembly using SAC305 solder with (a) OSP, (b) Solder on Pad (SOP), and (c) Immersion Sn surface finish (ImSn)



The bonding between the Cu and the solder alloy, such as SAC305, results in formation of an IMC compound layer. The thermodynamics between the formation of the IMC layer and the solder alloy itself will be thoroughly examined in Chaps. 3 and 4. Several good references are published which explain the details of the shape of the IMC layer [88–92], but as shown in Fig. 2.9, the IMC layer typically has a scallop-shaped interface. Between the Cu and the  $\text{Cu}_6\text{Sn}_5$  IMC, a second IMC layer of  $\text{Cu}_3\text{Sn}$  forms, though it is not always thick enough to see right



**Fig. 2.10** Package side interface after board assembly using electrolytic NiAu surface finish

after assembly. The difference between two IMC layers is more clearly shown in samples after isothermal aging, discussed further in Chap. 4. The continuous diffusion of Cu into the solder and the Sn diffusion into the Cu region lead to a thicker  $\text{Cu}_3\text{Sn}$  layer and an evenly thickened  $\text{Cu}_6\text{Sn}_5$  layer.

Another purpose of the surface finish is to prevent the Cu diffusion into the bulk solder. Since Cu is a fast diffuser, a prolonged exposure at high temperature during reflow can result in rapid consumption of the Cu pad that weakens the interface. One of the surface finish material options that reduce the consumption of Cu is a diffusion barrier layer of Ni. However, Ni has poor wettability for solder alloys, thus to facilitate wetting, a thin layer of Au is plated on top of the Ni surface. Applying the Ni on top on the Cu pad can be done using several different approaches. One is electrolytic plating and another is the electroless Ni plating method. Each surface finish has its own property and influence on the solder joint.

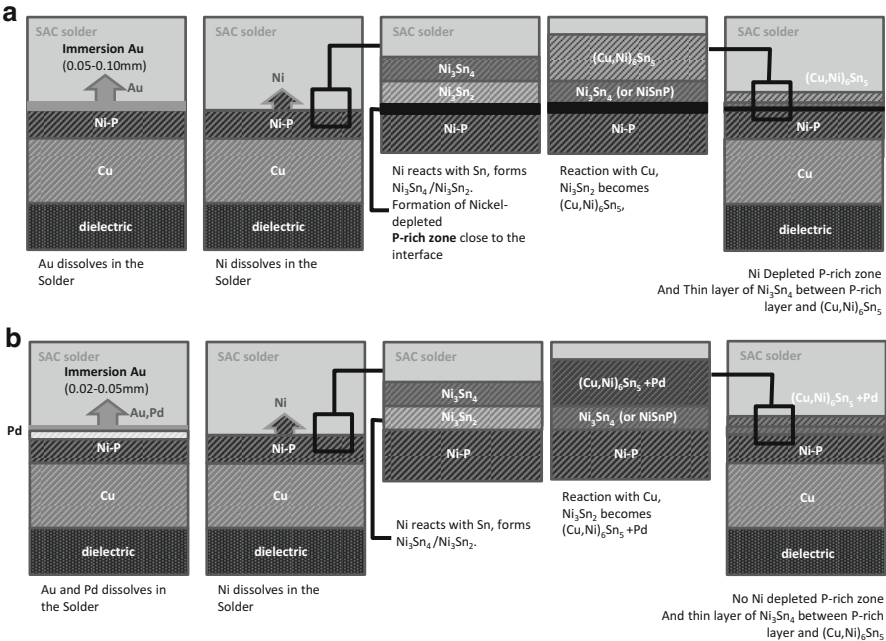
Electrolytic nickel gold (NiAu) surface finish is a widely used surface finish for package-side surface finish interfaces. Through an electrolytic process, a layer of around 3–5  $\mu\text{m}$  nickel and a flash of gold layer (usually less than 0.75  $\mu\text{m}$  of gold) are applied. The Au provides a good wettability and also a good corrosion protection of the Ni layer beneath. Most of the Au is consumed into the solder during the reflow process, and the Ni layer directly interfaces with the solder alloy by forming an intermetallic layer in between. With Ni in the surface finish composition, the interfaces show a different IMC layer morphology and composition than the OSP, SOP, and ImSn surface finish. Figure 2.10 shows a typical interface at the package-side

interface with NiAu surface finish and SAC305 solder alloy. Unlike the scallop type IMC for SOP and ImSn surface finish, the IMC here shows needle-shape IMC structure. These are  $(\text{Cu,Ni})_6\text{Sn}_5$  IMCs.

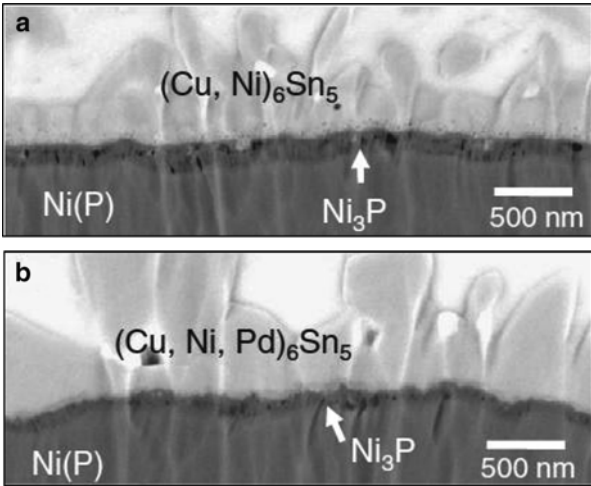
The  $\text{Cu}_6\text{Sn}_5$ -based intermetallic compound (IMC) containing Ni is the primary phase at the Sn–Ag–Cu/Ni interface with Cu content higher than 0.5 wt.% in the solder joint [93]. Ni exhibits significant solubility in  $\text{Cu}_6\text{Sn}_5$ , occupying the Cu atom sublattice to form  $(\text{Cu,Ni})_6\text{Sn}_5$  with up to 27 wt.% Ni. Thermodynamic calculations demonstrate that Ni additives can stabilize the  $(\text{Cu,Ni})_6\text{Sn}_5$  structure. The Gibbs free energy of  $(\text{Cu,Ni})_6\text{Sn}_5$  decreases by 9 kJ/mol as the Ni content increases to 20 wt.%, confirming that  $(\text{Cu,Ni})_6\text{Sn}_5$  is a more stable phase than  $\text{Cu}_6\text{Sn}_5$  in solder joints [94]. In fact,  $\text{Cu}_6\text{Sn}_5$  exists in two types of crystal structures and transforms from the monoclinic  $\eta'$   $\text{Cu}_6\text{Sn}_5$  at temperatures below 186 °C to a more stable hexagonal  $\eta$   $\text{Cu}_6\text{Sn}_5$ , which causes a volume expansion that generates internal stresses. With 5 wt.% Ni,  $(\text{Cu,Ni})_6\text{Sn}_5$  is stable in the hexagonal  $\eta$  structure at all temperatures [95, 96].

ENIG is another nickel-based surface finish. ENIG is formed by the deposition of electroless nickel–phosphorus (Ni–P) layer on a catalyzed copper surface followed by a thin layer of immersion gold. It provides a good diffusion barrier against reaction with Sn-based solders, has relatively low cost, and provides good wettability/solderability. The immersion gold protects the underlying nickel from oxidation/passivation in the same way as the electrolytic NiAu surface finish. The ENIG surface finish is used on the both package-side and board-side surfaces. The historical drawback was that the electroless nickel layer is brittle and has been found to break up during mechanical stress. Also, a galvanic hypercorrosion occurs on the Ni–P surface layer caused by the immersion Au solution, which is usually called “black pad” [97], due to the formation of Ni oxide that degrades the interfacial strength. These drawbacks can be avoided with better process control and are now less problematic. Although the processes in the industry are well tuned and controlled, the fundamental risk for black pads can be overcome by using ENEPIG surface finish. Pd prevents corrosion of the Ni–P layer that occurs before the immersion Au plating solution is used. ENEPIG is very similar to ENIG and is formed by the deposition of electroless nickel followed by 0.2  $\mu\text{m}$  of electroless palladium with an immersion gold flash ( $\sim 0.03 \mu\text{m}$ ). The palladium is plated on the electroless nickel by chemical reduction instead of a displacement reaction, which prevents attack on the electroless nickel layer.

Figure 2.11 shows a schematic diagram comparing ENIG and ENEPIG. Also, the growth behavior of  $\text{Cu}_6\text{Sn}_5$  and  $(\text{Cu,Ni})_6\text{Sn}_5$  in ENIG and ENEPIG joints in Fig. 2.12 shows differences in the interfacial reaction of ENIG and ENEPIG solder joints. Irregular-shaped IMCs formed after reflow on both metallizations. During the early stage of soldering, the thin Pd finish as well as the Au finish dissolves into the solder within a few seconds [98]. Pd was dissolved into the solder matrix since very low Pd concentration (about 0.01 wt.%) was detected by FE-EPMA. On the other hand, a slightly higher amount of Pd (0.3 wt.%) was found in the



**Fig. 2.11** Schematic comparison between (a) ENIG and (b) ENEPIG reflow process and layer evolution on the package side



**Fig. 2.12** Cross-sectional images of reflowed joints with columnar voids after thermal aging: (a) ENIG surface finish, (b) ENEPIG surface finish [100]



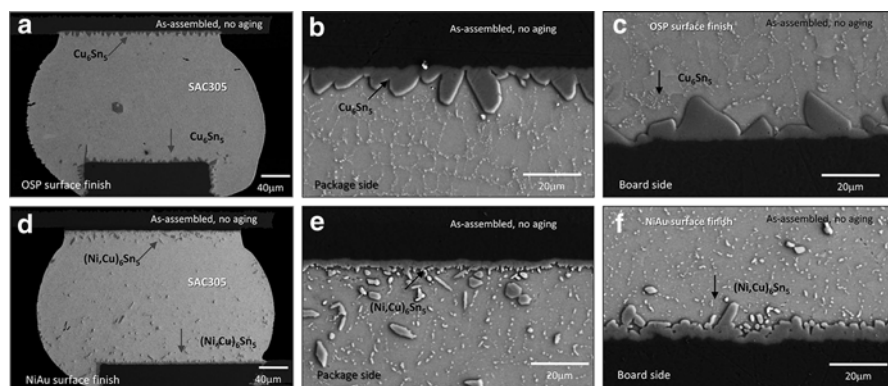
$(\text{Cu,Ni,Pd})_6\text{Sn}_5$ , implying that Pd was likely to dissolve into the IMC. Pd may refine the grain structure of  $(\text{Cu,Pd})_6\text{Sn}_5$  and also inhibit its grain growth [99]. The refinement of grain size may be attributed to lattice strain arising from the different atomic radii of Cu (128 pm) and Pd (137 pm), which causes slower grain growth in  $\text{Cu}_6\text{Sn}_5$  [100].

Other than the surface finishes stated above, there are immersion silver (ImAg) and hot air solder leveling (HASL) surface finish. Silver is deposited directly on the copper surface by a chemical displacement reaction for the ImAg surface finish. The reaction is fast and does not require the relatively high-temperature exposure usually associated with ENIG, and the contrasting color makes it easier to inspect than OSP. While there is some consideration related to silver migration, anti-migration agents have been added to minimize the effect. Hot air solder leveling (HASL) was a widely used surface finish before lead-free solders for board-side surface finish. The process consists of immersing circuit boards in a solder alloy (the alloy is composed of tin (Sn) 99.7 % and copper (Cu) 0.3 % with traces of nickel (Ni)), and the excess solder is then removed by so-called air knives, which blow hot air across the surface of the board. The increased complexity of boards and finer pitches has exposed many limitations with the HASL finish, but with recent efforts to prevent Cu pad corrosion in harsh environments, HASL can serve as an option for some end-use conditions because it usually covers all exposed metal pads.

## The Correlation Between the Surface Finish and the Solder Joint

One important factor related to the Ni-containing surface finish is that not only the region where the surface finish is applied but that the other end of the solder joint is also affected by the introduction of Ni into the solder joint. As illustrated in Fig. 2.7, the schematic drawing on the process from ball attachment to board assembly, the surface finish at the package side affects the board-side interface composition. The case for OSP, SOP, or ImSn might be minimal because the main compositions are simply Sn and Cu, but for surface finish containing Ni or Pd, the board-side interface IMC is mostly affected and getting into a relatively complex structure. One example for electrolytic NiAu surface-finished samples in Fig. 2.13 compares two package side surfaces: one is the OSP surface finish and the other is the NiAu surface finish. The interface at the board side, even though it is OSP for both cases, is affected by the surface at the package side. The series of EPMA maps in Fig. 2.14 after reflow also show that the board interface IMC has Ni in it. This indicates that elements in the surface finish at the package side actually affect the opposite board side by first dissolving into the molten solder and then forming/

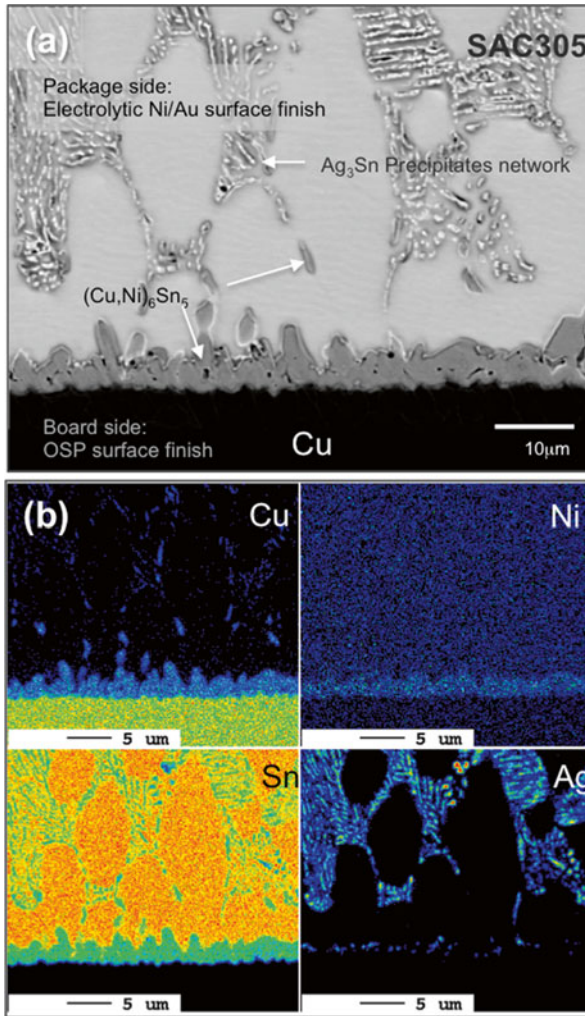




**Fig. 2.13** SEM microstructure after board assembly (unaged) of OSP (a–c) and NiAu (d–f) surface finishes: (a, d) Overall view of the joint, (b, e) higher magnification of the package side interface, and (c, f) board side interface

solidifying at the board interface. Thus, the surface finish composition is an important factor that directly influences the solder alloy composition and also the property of the joint. It is an additional source of elements, which can alter the composition of the solder alloy and at the same time affect the ultimate property of the material.

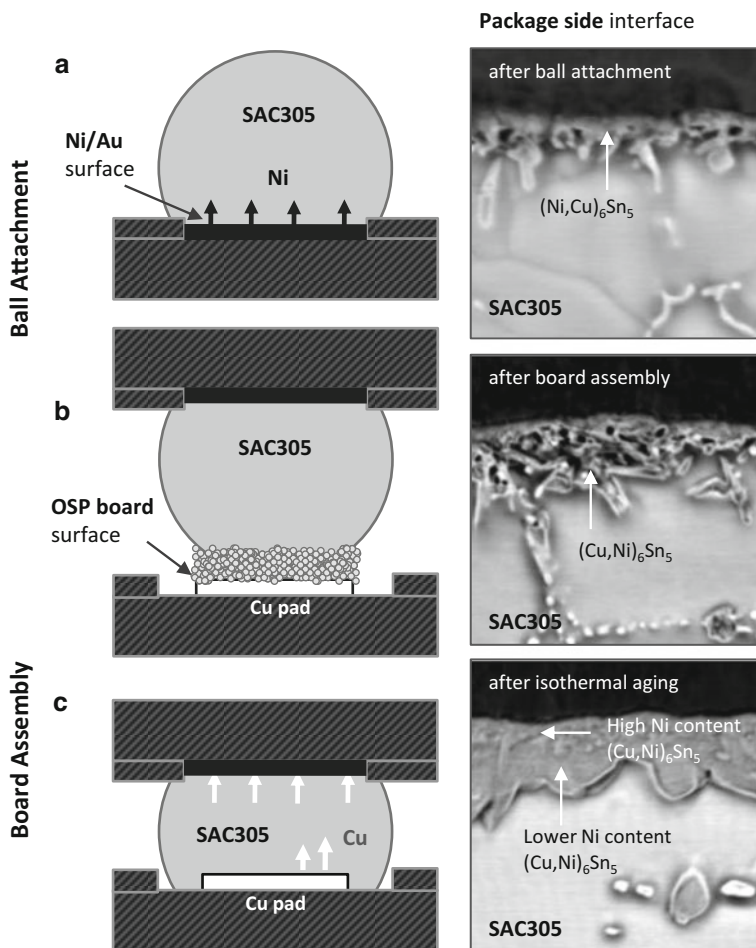
The additional Ni present on the board-side interface IMC during reflow occurs due to the diffusion of the Ni through the molten Sn and the formation of IMC at the time of solidification as shown in Fig. 2.15. At the ball attachment process reflow, a limited amount of Cu forms the  $\text{Cu}_6\text{Sn}_5$  IMC at the interface, and Ni from the surface finish diffuses into the IMC formation resulting in a  $(\text{Cu},\text{Ni})_6\text{Sn}_5$  IMC composition. Once the component is assembled to the board, a sufficient source of Cu is typically available from the board-side Cu pad. So, the IMC at the package-side interface forms additional IMC in the form of  $(\text{Cu},\text{Ni})_6\text{Sn}_5$ . Because after a certain thermal exposure, additional IMC formation or growth happened, but this time the composition is slightly different. After aging, the IMC became layer-like at the solder/Ni interface, and two kinds of  $(\text{Cu},\text{Ni})_6\text{Sn}_5$  with different Ni contents were detected as shown in Fig. 2.15c. The elemental map analysis using EPMA indicates that a continuous L- $(\text{Cu},\text{Ni})_6\text{Sn}_5$  layer with a lower Ni content formed above the H- $(\text{Cu},\text{Ni})_6\text{Sn}_5$  IMC, proving that the Ni is distributed nonuniformly in  $(\text{Cu},\text{Ni})_6\text{Sn}_5$ . This phenomenon will be further examined following isothermal aging in Chap. 4 and its effect on thermal and mechanical performance in Chaps. 5 and 6.



**Fig. 2.14** Board side interface and bulk region SEM image after board assembly with NiAu surface finish on the package side. (a) SEM, (b) Cu, Ni, Sn, and Ag EPMA maps

## Summary

In this chapter, we described interconnects at three scales: at the largest scale of connecting components, the structure of the package and boards, and then the microstructure of the interfaces between the solder and the package and board. We considered the variety of solder alloys and the process of board assembly and the importance of the package-side and board-side surface finish. Also, we



**Fig. 2.15** Interface microstructure development and IMC formation in the joint formation process. (a) Ball attachment to the package substrate reflow, (b) package placement on top of solder paste applied onto PCB, and (c) board assembly reflow

considered how the surface finish affects the microstructure and phases present in the intermetallic layer between the solder and package or board. Several additional factors and elements that make a simple structure into a complex system with various interactions have different roles that can improve one aspect of the interconnect and degrade another. In the next chapters, we will examine the mechanisms that govern the thermal and mechanical performance. Figure 2.16 shows the chapter summary.

Chapter Two describes the various types of packaging structures and the interconnections existing in manufactured products. The base structure of interconnects for different material set variations are described in the context of the various types of packaging strategies.

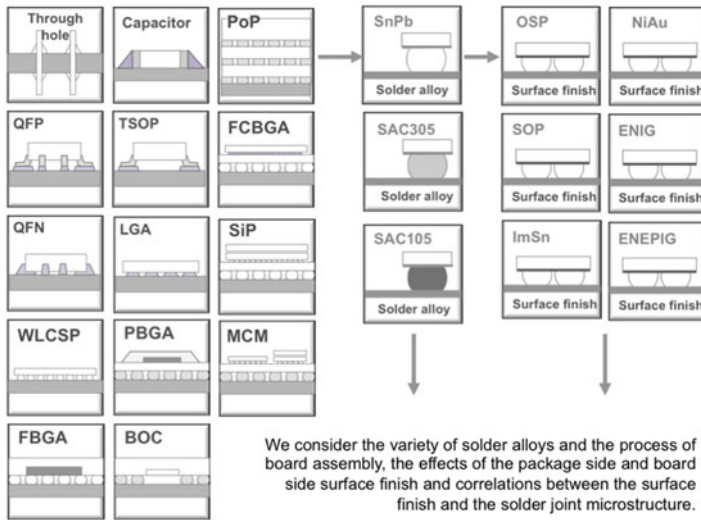


Fig. 2.16 Overall summary diagram of Chap. 2

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