Preface

Designing, fabricating, and testing of CMOS chips is a multi-billion dollar industry, spanning a multiplicity of engineering fields. Many of the complex tasks at each stage of design and production are handled with automated tools enabling rapid deployment of semiconductor chips in the marketplace at a low cost. Significant engineering resources are devoted to the development of these tools and in generation of associated software. Often engineers engaged in designing and testing of chips rely on automated tools and have limited exposure to the physical behavior of devices and circuits. Generally well proven and efficient, this approach lacks full utilization of university classroom learning in physics and engineering. Although detailed knowledge of a CMOS product may be daunting, a high-level view of various engineering aspects is extremely desirable when it comes to rapid diagnostics, problem resolution, and optimization of the entire production process.

Working with CMOS design, silicon technology development, and manufacturing teams in IBM's 180 to 32 nm CMOS technology nodes, we began deploying special test structures for DC and high-speed characterization of CMOS circuits. Initially our focus was on developing a methodology for bridging observed circuit behavior at high speeds to constituent component properties. Hardware data collected from the fab were compared to the simulated predictions using design automation tools. If the model-to-hardware mismatch was outside the specified range, silicon processes had to be modified to adjust the hardware to match the model. The alternative approach of updating the compact models to match the latest silicon technology was often not viable, considering the high cost of chip redesign and pressure to meet time-to-market demands. In either approach, it was imperative that the feedback from the test structures be accurate and reliable. Special techniques for design, test, and analysis were developed to quickly assimilate the information and to present it in a clear and concise manner so that experts as well as non-experts could follow the presentations and reports. These test structures have been placed in scribe-lines of CMOS chips and on dedicated test vehicles built at IBM and by IBM's partners in CMOS technology development. This integrated approach to design and test of electrical test structures is covered in our book entitled *Microelectronic Test Structures for CMOS Technology* published by Springer in August, 2011.

Some of these test structures, when embedded in CMOS product chips, proved to be very useful in product performance evaluation and debug. These monitors, primarily ring oscillators, are easier to analyze and model than the complex circuitry comprising the chip design itself. By proper configuration of embedded monitors, chip power and performance can be bridged back to device properties and to the EDA models and tools used for designing the chip circuitry. Changes in circuit characteristics can be monitored throughout the life of the product. Additional applications of such embedded test structures are in the areas of sorting and binning of chips and applying test limits with guardbands to meet warranted performance.

It has been our experience that understanding a complex system can be simplified by either observing the aggregate behavior of its components or by comparing the behavior of its key constituents to the system as a whole. Appropriately designed test structures and monitors can play a very important role in predicting the properties of the system. The knowledge derived is physically intuitive making it easier to detect model, design tool, and other software-related errors. A priori knowledge of physical behavior when applied to statistical data mining can considerably reduce the effort in resolving design and test issues. Cross-checking of data collected from embedded monitors, product chips, and system tests for consistency makes the findings conclusive with a high degree of confidence.

In *CMOS Test and Evaluation*: *A Physical Perspective*, we have attempted to describe the relationship between basic circuit components (resistors, capacitors and diodes, and MOSFETs) and a complex CMOS chip with as many as several billion transistors. Our approach is to provide an overview with examples to link various aspects of CMOS technology, design, and test. Simulated data representative of that acquired during electrical testing in product manufacturing and qualification are used to illustrate concepts and to demonstrate data visualization and presentation. Exercises are included at the end of each chapter. Many of the circuits described and incorporated in the examples and exercises enable observation through simulation of features that are not experimentally assessable, often providing clearer insight into aggregate behavior.

We hope that this book will prove useful in preparing physics and electrical engineering students for building a career in the semiconductor industry as it faces new challenges, as well as serving as a useful reference for practitioners in the field.

We are thankful to our former colleagues in IBM's Server and Technology Group and in IBM's Research Division for close collaborations throughout our tenure in IBM.

How to Use This Book

There are at least two effective ways that this book can be used. The first is by practitioners already confronting real problems on the test floor. As emphasized in the 2013 ITRS Roadmap, the CMOS test arena is in a state of rapid change. While this book cannot possibly address all the known changes or foresee many more to

come, the underlying physics of it all has not and will not change. In each chapter we attempt to present a high-level summary of the subject matter followed by a number of exercises, many of which relate to actual problems encountered in the field. While none of these may be identical to the crisis of the moment, the approach to resolution that we advance in the formulation and solution of exercises is based on physical insight, is very general in nature, and will apply to a wide range of new problems as they arise.

The second way this book can be used is in the education and training of science and engineering students preparing to work in the semiconductor test enterprise. It is in no way an attempt to replace or compete with any of the fine existing texts that focus in great depth on particular areas of design, fabrication, and test. It is assumed that students will have already mastered the contents of a number of these. It is our intent to build on them to provide an integrated technical view of CMOS test as a whole and to provide students with a set of exercises to help them develop physical insight. As mentioned above, the field of semiconductor test is changing rapidly and will continue to do so. Those who desire to enter and prosper in this field must be prepared to evolve with it. It is our goal to help them prepare for this journey through examples and exercises based on real problems encountered in CMOS manufacturing test, with an emphasis on gaining underlying physical insight, along with high-level topical summaries.

The scope of this book and a brief description of chapter contents are covered in Sect. 1.8. The introductory material in the beginning of the chapters can be covered quickly with much of the time and effort devoted to circuit simulations and data analysis. The aim is to help develop an intuitive physical understanding of the material covered without becoming bogged down in the details.

It is essential to have access to compact device models for different technology nodes or from different foundries, together with a SPICE simulation environment. By working through the examples and exercises, students can learn to cross-check the results and quickly spot and correct errors. Presenting conclusions and the line of reasoning in a clear and unambiguous manner is extremely important. Examples of this are presented in the text as well as in solutions to exercises published on the web.

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http://www.springer.com/978-1-4939-1348-0

CMOS Test and Evaluation
A Physical Perspective
Bhushan, M.; Ketchen, M.B.
2015, XIII, 424 p. 338 illus., Hardcover
ISBN: 978-1-4939-1348-0