
Contents

1	Introduction	1
1.1	Simplicity in Complexity	2
1.2	CMOS Design and Test Overview	4
1.3	Tests Types and Timelines	5
1.4	Test Economics	8
1.5	Future Test Challenges	9
1.6	Silicon Technology and Models	10
1.7	Data Analysis and Characterization	10
1.8	Scope of the Book	11
1.9	Summary and Exercises	13
	References	15
2	CMOS Circuits Basics	17
2.1	Circuit Components and Building Blocks	19
2.1.1	MOSFETs	21
2.1.2	Interconnects	28
2.1.3	Passive R and C Components	30
2.1.4	Logic Gates	31
2.2	SPICE Simulations	34
2.2.1	PTM (BSIM)	37
2.2.2	MOSFET Characteristics	38
2.2.3	Standard Cell Library Book Characteristics	50
2.2.4	Delay Chains	64
2.2.5	Ring Oscillators	71
2.2.6	Comparison of Logic Gate Characterization Methods	75
2.2.7	Monte Carlo Analysis	77
2.3	Summary and Exercises	79
	References	83
3	CMOS Storage Elements and Synchronous Logic	85
3.1	CMOS Chip Overview	86
3.1.1	I/O Circuits	87

3.1.2	Combinational Logic	88
3.1.3	Clock Generation and Distribution	91
3.2	Sequential Logic and Clocked Storage Elements	93
3.2.1	Level-Sensitive Latches	95
3.2.2	Edge-Triggered Flip-Flops	98
3.2.3	Setup and Hold Times	100
3.2.4	Register Files	101
3.3	Memory	102
3.3.1	SRAM	103
3.3.2	DRAM	108
3.4	Circuit Simulations	109
3.4.1	SRAM SNM	109
3.4.2	Logic Data Path	112
3.5	Summary and Exercises	121
	References	123
4	IDDQ and Power	125
4.1	Silicon Technology Scaling and Power	127
4.2	IDDQ	128
4.2.1	MOSFET Leakage Currents	129
4.2.2	IDDQ of Logic Gates and Memory Cells	130
4.2.3	IDDQ Estimation in Design and Measurements	135
4.2.4	Defect Generated IDDQ	137
4.3	Power	140
4.3.1	Measuring Power	140
4.3.2	AC Power	141
4.3.3	DC Power	146
4.4	Total Power	148
4.5	Power Management	151
4.5.1	Power Management in Chip Design	152
4.5.2	System Power Management	155
4.6	Summary and Exercises	155
	References	157
5	Embedded PVT Monitors	159
5.1	Placement and Integration	160
5.2	Silicon Process Monitors	162
5.2.1	MOSFETs	162
5.2.2	Delay Chains	163
5.2.3	Ring Oscillators	166
5.3	Power Supply Voltage and Noise Monitors	170
5.4	Critical Path Monitors	173
5.5	Temperature Monitors	174
5.6	Circuit Stages for ROs and Delay Chains	177
5.6.1	MOSFET Parameter Extraction	182
5.6.2	SRAM Stage Designs	186

5.6.3	Silicon Process-Sensitive Suite	188
5.6.4	Strengths and Limitations of RO-Based Monitors	192
5.7	Data Collection and Characterization	193
5.8	Summary and Exercises	197
	References	199
6	Variability	201
6.1	Sources and Impact of Variations	202
6.1.1	Silicon Process Variations	205
6.1.2	Random Variations	211
6.1.3	Voltage Variations	212
6.1.4	Temperature Variations	214
6.2	Variability Characterization	215
6.2.1	Silicon Manufacturing Tests	216
6.2.2	On-Chip Embedded PVT Monitors	216
6.2.3	Functional Parameters	218
6.2.4	Optical Imaging	218
6.2.5	Thermal Imaging	220
6.3	Minimizing Variations	220
6.3.1	Chip Design and Floorplanning	221
6.3.2	Reticle and Wafer Assembly	222
6.3.3	Silicon Process Improvements	222
6.4	Accommodating Variability in Circuit Design	223
6.4.1	Simulation Corners	225
6.4.2	Impact of Random Variability on Circuits	227
6.5	Summary and Exercises	235
	References	239
7	Electrical Tests and Characterization in Manufacturing	241
7.1	Digital CMOS Chip Tests	242
7.1.1	Test Flow	243
7.1.2	Test Equipment	245
7.1.3	DC and AC Parametric Tests	246
7.1.4	Structural Faults and ATPG	246
7.1.5	IDDQ Tests	251
7.1.6	DFT and Diagnostics	254
7.1.7	Scan Design	255
7.1.8	Built-in Self-Test	257
7.1.9	Boundary Scan	258
7.1.10	Measurements of T_{cmin} , V_{min} , and AC Power	259
7.2	Yield	260
7.2.1	Defect Limited Yield	261
7.2.2	Cycle Time Limited Yield	263
7.3	Failure Analysis	265
7.4	Product Chip Characterization	267

7.4.1	Silicon Manufacturing Line Tests	267
7.4.2	Silicon Process-Split Hardware	269
7.4.3	Embedded Process Monitors	270
7.4.4	Aggregate Behavior	277
7.4.5	Silicon Manufacturing Process Window	278
7.5	Adaptive Testing and Binning	278
7.6	Summary and Exercises	281
	References	284
8	Reliability	285
8.1	Reliability and End-of-Life	286
8.1.1	Accelerated Stress Tests and Failure Rates	288
8.2	CMOS Circuit Performance Degradation Mechanisms	292
8.2.1	Bias Temperature Instability	292
8.2.2	Hot Carrier Injection	300
8.2.3	Time-Dependent Dielectric Breakdown	301
8.2.4	Electromigration	302
8.2.5	Soft Errors	303
8.3	Managing Reliability	303
8.3.1	Voltage Screening	304
8.3.2	Burn-In	305
8.3.3	Guard-Banding	306
8.4	Summary and Exercises	309
	References	310
9	Basic Statistics and Data Visualization	311
9.1	Basic Statistics	312
9.1.1	Probability	314
9.1.2	Statistical Distributions	315
9.1.3	Sample Size Effects	318
9.1.4	Non-normal Distributions	321
9.2	Data Filtering, Correlation, and Regression	323
9.3	Statistical Variations	326
9.3.1	Range of Systematic and Random Variations	327
9.3.2	Sensitivity Analysis of a Function	330
9.4	Bayesian Statistics	333
9.5	Data Visualization	334
9.6	Summary and Exercises	343
	References	344
10	CMOS Metrics and Model Evaluation	347
10.1	Measurement Standards	348
10.2	Scaling Trends in CMOS Products	351
10.3	CMOS Performance Metrics	355
10.3.1	MOSFET Performance	355

10.3.2	Interconnect Performance	363
10.3.3	Logic Gate Performance	365
10.4	CMOS Power-Performance-Density Metrics	367
10.4.1	Circuit Density	368
10.4.2	Energy and Power Density	369
10.4.3	V_{DD} Dependencies of Different Metric Parameters	373
10.4.4	Summary of Performance Metrics	374
10.5	Compact Models and EDA Tool Evaluation	374
10.5.1	BSIM Models	376
10.5.2	Layout Parasitic Extraction	383
10.5.3	Timing and Power Tools	385
10.6	PD-SOI vs. Bulk Silicon Technology	386
10.7	Closing Comments on CMOS Technology Evaluation	394
10.8	Summary and Exercises	395
	References	398
Appendix A: MOSFET and Logic Gate Parameters		
	(PTM HP Models)	399
Appendix B: BSIM4 PTM Models		407
Glossary		413
Index		421

CMOS Test and Evaluation

A Physical Perspective

Bhushan, M.; Ketchen, M.B.

2015, XIII, 424 p. 338 illus., Hardcover

ISBN: 978-1-4939-1348-0