

Preface

The design of the clocking subsystem represents a crucial aspect in CMOS VLSI integrated circuits, as it strongly affects not only the chip performance, but also its overall energy consumption. Independently of the nature of the system (fully synchronous, globally asynchronous, locally synchronous), any clocking subsystem can be subdivided into three main parts: similar to the structure of a tree, the root is represented by the clock generation, the branches are represented by the circuits devoted to clock distribution, and the clocked storage elements (i.e., latches and/or flip-flops) are the final leaves. Flip-flops (or, more in general, clocked storage elements) are among the most important cells used in digital systems, such as microprocessors. They separate the various stages that pipelines are made up of, hold the state, and prevent early transitions that would be otherwise determined by fast paths. Overall, flip-flops synchronize and regulate the entire flow of data within a digital system.

In high-performance systems, relatively little combinational logic is contained by each pipeline stage, hence flip-flops introduce a timing overhead that is a significant fraction of the clock cycle. On the other hand, due to the high switching activity of the clock signal, the overall dissipation of the clocking subsystem can be as high as $30 \div 50$ % of the overall chip energy budget. It is crucial to keep this energy within reasonable bounds, since it reduces the energy available for computation under a given energy budget, and hence it limits the overall performance in power-limited systems (i.e., the vast majority of practical cases).

The above performance and energy issues, together with the need for adequate robustness and ability to deal with clock uncertainties, make the flip-flops design quite tricky. Accordingly, these circuits have been extensively studied in the past, and significant effort has been devoted to propose new circuit solutions and to properly select the flip-flop topology depending on the requirements set by the application. Such a task is further complicated by the issues that are naturally posed by nanometer technologies, such as the impact of (a) layout parasitics associated with interconnections, degrading both speed and energy, (b) leakage, affecting energy both in active and in standby mode, and (c) process and environmental variations, which require considerable design margin that negatively impact both performance and energy. Unfortunately, the existing body of work on flip-flop design largely neglects all these effects, and a more thorough analysis is needed to allow the designer to take the above issues into account.

The energy-aware design, the comparison, and the selection of the most appropriate flip-flop topology for a targeted application has been recently investigated by the authors. The main focus of this book is to provide the reader with a deep understanding of the challenges associated with flip-flop design, and with clear guidelines to select the most suitable topology when all the above-mentioned nanometer issues are included. Basic foundations are provided to set the stage for the comprehension of analyses and results. Unitary and well-grounded simulation and evaluation methodologies are presented, and many analytical derivations are included to gain an insight into the main dependencies of important parameters on circuit properties. Finally, several quantitative results are reported to emphasize the practical perspective of the book, as a result of an extensive and thorough simulation analysis.

The book can be used as a reference to practicing engineers working in VLSI design and also by undergraduate, graduate, and postgraduate students who are already familiar with basic electronics and digital circuits design.

The outline of the book is as follows. The first three chapters contain all the theoretical background (including novel modeling approaches), which is then used in the remainder of the book. Chapter 1 describes the well-known Logical Effort method, which is extensively adopted throughout the book for both modeling and design purposes.

Chapter 2 is about the energy consumption of digital circuits and the adopted framework to evaluate the efficiency of the energy-delay tradeoff. The adoption of suitable figures of merit and the concept of energy-efficient curve are discussed. A novel methodology to optimize transistor sizes is introduced to manage the energy-delay tradeoff. In this chapter, it is also shown that Logical Effort enables the derivation of practical design constraints, when exploring the energy-delay space.

Chapter 3 provides an overview of the clocking subsystem and clocked storage elements, introducing the main timing and energy parameters. A general classification of clocked storage elements is presented, and their basic properties are reviewed.

A comprehensive design strategy for nanometer CMOS flip-flops through circuit energy-delay optimization is presented in Chap. 4. The methodology also accounts for the important contribution of interconnect parasitics, based on the Logical Effort and energy-efficient design methodologies described in the first two chapters.

The results of a wide comparison of 19 flip-flop topologies belonging to four classes (Master-Slave; Pulsed both Implicit and Explicit; Differential and Dual-Edge-Triggered), and selected among the most representative and best known topologies, are reported in Chap. 5. The exploration of several tradeoffs, including energy, delay, leakage, area, and clock load allows for comparing flip-flops in a very general manner.

Chapter 6 presents results on the optimization of clock buffers, based on the explicit analysis of their interaction with flip-flops and using the clock slope as a design parameter.

The impact of variations on flip-flops is analyzed in Chap. 7. Process/voltage/temperature (PVT) variations, as well as variations induced by the clock distribution network (i.e., clock slope variations) are thoroughly analyzed and compared for Single-Edge Triggered flip-flops. As far as Double-Edge Triggered flip-flops are concerned, results are summarized in the Appendix of the same chapter to improve the readability.

Finally, in Chap. 8, a novel class of ultrafast and extremely energy-efficient flip-flop topologies that were recently proposed by the authors is presented, together with experimental results from an integrated prototype in 65 nm CMOS. The proposed topologies achieve the best speed and energy efficiency in the high-speed to minimum *ED* product region of the design space that have ever been reported so far.

Flip-Flop Design in Nanometer CMOS

From High Speed to Low Energy

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