Chapter 2
3D/TSV-Enabling Technologies

Three-dimensional (3D) integration is a promising alternative option to traditional two-dimensional (2D) planar chips. The 3D integration is mainly concerned with the communication infrastructure between different stacked dies of future multi-core system-on-chip (SoC) and network-on-chip (NoC). Among several 3D integration technologies, the through silicon via (TSV) approach is the most promising one and therefore is the focus of the majority of 3D integration R&D activities. However, there are challenges that should be overcome before the production of TSV-based 3D integrated circuits (ICs) becomes possible, e.g., electrical modeling challenges, thermal and power challenges, technological challenges, design methodology challenges, and computer-aided design (CAD) tool development challenges. The manufacturability of TSV-based 3D-ICs is an important issue for realizing real 3D-ICs designs.

2.1 3D/TSV Technology

The small-scale production of integrated circuits (ICs) started in the early 1960s. The modern-day ICs may have billions of transistors. The functionality scales by reducing the size of the transistors and also by increasing the transistor count per unit area of the processor die. More transistors are added to processors with each technology node. System-on-chip (SoC) was introduced in order to integrate all the components on a single substrate. SoC has incredible functionality, having processor, digital logic, memory, embedded intelligence, and analog components on a single die. However, interconnect length is a critical issue for SoC due to increase in the chip dimensions. Mixed signal integration is another issue for present-day SoC as the noisy digital part cannot be placed in close proximity to the sensitive analog part. In addition to this, same technology node has to be followed for different components of SoC which may place stringent requirements on analog and radio frequency (RF) components. Three-dimensional (3D) integration with through silicon vias (TSVs) is, therefore, an obvious choice for mixed technology applications compared to SoC. In other words, increasing drive for the integration of different

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Table 2.1 A comparison between alternative design implementations

Property	Single chips	SoC	3D
Modular flexibility	High	Low	Medium
System performance	Low	Medium	High
Physical dimension	Large	Medium	Small
Complexity of fabrication	Low	Medium	Medium
Cost	Low	Medium	High
CAD tools and design methodologies	Available	Available	Not deployed yet

signals (analog, digital, RF) and technologies (SOI, HBTs, GaAs, strained silicon, and so on) is introducing various design concepts, for which existing planar (3D) technologies may not be suitable, so 3D-ICs are introduced.

The purpose of 3D integration is either to partition a single chip into multiple strata to reduce global interconnect length or stacking of chips together using TSVs. Increasing the number of strata from one to four reduces the length of the longest interconnect by 50% with 75% improvement in latency and 50% improvement in interconnect energy dissipation. Using 3D integration, the clock frequency can be increased by 3.9× and area and power can be reduced by 84%. Energy dissipation of long on-chip wires can be reduced by 54% by using 3D interconnects in a 45-nm technology node. 3D integration provides the potential for a tremendously increased level of integration per unit footprint compared to its two-dimensional (2D) counterpart.

The migration from 2D to 3D-ICs brings higher bandwidth, reduced power consumption, and higher integration density. The improved performance, reduced timing, and small form factors are also key drivers for 3D integration and TSV interconnect technology.

A qualitative comparison regarding the benefits introduced by the 3D integration process, compared to existing system design approaches, is summarized in Table 2.1 and illustrated in Fig. 2.1.

Another classification to technology is divided into SiP, SoP, SoC, and 3D, where system-in-package (SiP) can hire different chips/dies from different processes in one package. This can be quite good, for example, where you have to get complementary metal oxide semiconductor (CMOS)-based parts and high-frequency (HF) components in one package (wireless apps). The latter is quite difficult to do in CMOS process. We use SiP for chips integrating different kinds of technologies like RF, SOI, etc. making the coexistence of these different technologies on the same chip possible. SiP is based on bonding wires (Fig. 2.2). System-on-package (SoP) is a "technical" term for printed circuit board (PCB) with bare dies in a single package (Fig. 2.3). The 3D approach has a considerable edge in feature size compared to SoP as shown in Table 2.2.

3D integration technology provides increased performance in many design criteria as compared to the current 2D approaches, since 3D-ICs, which contain multiple layers of active devices, extensively utilize the vertical dimension to connect components and are expected to address interconnect delay-related prob-

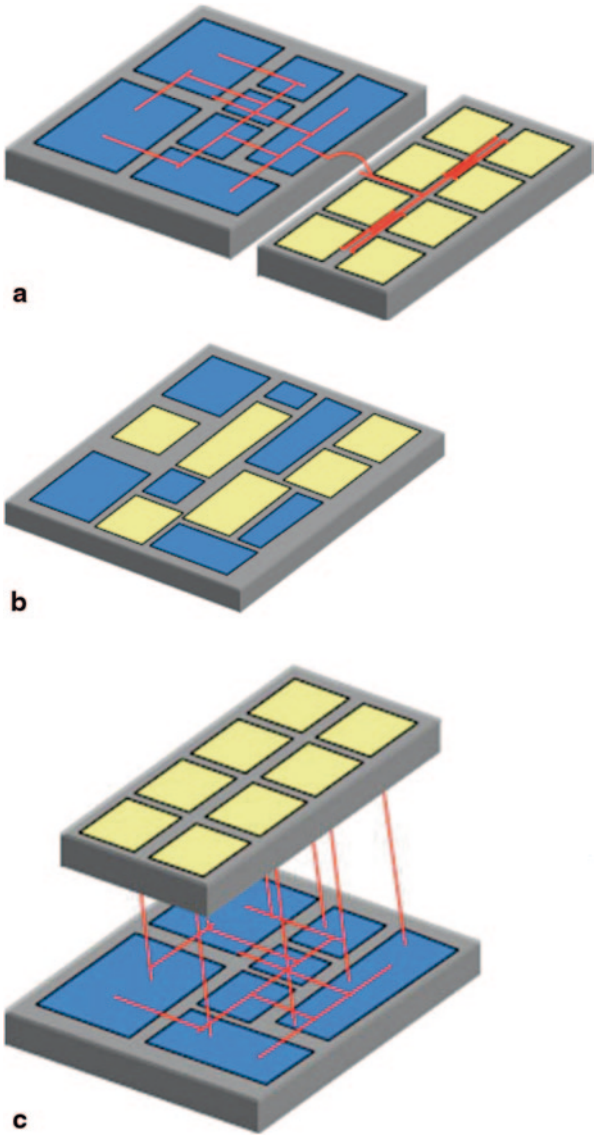

Fig. 2.1 A comparison between alternative design implementations: **a** single chips, **b** SoC, and **c** 3D [1]

lems by the use of short wires in 3D designs. The distance between layers is relatively small (~30–300 μm) in 3D-ICs compared to inter-router distance in 2D-ICs (~1000 μm or more) as is schematically shown in Figs. 2.4 and 2.5. These shorter wires will decrease the average load capacitance and resistance and decrease the number of repeaters which are needed to regenerate signal on long wires. More importantly, 3D technology enables the integration of heterogeneous technologies. In the 3D design, a 2D chip is divided into a number of different blocks, and

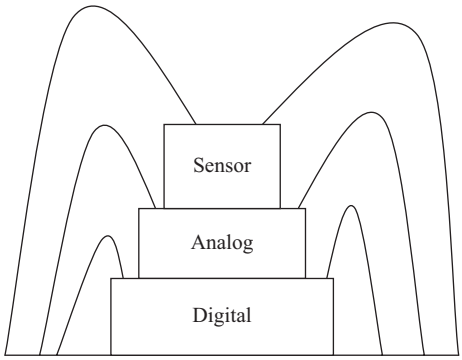

Fig. 2.2 SiP technology, where it can hire different chips/dies from different process in one package [1]

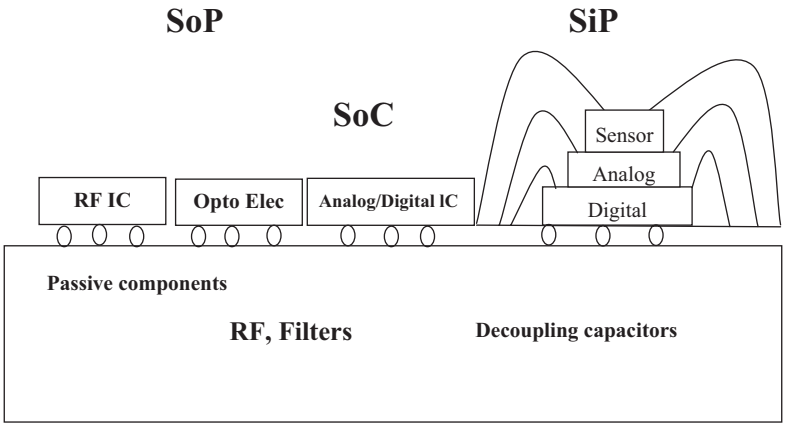

Fig. 2.3 SoP technology, where it is a "technical" term for PCB with bare dies in a single package [1]

Table 2.2 Comparison of feature sizes between 3D-IC and SoP

Feature	3D	SoP
Smallest via size (μm)	0.14	1
Largest via size (μm)	10	90
Smallest via pitch (μm)	0.4	10
Largest via pitch (μm)	200	200
Minimum silicon thickness (μm)	2	4
Maximum silicon thickness (μm)	70	300

each one is placed in a separate layer of silicon where each layer is stacked on top of each other, as schematically shown in Fig. 2.6. This may be exploited to build a SoC by placing different circuits with performance requirements in different lay-

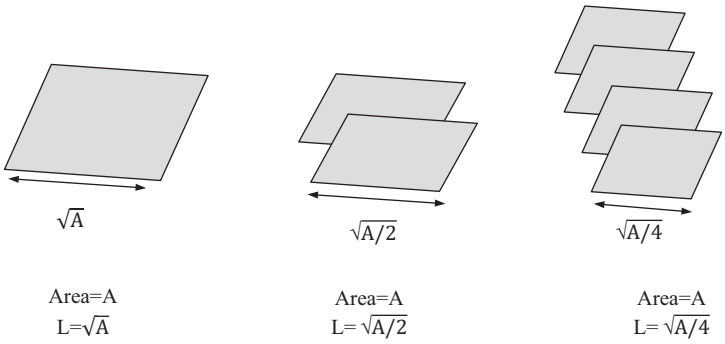

Fig. 2.4 Reduction in wire length where the original 2D circuit is implemented in two and four planes

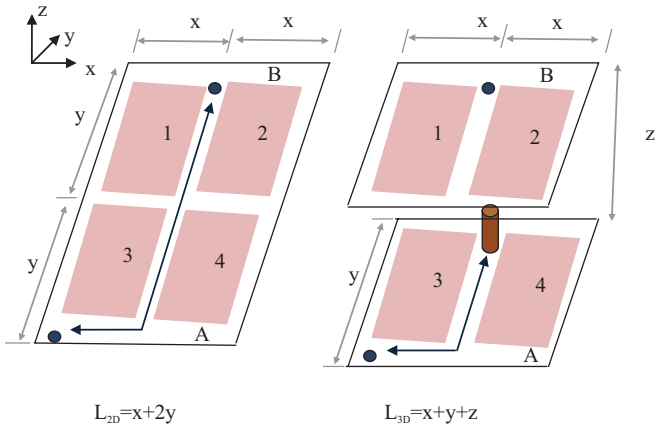

Fig. 2.5 Reduction in wire length where the original 2D circuit is implemented in two planes ($z<y$)

ers which enables novel "More than Moore" applications [1, 2]. Moreover, the 3D integration can be implemented on different levels: technology level, architecture level, or circuit level (Fig. 2.7). The advantages of 3D integration are summarized in Table 2.3.

In 3D integration, the communication among the stacked ICs and embedded components requires vertical interconnections. Since processing the vertical interconnections is challenging compared to the planar ones, the electrical and mechanical characteristics of the vertical interconnections can be a bottleneck for achieving the required system performance. Thus, various types of vertical interconnections are still being proposed. Several interconnection elements are already popular in industry. Figure 2.8 shows typical 3D structures with four types of interconnections,

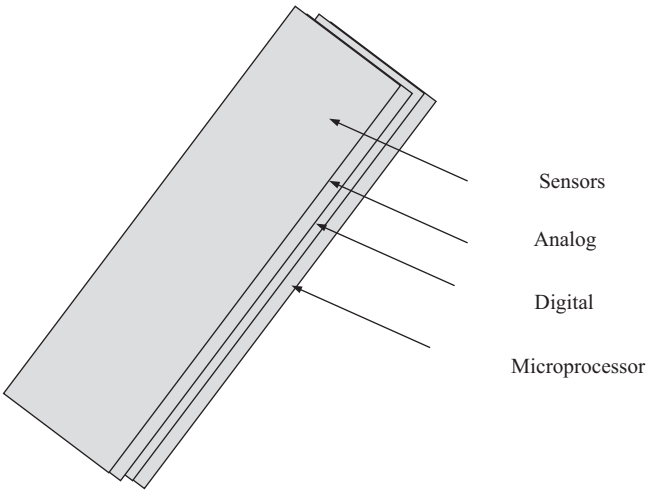

Fig. 2.6 A possible design for a 3D SoC (heterogeneous technologies)

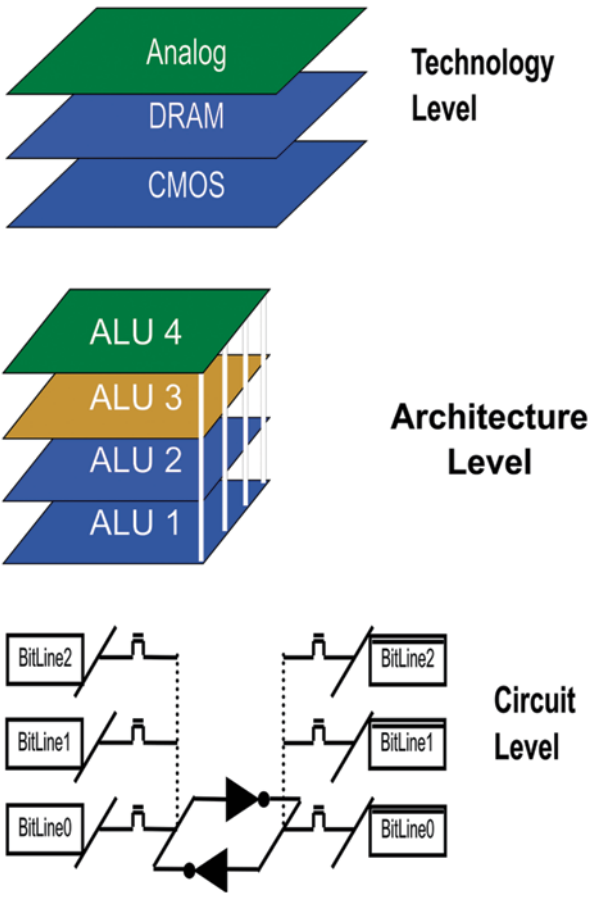

Fig. 2.7 Different levels of 3D integration: technology level, architecture level, and circuit level [2]

Table 2.3 Advantages of 3D integration

Advantages of 3D integration
1. Heterogeneous integration of devices
2. Reduced distance of global interconnects
3. Higher integration density
4. Higher form factor
5. Faster access between memory and logic device modules
6. Reduced overall resistance
7. Reduced power
8. Reduced packaging cost
9. Elimination of wire bonds
10. EMI and shielding
11. High bandwidth computer architectures
12. Use only one set of I/O pads to minimize parasitics due to I/O
13. Better reliability
14. Override the saturation of Moore's law

including bonding wires, TSV interconnections (which is a new silicon-based 3D packaging structure), metal bumps, and contactless communication (inductive and capacitive coupling). Table 2.4 summarizes the main difference between those four types of interconnects. It is clear that to improve electrical performance, TSV interconnections are becoming a major choice to replace the bonding wires and metal bumps [3]. TSV is not new, but now it is finally becoming a viable option [4].

2.2 TSV Structure

The general structure of a TSV (Fig. 2.9) is typically a cylinder with a uniform circular cross section of a conducting material (copper) surrounded by an insulator (silicon dioxide) which is intended to prevent leakage and resistive coupling through the substrate (silicon). 3D-ICs, which contain multiple layers of active devices, extensively utilize the vertical dimension to connect components.

Usually, the TSV interconnections are fabricated as an array in a silicon substrate. TSVs distribution is mainly determined during physical design such as partitioning, placement, and routing. TSVs can be laid out in a row, within a regular matrix, or within an irregular distribution depending on the applications and technology constraints [1–4].

The characteristics of a TSV are dependent on its geometrical parameters (such as the TSV diameter, height, pitch, and oxide layer thickness) and electrical parameters (such as the metal conductivity, the oxide permittivity, and the silicon substrate resistivity). The International Technology Roadmap for Semiconductors (ITRS) for the TSV is shown in Table 2.5.

The fundamental difference between TSVs and vias found in packages and PCBs is the semiconducting material surrounding them. Instead of looking at TSVs as

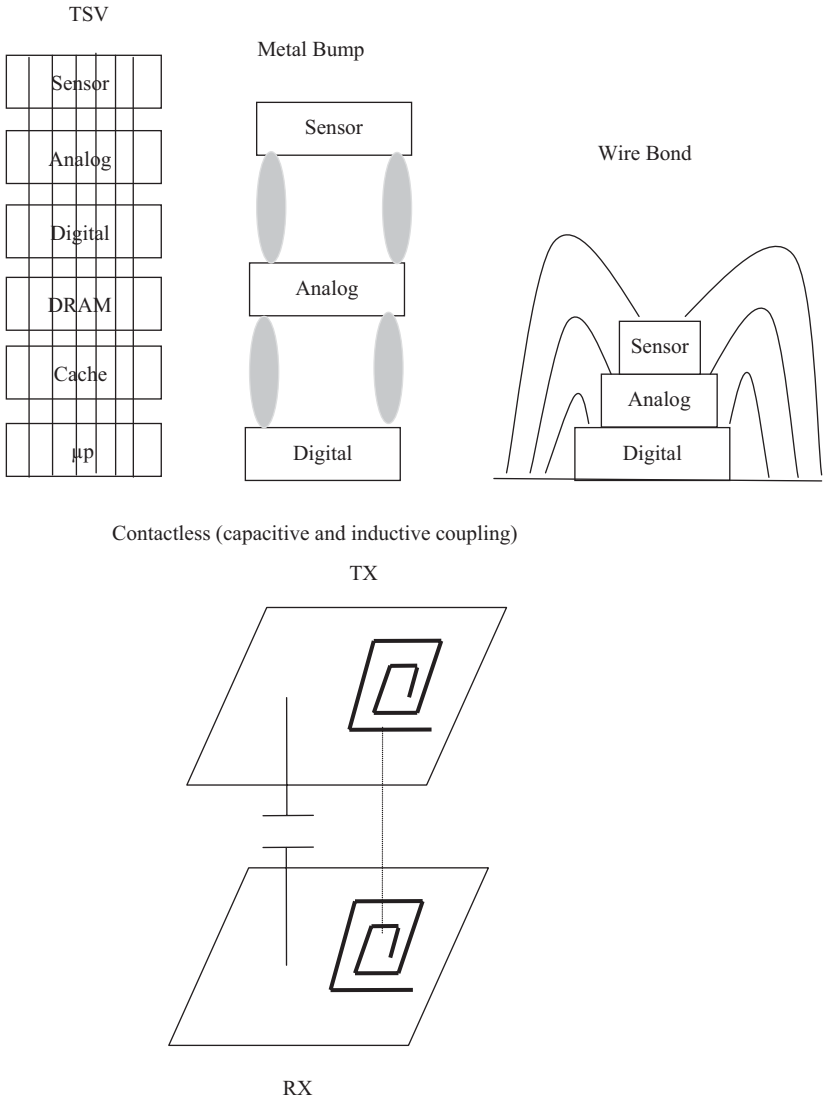

Fig. 2.8 Examples of 3D structures with interconnection elements, including bonding wires, TSV interconnections (which is a new silicon-based 3D packaging structure), metal bumps, and contactless communication (inductive and capacitive coupling)

wires, maybe other opportunities exist where the semiconducting properties of the substrate could be used to make the TSV function more like a device. With this thinking, the usefulness of the TSV can be enhanced and could potentially lead to enhanced performance and provide solutions for solving other problems being faced in 3D integration (the TSV can be considered to be a device, rather than using it only as a method of interconnect).

Table 2.4 Comparison among different 3D assembly technologies

Technologies	Advantages	Disadvantages
Wire bonding	Flexible connection High reliability Mature processing and cost-effective	Low density Long wiring Poor signal integrity Large pad area
Metal bumps	Short length	Large solder ball
TSVs	Short length High density Small footprint	Complex fabrication
Contactless (inductive and capacitive coupling)	Reducing the length of electrical paths Simple fabrication	Less reliability Cross talk and coupling issues Size of inductors (inductive coupling)

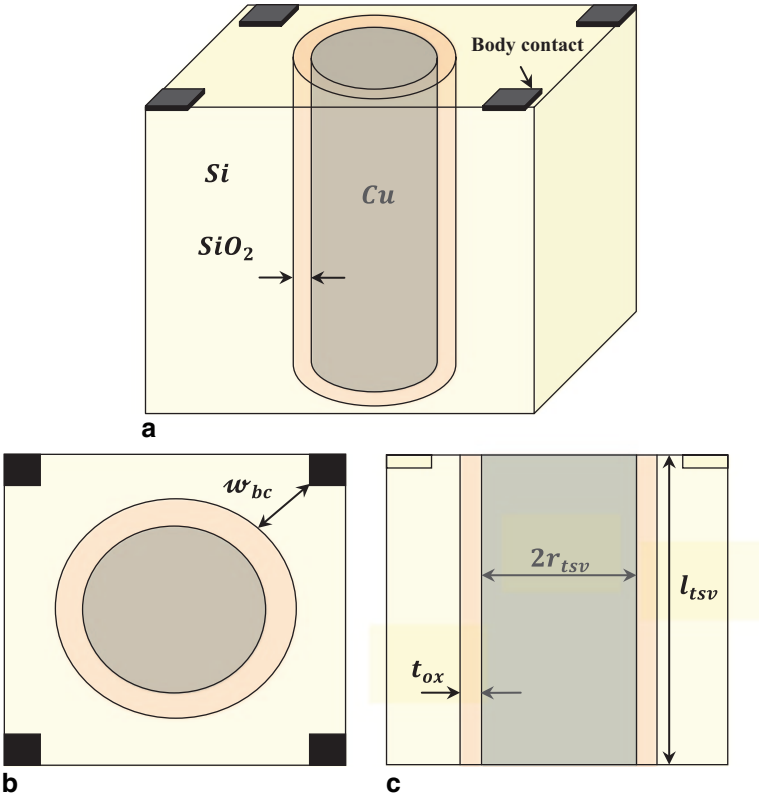

Fig. 2.9 The TSV structure assuming a uniform circular cross section of copper surrounded by an oxide inside a silicon substrate: **a** 3D view, **b** top view, and **c** side view

Table 2.5 ITRS for TSV

Parameters	2009–2012	2012–2015
Minimum TSV diameter (μm)	4–8	2–4
Minimum TSV pitch (μm)	18–16	4–8
Minimum TSV depth (μm)	20–50	20–50
Minimum TSV aspect ratio	1:10	1:20
Minimum contact pitch (μm)	20	10
Number of tiers	2–3	2–4

Table 2.6 3D and 2D wire model

3D wire model	2D wire model
Wires with finite width , thickness, and finite length 	Wires with finite width and thickness, but infinite length 

Fig. 2.10 Coaxial cable cross section

Since TSVs are surrounded by silicon, if you turn it laterally, they look like metal oxide semiconductor (MOS) capacitors. Therefore, biasing the silicon substrate should alter the capacitance of the TSVs. So, now the TSVs are no longer a wire but behave as a variable capacitor (depending on the bias voltage), similar to a device (such as a MOS capacitor).

The difference between 3D interconnect and 2D interconnect is that 2D wires have finite width and thickness, but infinite length. 3D wires have finite width, thickness, and finite length. These differences are depicted in Table 2.6. The shape can be rectangular or circular. But, from the simulation results, it can be found that the shape can affect the results very little. Moreover, a TSV is not like a coaxial cable which does not contain semiconductor as depicted in Fig. 2.10.

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