Preface

Embedded computer systems are pervasive in our modern society with a wide application domain such as automotive and avionic systems, electronic medical equipment, telecommunication devices, industrial automation, and consumer electronics.

At the so-called *Electronic System Level (ESL)*, designers start with a specification model of the system and follow a systematic top-down design approach to refine the model to lower abstraction levels step-by-step by adding implementation details. ESL models are usually written in C-based *System-Level Description Languages (SLDLs)*, and contain the essential features such as clear structure and hierarchy, separate computation and communication, and explicit parallelism. Typically, ESL models are validated through simulation. Fast yet accurate simulation is highly desirable for designing efficient and effective systems.

In this book, we review and study the parallel discrete event simulation for electronic system-level designs on simulation platforms with multiple CPU cores. After a survey of state-of-the-art approaches, we describe a new technique, namely *Out-of-Order Parallel Discrete Event Simulation (OoO PDES)*, to effectively exploit the available computational resources on multi-core simulation hosts for cycle-accurate simulation. OoO PDES breaks the global simulation-cycle barrier of traditional DE simulation by localizing the simulation time into each thread, carefully delivering notified events, and handling a dynamic management of simulation sets. Potential conflicts caused by parallel accesses to shared variables and out-of-order thread scheduling are prevented by an advanced predictive static model analyzer in the compiler. As such, OoO PDES allows the simulator to effectively exploit the parallel processing capability of the multi-core system to achieve fast speed simulation without loss of simulation and timing accuracy.

Moreover, ESL models must contain explicit and efficient parallelism in order to utilize parallel processing for low power and high performance. Parallelization is a particularly important but also very difficult task in system modeling. Based on our parallel simulation infrastructure, we further present the automatic approaches that can help the designer to quickly narrow down the debugging targets in faulty ESL models with parallelism.

Overall, our work provides an advanced parallel simulation infrastructure for efficient and effective system-level model validation and development so as to build better products in shorter time.

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