

# Contents

<b>1</b>	<b>Introduction</b>	1
1.1	System-Level Design	3
1.1.1	Levels of Abstraction	4
1.1.2	The Y-Chart	5
1.1.3	System-Level Design Methodologies	6
1.1.4	Electronic System-Level Design Process	8
1.2	Validation and Simulation	10
1.2.1	Language Support for System-Level Design	10
1.2.2	System Simulation Approaches	12
1.2.3	Discrete Event Simulation	13
1.3	Goals	15
1.4	Overview	16
1.5	Related Work	17
1.5.1	The SpecC Language	17
1.5.2	The SystemC Language	22
1.5.3	The System-on-Chip Environment Design Flow	22
1.5.4	Multicore Technology and Multithreaded Programming	25
1.5.5	Efficient Model Validation and Simulation	27
<b>2</b>	<b>The ConcurrnC Model of Computation</b>	29
2.1	Motivation	29
2.2	Models of Computation	30
2.3	ConcurrnC MoC	32
2.3.1	Relationship to C-based SLDLs	32
2.3.2	ConcurrnC Features	33
2.3.3	Communication Channel Library	34
2.3.4	Relationship to KPN and SDF	35
2.4	Case Study	35

<b>3</b>	<b>Synchronous Parallel Discrete Event Simulation</b>	39
3.1	Traditional Discrete Event Simulation	39
3.2	SLDL Multithreading Semantics	41
3.2.1	Cooperative Multithreading in SystemC	41
3.2.2	Pre-emptive Multithreading in SpecC	42
3.3	Synchronous Parallel Discrete Event Simulation	43
3.4	Synchronization for Multicore Parallel Simulation	44
3.4.1	Protecting Scheduling Resources	44
3.4.2	Protecting Communication	45
3.4.3	Channel Locking Scheme	45
3.4.4	Automatic Code Instrumentation for Communication Protection	47
3.5	Implementation Optimization for Multicore Simulation	49
3.6	Experiments and Results	50
3.6.1	Case Study on a H.264 Video Decoder	50
3.6.2	Case Study on a JPEG Encoder	55
<b>4</b>	<b>Out-of-Order Parallel Discrete Event Simulation</b>	57
4.1	Motivation	57
4.2	Out-of-Order Parallel Discrete Event Simulation	59
4.2.1	Notations	59
4.2.2	Out-of-Order PDES Scheduling Algorithm	62
4.3	Out-of-Order PDES Conflict Analysis	62
4.3.1	Thread Segments and Segment Graph	62
4.3.2	Static Conflict Analysis	67
4.3.3	Dynamic Conflict Detection	70
4.4	Experimental Results	71
4.4.1	An Abstract Model of a DVD Player	71
4.4.2	A JPEG Encoder Model	72
4.4.3	A Detailed H.264 Decoder Model	73
<b>5</b>	<b>Optimized Out-of-Order Parallel Discrete Event Simulation</b>	75
5.1	Optimized Compiler Using Instance Isolation	75
5.1.1	Motivation	75
5.1.2	Instance Isolation Without Code Duplication	79
5.1.3	Definitions for the Optimized Static Conflict Analysis	80
5.1.4	Algorithm for Static Conflict Analysis	81
5.1.5	Experimental Results	83
5.2	Optimized Scheduling Using Predictions	84
5.2.1	State Prediction to Avoid False Conflicts	85
5.2.2	Static Prediction Analysis	85

5.2.3	Out-of-Order PDES Scheduling with Predictions . . . . .	90
5.2.4	Optimized Out-of-Order PDES Scheduling Conflict Checking with a Combined Prediction Table . . . . .	91
5.2.5	Experimental Results. . . . .	91
<b>6</b>	<b>Comparison and Outlook . . . . .</b>	<b>95</b>
6.1	Experimental Setup . . . . .	95
6.1.1	Experimental Environment Setup . . . . .	95
6.1.2	The Parallel Benchmark Models . . . . .	96
6.1.3	The Embedded Applications. . . . .	98
6.2	Parallel Discrete Event Simulation Overlook. . . . .	100
<b>7</b>	<b>Utilizing the Parallel Simulation Infrastructure. . . . .</b>	<b>107</b>
7.1	Introduction . . . . .	107
7.1.1	Creating Parallel System Models . . . . .	108
7.1.2	Shared Variables and Race Conditions . . . . .	109
7.2	Race Condition Detection for ESL Models. . . . .	110
7.3	Dynamic Segment Aware Detection. . . . .	111
7.3.1	Automatic Race Condition Diagnosis . . . . .	112
7.3.2	Race Condition Elimination Infrastructure . . . . .	113
7.3.3	Experiments and Results . . . . .	116
7.3.4	Case Study: A Parallel H.264 Video Decoder. . . . .	116
7.3.5	Case Study: A Parallel H.264 Video Encoder. . . . .	117
7.3.6	Additional Embedded Applications . . . . .	119
7.3.7	Conclusions for Dynamic Segment Aware Detection . . . . .	120
7.4	Static Segment Aware Detection . . . . .	120
7.4.1	Segment Graph Data Structures . . . . .	120
7.4.2	Determining MHP Segments . . . . .	122
7.4.3	MHP Algorithm for Race Condition Analysis. . . . .	125
7.4.4	Experiments and Results . . . . .	127
7.4.5	Conclusions for Static Segment Aware Detection . . . . .	129
<b>8</b>	<b>Conclusions . . . . .</b>	<b>131</b>
8.1	Contributions . . . . .	131
8.1.1	A Model of Computation for System-Level Design. . . . .	132
8.1.2	A Synchronous Parallel Discrete Event Simulator. . . . .	132
8.1.3	An Advanced Parallel Discrete Event Simulation Approach . . . . .	133
8.1.4	An Infrastructure for Increasing Modeling Observability . . . . .	133

8.2	Future Work . . . . .	134
8.2.1	Model Parallelization. . . . .	134
8.2.2	Multithreading Library Support. . . . .	134
8.2.3	Extension to the SystemC SLDL . . . . .	134
8.2.4	Parallel Full System Validation. . . . .	135
8.3	Concluding Remarks . . . . .	135
<b>References . . . . .</b>		<b>137</b>
<b>Index . . . . .</b>		<b>143</b>

Out-of-order Parallel Discrete Event Simulation for  
Electronic System-level Design

Chen, W.

2015, XIX, 145 p. 51 illus., 41 illus. in color., Hardcover

ISBN: 978-3-319-08752-8