Preface

The application of Very Large Scale Integration (VLSI) circuits is ubiquitous while the size of the hardware components is shrinking. VLSI circuits are used for a wide range of different applications in embedded systems such as medical electronics, automotive systems and avionics. A failure of a chip in non-critical applications may cause significant economic loss while in critical applications may also endanger human's lives in the worst case. Consequently, the correct design of VLSI circuits is crucial.

The debugging process is dedicated to localize and to rectify the root cause of the erroneous behavior of VLSI circuits. This process often remains as a manual task and increases the time required for development cycles of Integrated Circuits (ICs) significantly. Therefore, debug automation procedures are required to accelerate finding and fixing bugs and faults and, consequently, to increase the productivity of IC design.

This book contributes to debugging and diagnosis technology at the most challenging gaps on different abstraction levels of a hardware system, i.e., chip, gate-level, Register Transfer Level (RTL) and transaction-level.

In this book, we propose automated debugging approaches for the bugs and the faults which appear in different abstraction levels of a hardware system, i.e., transaction-level, RTL, and gate-level. Our automated debug approaches are applied to a hardware system at different granularities to find the possible location of bugs and faults. The transaction-based debug approach is applied to a hardware system at transaction-level asserting the correct relation of transactions. Our automated debug approach for design bugs finds the potential fault candidates at RTL and gate-level of a circuit. In this case, logic bugs and synchronization bugs are considered as they are the most difficult bugs to be localized. For electrical faults and, in particular, delay faults our proposed debug automation finds the potential failing speedpaths in a circuit at gate-level.

The proposed debug approaches for transactions, design bugs and electrical faults have been evaluated on suitable benchmarks at different levels of abstraction, i.e., transaction-level, RTL and gate-level. The experiments have shown that our debug

approaches achieve high diagnosis accuracy and reduce the debugging time. As a result, the time of the IC development cycle decreases and the productivity of IC design increases.

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