

Chapter 2

Diodes and Transistors

In all basic circuits of the pulse DC/DC or DC/AC voltage converters, the switching elements are transistors (bipolar and unipolar) and diodes. In the analysis of a basic circuit, transistors and diodes have been considered as ideal switches (zero on-resistance, infinite off-resistance, and instantaneous transition from one state to the other). However, they are not ideal switches but have real parameters, in both the static and dynamic modes of operation. The influence of these parameters on the characteristics of pulse converters is considerable, particularly on the efficiency factor. For this reason, in this chapter, a description is given of the basic switching characteristics of transistors (bipolar and unipolar) and diodes. An analysis is presented of the modes of control of transistor switches and the optimum control circuits are given. The analysis is of a general character and applies to all pulse assemblies using diodes or transistors as switches.

2.1 Diode as a Switch

The static characteristic of a p-n junction diode is nonlinear and is determined by

$$I_d = I_s \left(e^{V_d/m_d \phi_t} - 1 \right) \quad (2.1)$$

where I_s is the reverse saturation current, m_d is the correction factor ($m_d = 2$ for small currents—in the vicinity of the knee of the characteristic and $m_d = 1$ at higher currents), ϕ_t is the temperature potential. The static characteristic (Fig. 2.1) consists of three regions: conduction region (low-resistance), cut off (high-resistance), and breakdown. The region where the operating point is found depends on the voltage applied to the diode. Therefore, a diode can be used as a switch because its resistance can be controlled by the applied voltage.

When a diode is forward biased and if $V_d > V_{Dt}$, where V_{Dt} is the conduction threshold voltage, the diode is on (conducting). Then its resistance is small (from 10 to 100 Ω). Since the threshold voltage of Si diodes is $V_{Dt} = (0.5\text{--}0.6)$ V, in the conduction region $V_d \gg m\phi_t$, and $\exp(V_d/m_d\phi_t) \gg 1$, so the current is

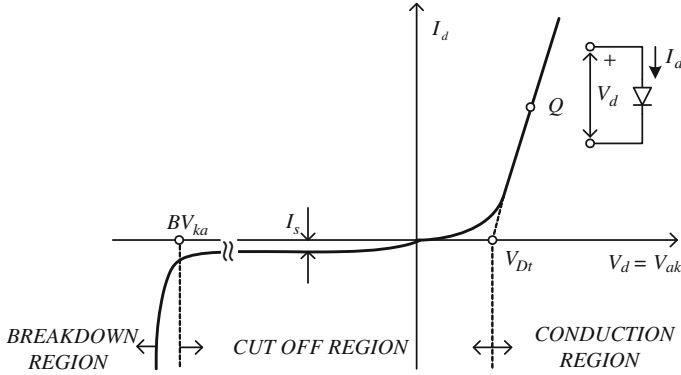


Fig. 2.1 The static diode characteristic

$$I_d \approx I_s e^{V_d / (m_d \phi_t)} \quad (2.2)$$

The dynamic diode resistance is the reciprocal value of the dynamic diode conductance and is defined by

$$r_d = \left. \frac{1}{dI_d/dV_d} \right|_{V_d=\text{const}} = \frac{m_d \phi_t}{I_{DQ}}, \quad (2.3)$$

where I_{DQ} is the diode current at the quiescent operating point Q . Any increase of the diode current I_{DQ} decreases the dynamic resistance. For instance, for $I_{DQ} = 1 \text{ mA}$, $r_d = 26 \Omega$ and for $I_{DQ} = 26 \text{ mA}$, $r_d = 1 \Omega$. It has been assumed that $\phi_t = 26 \text{ mV}$ and $m_d = 1$. It should be emphasized that (2.3) is the p-n junction resistance. The total resistance between the anode and the cathode is increased by the resistance of the base (substrate), which is typically $10\text{--}100 \Omega$, i.e., $R_d = r_d + r_b$. At high currents the resistance r_b is dominant and the V - I characteristic in that region is almost linear.

In many practical applications a conducting diode can be approximated, with a satisfactory accuracy, by a straight line of the slope determined by R_D and a voltage source V_{Dt} (Fig. 2.2a). Then

$$V_d = V_{Dt} + R_D I_D. \quad (2.4)$$

On the other hand, in the majority of diode applications as a switch, the resistance of the driving circuit, which determines the current I_{DQ} in the quiescent operating point Q , is much higher than R_D so that the voltage variation across the diode is negligible. The diode is then replaced by a voltage source V_D and its characteristic is drawn as a straight line that passes through the operating point Q and is orthogonal to the V_D axis (Fig. 2.2b). Typically $V_D = 0.7\text{--}0.8 \text{ V}$ and includes a voltage drop of $0.1\text{--}0.2 \text{ V}$ across R_D .

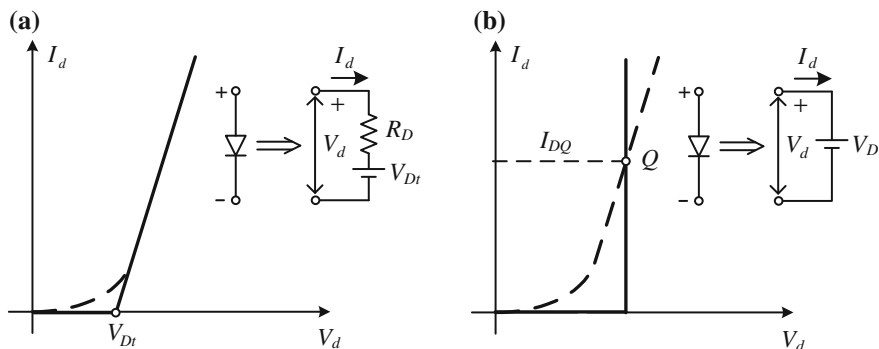


Fig. 2.2 The practical approximations of the V-I characteristic in the conduction region and the corresponding diode equivalent circuits (*dashed line*—real characteristic)

When a diode is reverse biased, i.e., $V_{AK} < 0$, and if $|V_{AK}| > m_d \phi_t$, then $\exp(V_D / m_d \phi_t) \ll 1$ and the current through the diode is equal to the reverse saturation current $I_{DF} = -I_S$. Namely, already at $V_{AK} = -0.2$ V from (2.1) it follows that $I_D = -0.98I_S$. This means that at very small reverse voltages the cathode-anode current is saturated at $-I_S$. The measurements, however, indicate that the reverse current is considerably larger than I_S . This difference is largely due to generation-recombination of charge carriers in the transition region of the p-n junction. At reverse bias, the concentration of charge carriers in the depleted region drops well below the equilibrium concentration. Consequently, recombination is decreased and generation prevails. Owing to the generation of electron-hole pairs a reverse current proportional to the volume of the depleted region Sd and the rate of generation of pairs $G = n_i / (2\tau_0)$ arises, i.e.,

$$I_G = Sq \frac{n_i}{2\tau_0} d, \quad (2.5)$$

where S is the p-n junction area, d is the width of the transition region, n_i is the intrinsic concentration of free charge carriers, τ_0 is the lifetime of carriers in the transition region. It is well known that the width of the transition region increases with increasing the reverse bias, thus causing the increase of the reverse current due to increased generation of the electron-hole pairs:

$$I_G = Sq \frac{n_i}{2\tau_0} d_0 \left(1 - \frac{V_I}{\phi_k}\right)^n, \quad (2.6)$$

where V_I is the reverse voltage, ϕ_k is the contact potential, d_0 is the width of the depletion region at $V_I = 0$, $n = 1/2$ for abrupt and $n = 1/3$ for a p-n junction with a linear distribution of impurities.

The reverse saturation current I_S obtained on the basis of the diffusion theory of the p-n junction is determined by

$$I_s = Sq \left(\frac{D_p p_{n0}}{L_p} + \frac{D_n n_{p0}}{L_n} \right), \quad (2.7)$$

where D_p , L_p , and D_n , L_n are the respective diffusion coefficients and the diffusion lengths for the holes and electrons, respectively, p_{n0} is the concentration of holes in n -type semiconductor, n_{p0} is the concentration of electrons in p -type semiconductor. In the majority of practical applications the p-n junction is highly asymmetric since the concentration of holes p_{p0} in the p -type region is much higher than the concentration of electrons in the n -type region. Therefore, a p^+n^- junction is the most frequent one. Then, $p_{p0} \gg n_{n0}$ and the hole current in (2.7) is much higher (several orders of magnitude) than the electron current. The reverse saturation current is thus

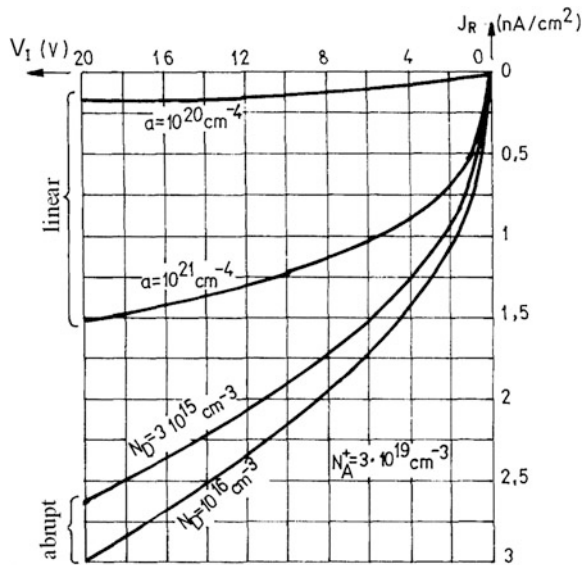
$$I_s \approx I_{sp} = Sq D_p \frac{p_{n0}}{L_p}. \quad (2.8)$$

Applying the relations $p_{p0}n_{n0} = n_i^2$ and $L_p = D_p \tau_0$ one obtains:

$$\frac{I_G}{I_s} = \frac{1}{2} \frac{d}{L_p} \frac{n_{n0}}{n_i}. \quad (2.9)$$

For instance, for a silicon diode with the following parameters: $d = 10^{-4}$ cm, $L_p = 2 \times 10^{-2}$ cm, $n_{n0} = 2.5 \times 10^{15}$ cm $^{-3}$, and $n_i = 1.9 \times 10^{10}$ cm $^{-3}$ the ratio of the reverse generation current I_G to the reverse saturation current I_s is $I_G/I_s \approx 300$. At voltages of approximately 10 volts this ratio may become several thousands. Therefore, the total reverse current of a diode is shown in Fig. 2.3.

Fig. 2.3 Reverse current density versus reverse voltage for linear and abrupt p-n junction



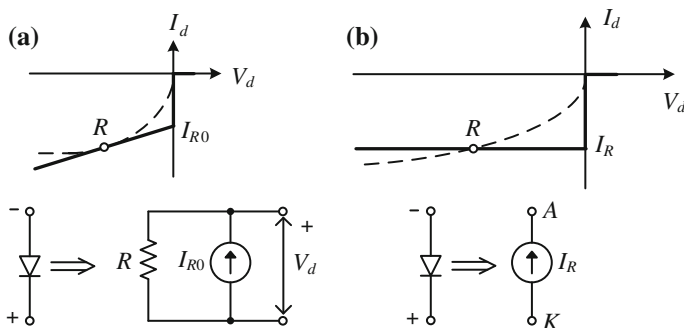


Fig. 2.4 The approximations of V-I characteristic and the corresponding equivalent circuits in the reverse region (*dashed lines*—real characteristics)

$$I_I = I_s + I_G \approx I_G. \quad (2.10)$$

Thus for linear and abrupt junctions the current density characteristic of a diode according to (2.6) is parabolic. In practice, however, the reverse characteristic of a diode is often replaced by a straight line tangential to the operating point R with a segment $-I_{R0}$ on the ordinate (Fig. 2.4a). This means that a diode can be replaced by a parallel connection of a current source I_{R0} and a leakage (reverse) resistance R_I (Fig. 2.4a). Then

$$I_d = -(I_{R0} + V_d/R_I). \quad (2.11)$$

Reverse resistance R_I ranges from several tens $\text{k}\Omega$ (power diodes) to several hundreds $\text{M}\Omega$. The resistance of the driving circuit is usually much lower than R_I , and the change of the reverse current can be neglected. The diode is then replaced by a current source $I_{RR} > I_{R0}$ (Fig. 2.4b) which is specified for a given reverse voltage V_I . The reverse current I_{RR} is usually between 10^{-12} and 10^{-6} A for silicon diodes. Since this current is directly proportional to the surface of the p-n junction, this means that I_{RR} of power diodes is large and can be of the order of mA.

When the reverse voltage is higher than the breakdown voltage of a p-n junction, the diode behaves like a Zener diode if the current is limited. Typical values of the breakdown voltage are between several V up to 100 V. For a high voltage diode this voltage ranges from several 100 V up to several kV.

2.1.1 The Temperature Characteristics

The basic static parameters of a diode as a switch are the reverse current I_R when diode is not conducting and the forward bias voltage V_D when it is conducting. In many applications the temperature sensitivities of these parameters are of

considerable influence on the temperature sensitivities of the functional parameters of the circuits incorporating diodes.

The reverse current is approximated by (2.5). All parameters except n_i are constants independent on temperature, whereas the temperature dependence of n_i^2 is determined by:

$$n_i^2 = AT^3 e^{-V_g/\phi_t}, \quad (2.12)$$

where T is temperature in K, $A = 1.5 \times 10^{32} \text{ cm}^6 \text{ K}^3$, V_g is the bandgap voltage and at room temperature it is 1.11 V. Voltage V_g is also temperature dependent and for silicon it is approximately determined by¹

$$V_g(t) = V_{g0} - 3.6 \times 10^{-4} T, \quad (2.13)$$

where $V_{g0} = 1.21 \text{ V}$ is the bandgap voltage for silicon at absolute zero. The reverse current thus can be written in the form

$$I_R = B T^{3/2} e^{-V_g/(2\phi_t)}, \quad (2.14)$$

where:

$$B = qSA^{1/2} \frac{d}{2\tau_0}. \quad (2.15)$$

After differentiating (2.14) over temperature and rearranging it, the temperature coefficient of the reverse current is obtained as

$$\frac{dI_R}{I_R dT} = \frac{1}{2T} \left(3 + \frac{V_{g0}}{\phi_t} \right). \quad (2.16)$$

At room temperature $T_0 = 300 \text{ K}$, the temperature potential is $\phi = 26 \text{ mV}$, $V_{g0} = 1.21 \text{ V}$ and

$$\left. \frac{dI_R}{I_R dT} \right|_{T_0} = 0.0825 \left[\frac{1}{^\circ\text{C}} \right] \quad (2.17)$$

Very often, however, a more practical expression for $I_R = f(T)$ is used

$$I_R(T) = I_R(T_0) 2^{\frac{T-T_0}{T_x}}, \quad (2.18)$$

where $I_R(T_0)$ is the current I_R at temperature T_0 and T_x is the temperature variation with respect to T_0 , which doubles the value of I_R . T_x can be calculated by equating (2.14) and (2.18) which gives

$$\frac{3}{2} \ln \frac{T}{T_0} + \frac{V_g}{2\varphi_t} \left(\frac{\varphi_t}{\varphi_t(T_0)} - 1 \right) = \frac{T - T_0}{T_x} \ln 2. \quad (2.19)$$

If $(T - T_0)/T_0 \ll 1$ the logarithm of the temperature ratio can be written in the form

$$\ln \frac{T}{T_0} = \ln \left(1 + \frac{T - T_0}{T_x} \right) \approx \frac{T - T_0}{T_x}. \quad (2.20)$$

Since $\varphi_t/\varphi_t(T_0) = T/T_0$, from (2.19) and (2.20) it follows that:

$$T_x = \frac{2 \ln 2}{3 + V_g/\varphi_t} T_0. \quad (2.21)$$

At room temperature ($T = 300$ K) for a silicon diode $T_x = 9$ °C. This would mean that the reverse current doubles for each 9 °C. Here the influence of the reverse saturation current is neglected. It can be shown that its variation with temperature is higher by a factor of 2 (it doubles for each 4.5 °C) since the generation current is proportional to n_i ($I_G \approx I_R \sim n_i$) whereas the injection current is proportional to n_i^2 ($I_S \sim n_i^2$). Due to the influence of the temperature variations of I_S it is accepted in practice that the total reverse current doubles for each 10 °C, i.e.

$$I_R = I_R(T_0) 2^{\frac{T-T_0}{10^\circ\text{C}}}. \quad (2.22)$$

It should be stressed that for small silicon diodes the current $I_R(T_0)$ is quite small and in many applications its temperature variation is of no importance.

The forward bias voltage V_d is also a function of temperature. The case of high currents I_D , when $m_d = 1$, will be considered first. Now the diffusion current compared to the generation-recombination current is dominant and using (2.2), (2.7), and (2.12), taking that $p_{n0} = n_i^2/N_D$ and $n_{p0} = n_i^2/N_A$, one obtains

$$V_d = V_g - \varphi_t \ln \frac{DT^3}{I_D}. \quad (2.23)$$

where D is a temperature independent constant. By differentiating V_d in terms of temperature at a constant current I_D it follows

$$\frac{dV_d}{dT} = \frac{V_d}{T} + \frac{dV_g}{dT} - \frac{\varphi_t}{T} \left(3 + \frac{V_g}{\varphi_t} \right). \quad (2.24)$$

At room temperature for $V_d = 0.7$ V

$$\frac{dV_d}{dT} = \frac{700}{300} - 0.36 - \frac{26}{300} \left(3 + \frac{1110}{26} \right) = -2 \frac{\text{mV}}{^\circ\text{C}}.$$

Therefore, the temperature coefficient of the forward bias voltage is negative. Typically, V_d decreases by 2 mV if the temperature increases by 1 °C. It should be stressed that the expression (2.24) is general because it is also valid for low currents. Then $m_d = 2$ and the generation-recombination current proportional to n_i is dominant instead of I_S , so that

$$V_d = V_g - 2\phi_t \ln \frac{PT^{3/2}}{I_D}, \quad (2.25)$$

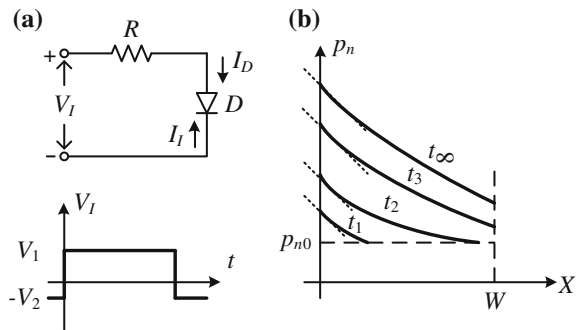
where P is a temperature independent constant. By differentiating (2.25) in terms of T one obtains after rearrangement that at low currents dV_d/dT is determined by (2.24). From (2.24), it is noticeable that the temperature coefficient depends on the position of the operating point. For instance, for $V_D = 0.6$ V, $dV_d/dT = 2.32$ mV/°C and for $V_D = 0.8$ V, $dV_d/dT = 1.66$ mV/°C. In general, it can be said that depending upon the operating regime the temperature coefficient of the forward bias voltage is within the range -1.5 to -2.5 mV/°C.

2.1.2 Dynamic Diode Characteristics

In addition to the static parameters in the switching regime, it is important to know the dynamic response of the diode. The dynamic characteristics of the diode are determined by the transition processes, i.e., the turn-on/turn-off transition times in response to a pulse drive.

Let the diode be driven through a resistance R by a pulse voltage source varying between $-V_2$ and V_1 (Fig. 2.5). The turn-on processes at the instant $t = 0$ will be considered first. For $t < 0$ $V_I = -V_2$ the diode is reverse biased and off. A change of the input voltage at $t = 0$ turns on the diode. If R is much higher than the diode resistance, the current through the diode is

Fig. 2.5 The basic diode switching circuit (a) and distribution of holes in the n -region (b)



$$I_D = \frac{V_1 - V_D}{R} \approx \frac{V_1}{R}, \quad (2.26)$$

because $V_1 \gg V_D$. It is known that the diode current is proportional to the gradient of the injected holes at the edge of the transition region, i.e.,

$$I_D = -qSD_p \frac{dp}{dx} \Big|_{x=0} = \frac{V_1}{R} = \text{const.} \quad (2.27)$$

During the turn-on process, the hole concentration at the edge of the transition region grows from the equilibrium concentration p_{n0} to the concentration determined by the steady state voltage applied across the diode. Since the current through the diode is constant, the change of the hole concentration at the edge of the transition region is also constant (Fig. 2.5b). Practically the steady state is established after a period somewhat longer than the lifetime of the holes, τ_p .

In general, the spatial concentration of holes in the n region during turn-on (Fig. 2.5b) is determined by the diffusion equation:

$$D_p \frac{\partial^2(\Delta p_n)}{\partial x^2} = \frac{\partial(\Delta p_n)}{\partial t} + \frac{\Delta p_n}{\tau_p}, \quad (2.28)$$

where $\Delta p_n = p_n - p_{n0}$ is the excess hole concentration in the n region. The equation governing the excess hole charge can be obtained if Eq. (2.28) is multiplied by $qSdx$ and integrated along the neutral region from $x = 0$ to $x = w$. Therefore:

$$qSD_p \left[\frac{\partial(\Delta p_n)}{\partial x} \Big|_w - \frac{\partial(\Delta p_n)}{\partial x} \Big|_0 \right] = \frac{d}{dt} \int_0^w qS \Delta p_n dx + \frac{1}{\tau_p} \int_0^w qS \Delta p_n dx. \quad (2.29)$$

Since the hole charge is determined by

$$Q_p = \int_0^w qS \Delta p_n dx \quad (2.30)$$

and taking into account (2.27), Eq. (2.29) can be written in the form

$$I_p(0) - I_p(w) = \frac{dQ_p}{dt} + \frac{Q_p}{\tau_p}. \quad (2.31)$$

In the same way, it is possible to derive the equation for the excess electrons in the neutral region. In practice, however, the impurity concentrations of the two sides of the junction are distinctly asymmetric, thus $N_A \gg N_D$, $p_{n0} \gg n_{p0}$ and consequently $Q_p \gg Q_n$. This indicates that the influence of holes on the dynamic process is dominant. Due to this, the index “ p ” in (2.31) can be replaced by “ d ”. Since $I_p(0) - I_p(w) \approx I_p(0) = I_d$ it follows

$$I_d = \frac{dQ_d}{dt} + \frac{Q_d}{\tau_d}. \quad (2.32)$$

This is the charge control equation and it represents the basic relation between the diode current and the excess minority carriers charge in the dynamic operating mode of the diode. In the steady state for a conducting diode $dQ_d/dt = 0$ and $I_d = Q_d/\tau_d$. The injection process is in equilibrium with the recombination process. In other words, a dynamic equilibrium between injection and recombination has been established. The amount of charge in the vicinity of the transition region is constant and proportional to the current through the diode.

At the instant t_0 the input voltage abruptly changes from $+V_1$ to $-V_2$. The diode is reverse biased, but the current through the diode does not drop immediately to the value of the reverse current. On the contrary, for some time the diode conducts with low resistance in the reverse direction (cathode–anode), the current being determined by the external elements. Namely, if $V_d \ll V_2$, the reverse current through the diode is

$$I_1 \approx V_2/R_2 = \text{const.} \quad (2.33)$$

When, at the instant $t = t_0$ the diode is abruptly reverse biased, the direction of the field applied to the p-n junction will change. The direction of the applied field is from the cathode towards the anode and it supports movement of the minority charge carriers. Thanks to this, the excess holes from the n region return to the p region. The direction of the change of the hole concentration at the edge of the junction is altered (Fig. 2.6a). Since the current is constant, the slope of the hole concentration at the edge of the junction is also constant. During this time the piled up charge clears away. A constant reverse current (low diode resistance) will exist as long as the hole concentration at the edge of the junction is greater than zero.

The duration of this phenomenon is called the discharge time, often the accumulation or storage time. It is denoted by t_s . Therefore, during t_s the charge piled up in the vicinity of the p-n junction clears away, i.e., during t_s the diode retains low resistance.

Putting $I_d = I_1$ into Eq. (2.32) and using the initial condition $Q_d(0) = \tau_d I_D$, one obtains that the change of the excess hole charge is

$$Q_d(t) = \tau_d(I_D + I_1)e^{-t/\tau_d} - I_1\tau_d. \quad (2.34)$$

From the condition $Q_d(t_s) = 0$ and (2.34) the storage time is

$$t_s = \tau_d \ln(1 + I_D/I_1). \quad (2.35)$$

Therefore, the storage time is lower if the forward current is lower (Fig. 2.7a), since the stored charge is lower. On the other hand, the storage time is lower if the reverse current is higher (Fig. 2.7b), because the process of clearing away the stored charge is faster.

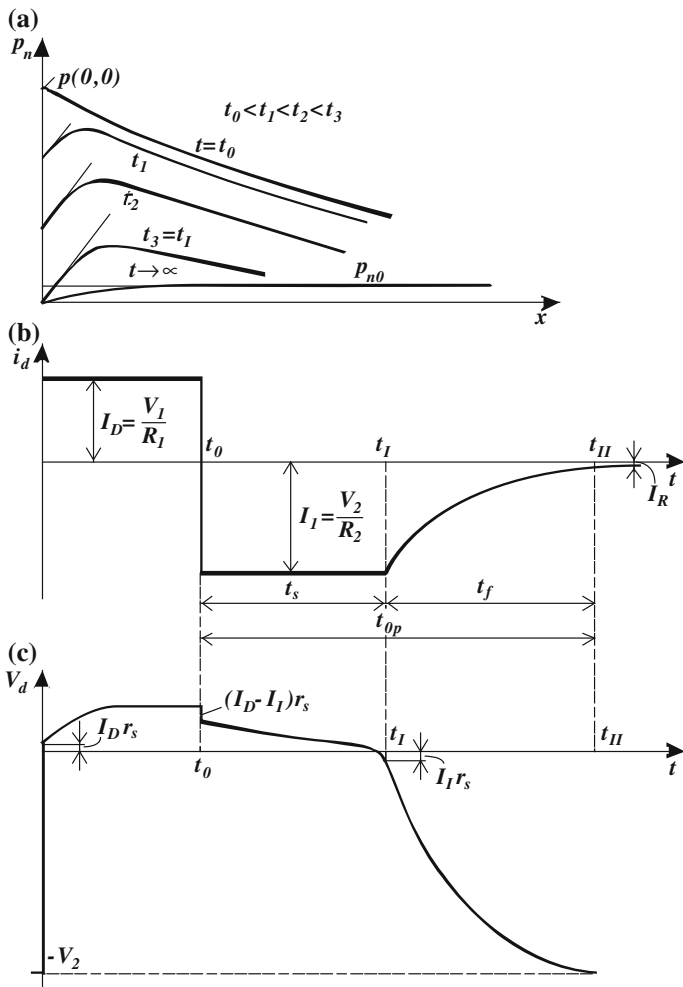


Fig. 2.6 Variation of the hole concentration (a), current (b), and voltage (c) during the turn-off process

Figure 2.6 shows the variations of the current and voltage of a diode in the transient regime. At the instant $t = t_0$ voltage undergoes a negative swing

$$\Delta V = r_s(I_D - I_I). \quad (2.36)$$

Here r_s is the Ohmic resistance of the diode and $I_D - I_I$ is the current swing through the diode at the initial moment. During t_s the voltage across the diode drops to a value $-r_s I_I$. After t_s the diode is obviously reverse biased. The turn-off process continues until the reverse current I_R is attained. The current through the diode reduces and the voltage across it grows more negative. This time is called the fall time and is denoted

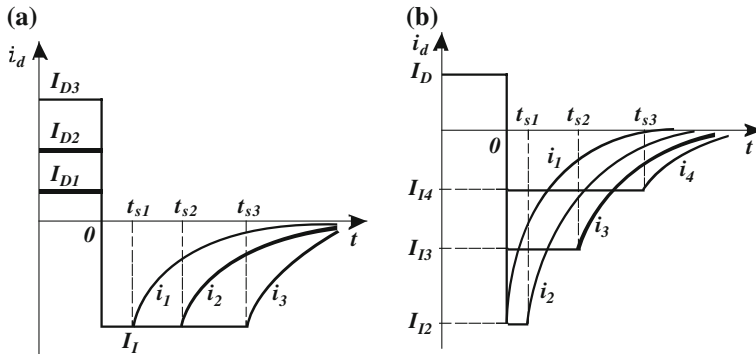


Fig. 2.7 The illustration of the dependence of storage time on forward current for a constant reverse current (a) and on reverse current for a constant forward current (b)

by t_f . Practically, during t_f the capacitor formed by the reverse biased p-n junction is charged. The total turn-off time of the diode $t_s + t_f$ is called the recovery time (denoted by t_r), or sometimes the reverse recovery time (denoted by t_{rr}).

It has been shown that the duration of the transient process is directly proportional to the lifetime of the minority carriers. For this reason in order to reduce τ_p in the n region in fast diodes one introduces the recombination centers, most frequently the atoms of gold. In this way, it is possible to obtain $\tau_p < 1$ ns. Fast diodes, however, have larger reverse saturation currents and lower breakdown voltages. The lifetime of holes in diodes with gold atoms increases with temperature, namely:

$$\tau_p(T) = \tau_p(T_0)(T/T_0)^r, \quad (2.37)$$

where r is a constant; for low injections in silicon it amounts to 3.5 and in germanium 2.2. For instance, for a temperature increase from 213 K (-60°C) to 353 K ($+80^\circ\text{C}$) the average lifetime in silicon increases nearly six times. The duration of the transient process thus largely depends upon temperature.

2.1.3 Schottky Diodes

It is known that the junction of a metal and a weakly doped semiconductor possesses rectifying properties. For instance, at an aluminum— n -type silicon junction, when the donor concentration in silicon is $N_D < 5 \times 10^{18} \text{ cm}^{-3}$, a Schottky barrier is formed and the junction is conductive in one direction and nonconductive in the other. A structure metal— n -type semiconductor with typically $N_D \leq 10^{16} \text{ cm}^{-3}$ makes a Schottky diode.

A Schottky barrier at a metal-semiconductor junction depends upon the type of metal and is within limits 0.58 and 0.85 V. This barrier, similarly to that of a p-n junction, prevents the diffusion of electrons from metal to semiconductor in a

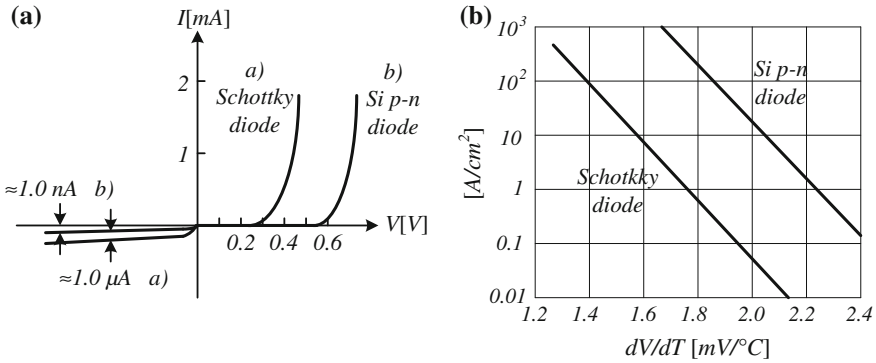


Fig. 2.8 V-I characteristic of Schottky diode (a) and temperature coefficient of forward voltage (b)

nonbiased diode. A positive polarization of the diode (metal is at a higher potential) decreases the potential barrier and electrons from semiconductor cross over to metal. A reverse polarization increases the potential barrier and widens the space charge region which prevents the movement of electrons. The diode is then not conducting. On the semiconductor side the phenomena are identical to those in a p-n junction.

The static V-I characteristic of a Schottky diode is similar to that of a p-n junction diode (Fig. 2.8) and can be written in the form

$$I_d = I_{D0}(e^{V_d/\varphi_t} - 1), \quad (2.38)$$

where the reverse saturation current is

$$I_{D0} = K_{SB} T^2 e^{-\phi_B/\varphi_t}. \quad (2.39)$$

K_{SB} is a constant which is determined experimentally and ϕ_B is the Schottky barrier. The reverse current of a Schottky diode is three to four orders of magnitude higher than the reverse current of a p-n junction diode of the same surface. For a junction with a surface of $S = 100 \mu\text{m}^2$ the reverse current is within the limits $2 \times 10^{-14} \text{ A}$ and 1 nA , depending on the material used.

Except for the difference in the reverse currents the threshold voltages of a Schottky and a p-n junction diodes are quite different. For a Schottky diode this voltage is typically 0.3 V whereas for a Si p-n diode it is approximately 0.6 V . Due to the smaller potential barrier the temperature coefficient of the forward voltage for a Schottky diode is smaller than that of a p-n junction diode (Fig. 2.8b). By neglecting one in the brackets of Eq. (2.38) and having in mind (2.39) it follows

$$\left. \frac{dV_d}{dT} \right|_{\Delta I_d=0} = \frac{V_d}{T} - \frac{\varphi_t}{T} \left(2 + \frac{\phi_B}{\varphi_t} \right). \quad (2.40)$$

For a Schottky diode with aluminum at room temperature $\phi_B = 0.7$ V. If V_D is taken to be 0.4 V, one obtains that $dV_D/dT = -1.2$ mV/°C. The experimentally obtained characteristics for the p-n junction and Schottky diodes (Fig. 2.8b) show that the temperature coefficient of a Schottky diode is smaller by about 0.4 mV/°C.

Schottky diodes are faster. In p-n junction diodes current is carried predominantly by minority carriers. Owing to their accumulation around the junction a delay arises in the turn-off process. In Schottky diodes the electrons are free charge carriers in metal and majority carriers in semiconductor. Current is thus carried by majority carriers and there is no effect of accumulation of minority carriers. Thanks to this Schottky diodes are considerably faster compared to p-n junction diodes. The recovery time of small-signal Schottky diodes is typically less than 0.1 ns.

2.1.4 The Selection of Pulse Diodes

For a good selection of a diode in each specific circuit, it is necessary to know its operation well, the circuit properties and manufacturer's data. These data are usually given in the form of maximum ratings of the static parameters in the forward and the reverse regions and the parameters of the transient state. Usually the following parameters are given at 25 °C:

- the maximum reverse voltage V_I or V_R (this is the maximum negative voltage still not causing the breakdown),
- the maximum reverse current I_R or I_I (this is the current at V_I),
- the maximum forward dc current I_D or I_F ,
- the maximum forward dc voltage V_D at the current I_D ,
- the maximum permitted power P_D (often this information is given instead of I_D or V_D),
- the maximum allowed junction temperature $T_{j\max}$ (this is most often the temperature at which the reverse current is not greater than the given value of I_I . Otherwise, the maximum p-n junction temperature is 90 °C for germanium and 175 °C for silicon diodes),
- the diagram of the permitted forward current versus temperature (Fig. 2.9a) and
- the diagram of the permitted power versus case temperature (Fig. 2.9b).

These data are given for diodes regardless of their purpose. In particular, for pulse diodes, the following additional data are given:

- the maximum forward current I_{DM} , when the current through the diode is pulsed (often the pulse width for a given I_{DM} is specified), and
- the maximum recovery time t_{tr} (usually both the forward and the reverse currents of the transient regime are given for which the specified t_{tr} is guaranteed).

Table 2.1 contains the maximum ratings of the basic parameters for some types of power, low-power, and Schottky diodes.

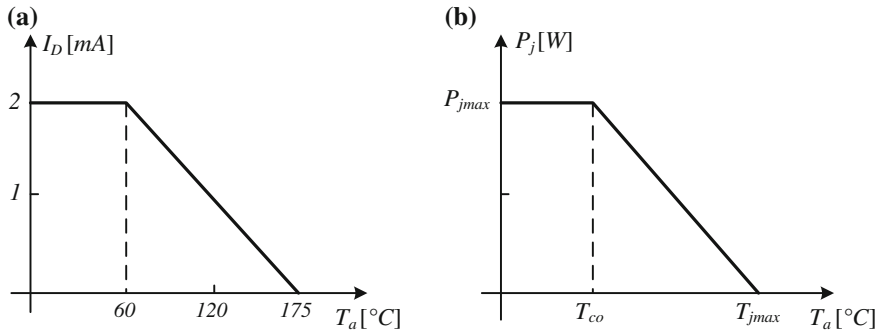


Fig. 2.9 The permitted forward current as a function of the ambient temperature (a) and the permitted junction power as a function of the case temperature (b)

Table 2.1 The basic parameters of different types of diodes

Type	The characteristics at 25 °C						
	I_p [A]	I_{DM} [A]	V_D [V]	I_D [A]	V_I [V]	I_R/V_I [mA]	$t_{rr,max}$ [ns]
Power diodes							
		10 ms	$T_j = 100\text{ °C}$		$T_j = 100\text{ °C}$		$I_D = I_I = 10\text{ mA}$
BYW 77-50	25	500	0.85	20	50	2.5	35
BYW 78-200	50	1500	0.85	50	200	5	60
BYW 08-100	80	1500	0.92	80	100	5	60
BYT 03-400	3	60	1.3	3	400	0.5	2
BYT08P-300A	8	100	1.3	8	300	2.5	2.2
Low power diodes							
		8.3					
1N4149	0.2	0.5	–	–	75	50×10^{-5}	4
1N4151	0.2	0.5	1	0.05	45	50×10^{-5}	2
1N4152	0.2	0.5	0.88	0.02	40	50×10^{-5}	2
1N3070	0.2	0.5	1	0.1	200	100×10^{-5}	5
Schottky diodes							
Bat 17	0.3	–	0.6	10	4	0.25×10^{-3}	<5 ($\tau < 100\text{ ps}$)

The dependence of the forward DC current on the ambient temperature T_a (Fig. 2.9a) shows that for $T_a \leq 60\text{ °C}$ the forward current is constant $I_D = 2\text{ A}$ in the given example. Above this temperature, the permitted forward current drops and for $T_a = T_{jmax}$ it is zero.

The power dissipated in a diode is $P_D = V_D I_D$ and it behaves as a source of heat. Consequently, the diode temperature increases. Thus, the process of self-destruction is possible as the influence of the current temperature coefficient which is positive prevails over the voltage temperature coefficient which is negative. Above the housing temperature T_{c0} the maximum permitted power of the junction decreases (Fig. 2.9b). In the range $T_{c0} < T < T_{j\max}$

$$\frac{T_{j\max} - T_{c0}}{P_{j\max}} = \frac{T_{j\max} - T_c}{P_j}, \quad (2.41)$$

where T_c is the housing temperature, P_j is the permitted, and $P_{j\max}$ is the maximum permitted junction power. From (2.41) it follows:

$$P_j = \frac{T_{j\max} - T_c}{R_{jc}}, \quad (2.42)$$

where

$$R_{jc} = \frac{T_{j\max} - T_{c0}}{P_{j\max}}. \quad (2.43)$$

is the thermal resistance between the junction and the housing. A part of the heat is exchanged between the housing and the ambient. In relation to this, the thermal resistance housing-ambient is defined as the difference between the junction-housing resistance and the total resistance, i.e.,

$$R_{ca} = \frac{T_{j\max} - T_a}{P_j} - R_{jc}. \quad (2.44)$$

The removal of heat is facilitated by mounting the diode on a heat sink. The junction temperature is then

$$T_j = P_j(R_{jc} + R_{ch} + R_{ha}) + T_a, \quad (2.45)$$

where R_{ch} and R_{ha} are the respective resistances housing-heat sink and heat sink-ambient.

2.2 Bipolar Transistor as a Switch

The applications of diodes as switches are quite limited owing to the fact that a diode is a two-terminal device so the control and the controlled circuits are the same. A transistor is a three-terminal device and the control circuit is separated from the load. In accordance with this, it is a standard switching element. In principle, transistors can be connected to a switching circuit in three different configurations:

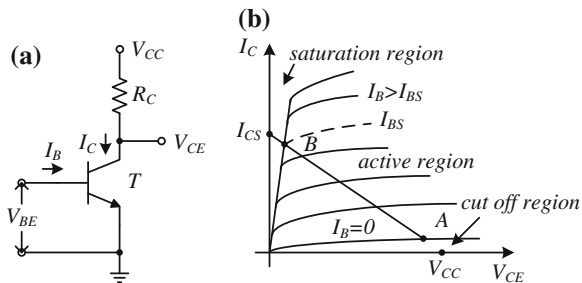


Fig. 2.10 The basic switching circuit (a) and operating regions of transistors (b)

common-emitter, common-base, or common-collector. As a rule, however, transistors are used as switches in the common-emitter configuration. Namely, in this case it is the highest ratio of the load current (collector current) to the input control current (base current), which maintains the on state of the transistor. In other words, this configuration requires the least power for performing control which is the basic requirement for any switch.

In addition to the transistor being used as the switch, the basic switching circuit comprises a load and a power supply (Fig. 2.10a). Depending upon the position of the operating point the transistor will be in one of the three possible regions: saturation, cut off, or active region (Fig. 2.10b). As a switch the transistor is either in saturation or is cut off. The saturation corresponds to the on-state and cut off to the off-state of the switch. These are the static states of the switch. For the analysis of the parameters of the switch use will be made of the Ebers-Moll equations given in the following form

$$I_C = \alpha_N I_E - I_{C0} \left(e^{V_{BC}/(m_c \varphi_t)} - 1 \right), \quad (2.46)$$

$$I_E = \alpha_I I_C + I_{E0} \left(e^{V_{BE}/(m_e \varphi_t)} - 1 \right), \quad (2.47)$$

where α_N and α_I are the respective current gain coefficients of the transistor in the common-base connection for the direct (normal) and reverse modes, I_{C0} is the collector current with the emitter circuit open, I_{E0} is the emitter current with the collector circuit open, m_c and m_e are the respective correction coefficients of the collector and emitter p-n junctions. Like in the case of the diode m_c and m_e are 2 at low currents and 1 at medium currents.

2.2.1 The Cut Off Region

In the cut off region the transistor as a switch is in the off state. It would be ideal if the collector current in this state, i.e., the load current, were equal to zero. In reality,

however, this current does exist. Its value depends on the method the transistors have been switched off. Each of these methods will be analyzed.

1. Both p-n junctions are reverse biased, i.e. $V_{BC} < 0$ and $V_{BE} < 0$

Let $|V_{BC}| \gg m_c \varphi_t$ and $|V_{BE}| \gg m_e \varphi_t$ (these conditions are already fulfilled if V_{BC} and V_{BE} are several 100 mV since $\varphi_t = 26$ mV and $\max\{m_e, m_c\} = 2$). Then:

$$e^{V_{BC}/m_c \varphi_t} \ll 1 \quad \text{and} \quad e^{V_{BE}m_e \varphi_t} \ll 1,$$

and from (2.46) and (2.47) it follows:

$$I_C = \alpha_N I_E + I_{C0} \quad (2.48)$$

$$I_E = \alpha_I I_C - I_{E0}. \quad (2.49)$$

From (2.48) and (2.49), having in mind that

$$\alpha_I I_{C0} = \alpha_N I_{E0} \quad (2.50)$$

one obtains that the collector and the emitter currents, when both junctions are reverse biased, are determined by:

$$I_C = \frac{1 - \alpha_I}{1 - \alpha_I \alpha_N} I_{C0}, \quad (2.51)$$

$$I_E = -\frac{\alpha_I(1 - \alpha_N)}{\alpha_N(1 - \alpha_N \alpha_I)} I_{C0}. \quad (2.52)$$

Typical values of the current coefficients are $\alpha_N = 0.96 - 0.995$ and $\alpha_I = 0.3 - 0.7$. At small currents, these values are several time smaller. Thus, $\alpha_N \alpha_I \ll 1$ and

$$I_c \approx (1 - \alpha_I) I_{C0} < I_{C0}, \quad (2.53)$$

$$I_E \approx -\frac{\alpha_I}{\beta_N} I_{C0}, \quad (2.54)$$

where

$$\beta_N = \frac{\alpha_N}{1 - \alpha_N} \quad (2.55)$$

is the common emitter current gain. The transistor can be replaced by the simplified equivalent circuit (Fig. 2.11a). The negative base current is given by

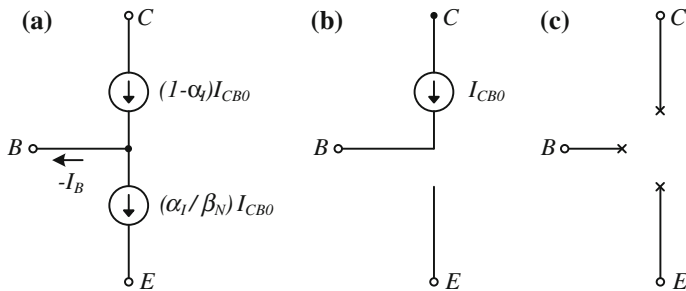


Fig. 2.11 The simplified equivalent circuits of transistor in the cut off region when both junctions are reverse biased

$$I_B \approx -(1 - \alpha_I + \alpha_I / \beta_N) I_{CB0}. \quad (2.56)$$

At small currents, β_N ranges from 1 to 5 and $\alpha_I \ll 1$ so that $I_C \approx I_{CB0}$, $I_E \approx 0$, and $I_B = -I_{CB0}$. The transistor equivalent circuit is shown in Fig. 2.11b. This is, therefore, equivalent to the open emitter. Since $I_C = -I_B$, it is customary that the collector-base current is denoted by I_{CB0} (open emitter collector-base current) and is often called—the reverse base current. It is straightforward to show that $V_{BE} < 0$ when the emitter is open. Namely, by introducing $I_E = 0$ and $I_C = I_{CB0}$ in (2.47) one obtains:

$$V_{BEO} = m_e \varphi_t \ln(1 - \alpha_N) = -m_e \varphi_t \ln(1 + \beta_N). \quad (2.57)$$

For $m_e = 2$ and $\beta_N = 3$, $V_{BEO} = -72$ mV. The current I_{CB0} is temperature dependent and, like the reverse diode current, it doubles with every 10 °C of temperature increase, i.e.

$$I_{CB0}(T) = I_{CB0}(T_0) 2^{\frac{T - T_0}{10^\circ \text{C}}}. \quad (2.58)$$

Usually I_{CB0} at room temperature is of the order of nA and for power transistors of the order of μA . In most practical applications, I_{CB0} can be neglected and the transistor can be considered an open circuit (Fig. 2.11c).

2. The second method of achieving cut off is obtained when: $V_{BE} = 0$ and $V_{BC} < 0$

i.e., when the base and emitter are short circuited and the collector junction is reverse biased. For $|V_{BC}| \gg m_c \varphi_t$ from (2.46) and (2.47) it follows:

$$I_C = \frac{I_{C0}}{1 - \alpha_N \alpha_I}, \quad (2.59)$$

$$I_E = \alpha_I I_C = \frac{\alpha_I}{1 - \alpha_N \alpha_I} I_{C0}. \quad (2.60)$$

Since $\alpha_N \alpha_I \ll 1$, then: $I_C \approx I_{C0}$, $I_E \approx \alpha_I I_{C0}$. The base current is $I_B = I_E - I_C = -(1 - \alpha_I) I_{C0}$. Since $\alpha_I \ll 1$, $I_B \approx -I_{C0}$. Therefore, when the base and emitter are short circuited ($V_{BE} = 0$) the currents are approximately as if $V_{BE} < 0$ or the emitter was open, i.e.

$$I_C \approx -I_B = I_{CBO}, I_E \approx 0. \quad (2.61)$$

3. Transistor will be cut off when: $I_B = 0$, $V_{BC} < 0$

i.e., if the base is open and the collector junction is reverse biased. By replacing $I_C = I_E = I_{CEO}$ in (2.46) and since $|V_{BC}| \gg m_e \phi_t$ it follows:

$$I_{CEO} = \frac{I_{C0}}{1 - \alpha_N} = (\beta_N + 1) I_{C0}. \quad (2.62)$$

In this case, the transistor can be replaced by the equivalent circuit of Fig. 2.12. Therefore, if the base is open, the collector current is $\beta_N + 1$ times greater than I_{CBO} . It should be emphasized that β_N at small currents is typically from 1 to 5, and $I_{CEO} = (2-6) I_{CBO}$. The open base voltage $V_{BE} = V_{OBE}$ can be obtained from (2.47) by the replacement $I_E = I_C = I_{CEO}$:

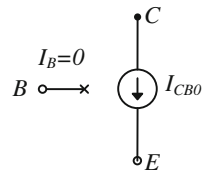
$$V_{OBE} = m_e \phi_t \ln(1 + \beta_N / \beta_I) > 0. \quad (2.63)$$

For instance, for $\beta_N = 3$, $\beta_I = 0.25$ and $m_e = 2$, $V_{OBE} = 133$ mV.

The characteristics of the currents I_C , I_E , I_B versus voltage V_{BE} , for $V_{BC} < 0$ (Fig. 2.13) show that the transistor is cut off when $V_{BE} < V_{OBE}$. In practice it may be assumed that a transistor is cut off if $V_{BE} < V_{BEt}$, where V_{BEt} is the voltage V_{BE} at the knee of the characteristic $I_B = f(V_{BE})$. V_{BEt} is the conduction threshold voltage and for silicon transistors it is typically 0.5–0.6 V.

Very often it is not convenient to realize the cut off state by $V_{BE} < 0$ or $V_{BE} = 0$. The third case ($I_B = 0$) should be avoided since the current I_{CBO} is relatively large and, as will be shown, the voltage limitations of transistors are then the most significant. For this reason the cut off state is often realized by a resistor R between the base and the emitter (Fig. 2.14a). The resistor R is chosen so that $V_{BE} < V_{OBE}$. Then the base current is negative and it is certain that $V_{BE} > 0$. The smaller V_{BE} the

Fig. 2.12 The open base equivalent circuit



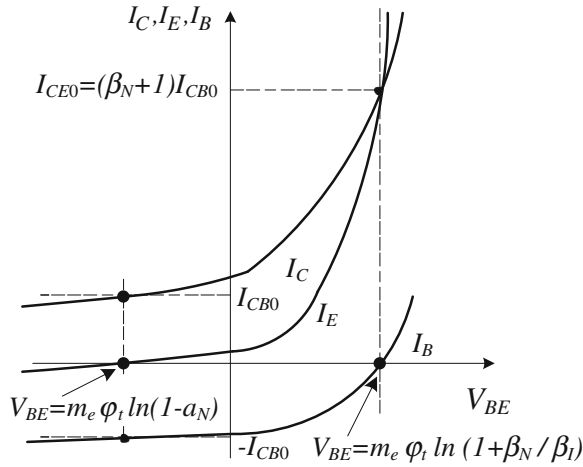


Fig. 2.13 Transistor currents in the cut off region

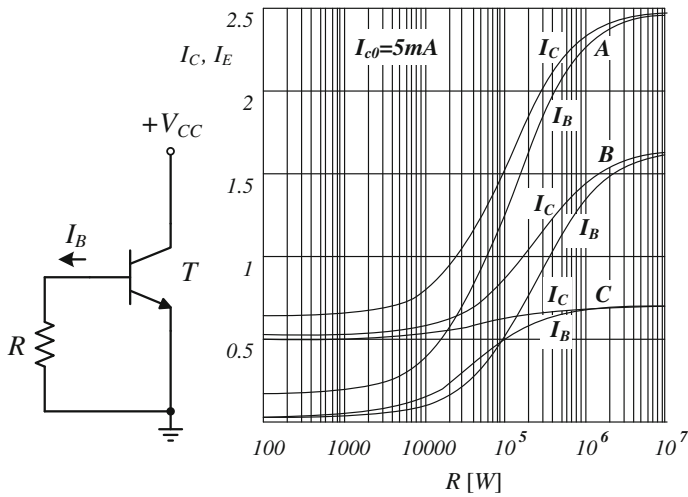


Fig. 2.14 The realization of the cut off state by a resistor (a) and the dependencies of the emitter and collector currents on resistor R for $I_{C0} = 5 \mu\text{A}$, (b) with $\alpha_N = 0.8$, $\alpha_I = 0.3$ (A) $\alpha_N = 0.7$, $\alpha_I = 0.1$ (B), and $\alpha_N = 0.3$, $\alpha_I = 0.1$ (C)

smaller collector current. Therefore it is assumed that V_{BE} is approximately zero, i. e. $V_{BE} \ll m_e \phi_t$. Since $|V_{BC}| \gg m_e \phi_t$ the emitter current is:

$$I_E = \alpha_I I_C + I_{EO} \left(e^{V_{BE}/(m_e \phi_t)} - 1 \right) \approx \alpha_I I_C + \frac{I_{EO} V_{BE}}{m_e \phi_t}, \quad (2.64)$$

and the collector current is determined by (2.48). Since

$$V_{BE} = R(I_C - I_E), \quad (2.65)$$

by using (2.64) and (2.48) one obtains:

$$I_C = \frac{\alpha_N m_e \varphi_t + \alpha_I I_{C0} R}{\alpha_N (1 - \alpha_N \alpha_I) m_e \varphi_t + \alpha_I (1 - \alpha_N) I_{C0} R} I_{C0}, \quad (2.66)$$

$$I_E = \alpha_I \frac{\alpha_N m_e \varphi_t + R I_{C0}}{\alpha_N (1 - \alpha_N \alpha_I) m_e \varphi_t + \alpha_I (1 - \alpha_N) I_{C0} R} I_{C0}. \quad (2.67)$$

It is straightforward to show that $V_{BE} = 0$ and $I_B = 0$ are both special cases of the cut off state caused by a resistor between the base and emitter. Namely, from (2.66) and (2.67) it follows that $R = 0$ results in (2.59) and (2.60) and $R \rightarrow \infty$ results in (2.62). On the basis of the variations of collector and emitter currents as functions of R (the R axis is shown in the logarithmic scale) (Fig. 2.14b) it follows that for the resistor R values below several $k\Omega$ the currents I_C and I_E are approximately as if the base and emitter were short circuited. Thus, the practical values of R are within limits from several hundred Ω to several $k\Omega$.

2.2.1.1 The Voltage Limitations

When a transistor is off, the collector junction is always reverse biased and sometimes the emitter junction is reverse biased too. Care must be taken that the reverse voltage is lower than the breakdown voltage. The impurity concentrations in the emitter barrier of diffused transistors are quite high and the emitter-base breakdown voltages are small, typically between 5 and 7 V, rarely 9 V. The reverse voltages of the emitter junction are usually smaller than the breakdown voltage. The reverse voltage of the collector junction is higher. The impurity concentration in the collector barrier is smaller and the breakdown voltage is higher and depends on the connection of the transistor. At high reverse voltages, the process of avalanche multiplication of carriers in the collector barrier appears leading to an abrupt increase of the collector current. In fact, due to the multiplication the parameters α_N and I_{CBO} exhibit sharp increase so the collector current in the common-base connection is expressed by

$$I_C = M \alpha_N I_E + M I_{CBO}, \quad (2.68)$$

where

$$M = \frac{1}{1 - (V_{CB}/BV_{CBO})^n} \quad (2.69)$$

is the multiplication factor. BV_{CBO} is the base-collector breakdown voltage at the open emitter ($I_E = 0$), and n is the parameter depending upon the impurity concentration of the less-doped region. For abrupt and linear p-n junctions n ranges from 2 to 6. If the emitter is open ($I_E = 0$), $I_C = MI_{CBO}$. In the breakdown region $M \rightarrow \infty$ and $I_C \rightarrow \infty$ which is obtained for $V_{CB} = BV_{CBO}$.

When a transistor is in the common-emitter connection, the breakdown phenomena are more complex and the collector current in the breakdown region is:

$$I_C = \frac{M\alpha_N}{1 - M\alpha_N} I_B + \frac{MI_{CBO}}{1 - M\alpha_N}. \quad (2.70)$$

For $I_B = 0$ the breakdown occurs at $M\alpha_N = 1$ resulting in:

$$BV_{CEO} = \frac{BV_{CBO}}{\sqrt[n]{\beta + 1}}. \quad (2.71)$$

Thus, for instance, if $BV_{CBO} = 60$ V, $n = 4$, and $\beta_N = 50$, then $BV_{CEO} = 22.6$ V. Therefore, the breakdown voltage of an open base transistor is several times lower compared to the open emitter situation (Fig. 2.15).

Most often the transistor is cut off by a resistor between the base and emitter (Fig. 2.14a). The base-emitter voltage is then negligibly small and the breakdown voltage of the transistor is equal to the collector-emitter voltage. It is usually denoted by BV_{CER} . By introducing in (2.66) the substitutions $\alpha_N = M\alpha_N$ and $I_{C0} = MI_{C0}$ and from the condition that $I_C \rightarrow \infty$ it follows (Fig. 2.16).

$$BV_{CER} = BV_{CBO} \sqrt[n]{1 - \frac{m\phi_t \alpha_N + RI_{C0}}{m\phi_t \alpha_N + \alpha_t RI_{C0}} \alpha_N \alpha_t}. \quad (2.72)$$

In the limiting cases when $R \rightarrow \infty$ (2.73) transforms into (2.71) and when $R = 0$, $BV_{CER} = BV_{CEK}$ (K -base and emitter short circuited), where

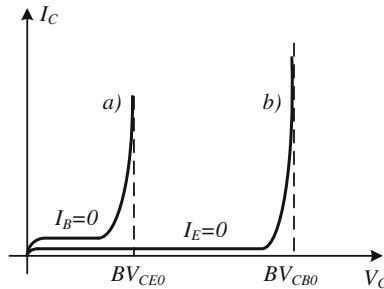
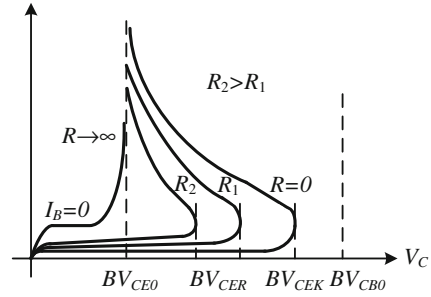


Fig. 2.15 The illustration of the breakdown characteristic of a transistor in common-emitter (a) and common-base (b) connection

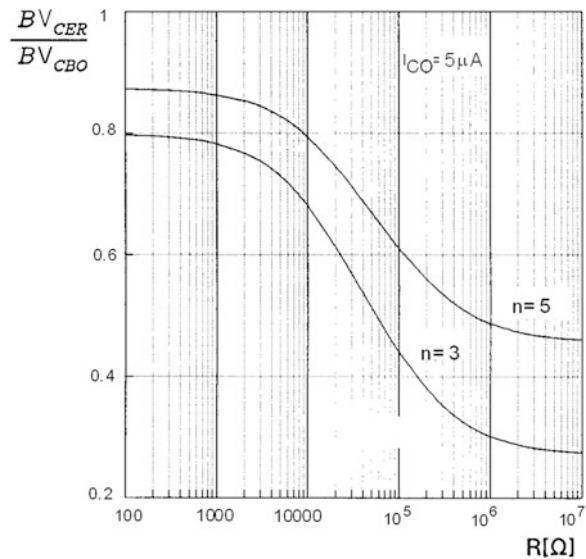
Fig. 2.16 Illustration of the dependence of the breakdown voltage from the resistance R



$$BV_{CEK} = BV_{CBO} \sqrt[n]{1 - \alpha_N \alpha_I}.$$

This expression can also be obtained directly from (2.59). Figure 2.17 shows the normalized voltage BV_{CER} as a function of R , according to (22.72). At small values of R the breakdown voltage is approximately the same as if the base and emitter were short circuited, i.e. $BV_{CER} \approx BV_{CEK}$. Consequently, it may be concluded that the currents and breakdown voltage of a transistor, when the resistor R is within limits from several 100Ω to several $k\Omega$, are nearly the same as if the base and emitter were short circuited (Figs. 2.14 and 2.17). The breakdown voltage is then only 10–20 % lower than the maximum breakdown voltage BV_{CBO} and the collector current is somewhat higher (up to 10 %) than I_{CB0} .

Fig. 2.17 Normalized breakdown voltage as function of R for $I_{C0} = 5\mu A$, $\alpha_N = 0.98$, $\alpha_I = 0.5$, $m = 1.5$ and for $n = 3$ and $n = 5$



Example 2.1 For the switch of Fig. 2.10 determine breakdown voltage in the following cases

- (a) $R \rightarrow \infty$,
- (b) The resistance between the base and the emitter is $R = 20 \text{ k}\Omega$, and $R = 100 \text{ }\Omega$.
The circuit of Fig. 2.10 has: $BV_{CBO} = 80 \text{ V}$, $\alpha_N = 0.983$, $\alpha_I = 0.1$, $I_{C0} = 50 \text{ nA}$, $\phi_t = 25 \text{ mV}$ and $n = 4$.

If $R \rightarrow \infty$ base is broken, the collector current is equal to emitter current (I_{CE0}) and using the Ebers-Moll model, the emitter (collector) current is (2.59)

$$I_{CE0} = \frac{I_{C0}}{1 - \alpha_N}.$$

In the breakdown region the parameters α_N and I_{C0} are multiplied by a multiplication factor $M = \frac{1}{1 - \left(\frac{BV_{CB}}{BV_{CBO}}\right)^n}$, where BV_{CB} is the breakdown voltage of the p-n junction collector-emitter in a general case, and BV_{CBO} is the breakdown voltage of the collector-base p-n junction with the broken emitter. From the breakdown condition $1 - \alpha_N \rightarrow 0$ one obtains (2.71)

$$BV_{CEO} = \frac{BV_{CBO}}{\sqrt[n]{\beta_N + 1}} = 28.67 \text{ V}.$$

- (a) If there is a resistor R between the base and the emitter of the transistor, using the Ebers-Moll model of transistor and multiplying in breakdown voltage region coefficients α_N and I_{C0} by the factor of multiplication, the breakdown voltage of p-n junction collector-base (BV_{CER}) is equal to (2.72):

$$BV_{CER} = BV_{CBO} \sqrt[n]{1 - \frac{m\phi_t\alpha_N + RI_{C0}}{m\phi_t\alpha_N + \alpha_I RI_{C0}} \alpha_N \alpha_I}, \text{ where } m_c = m_e = m.$$

- (b) For $R = 20 \text{ k}\Omega$ is obtained $BV_{CER} = 75.92 \text{ V}$, and for $R = 100 \text{ }\Omega$ is obtained $BV_{CER} = 75.96 \text{ V}$.

2.2.2 The Saturation Region

When $V_{BE} > V_{BEt}$, the transistor is on and it may be either in the active or in the saturation region. In the active region the collector current is $I_C = \beta I_B + I_{CEO} \approx \beta I_B$ and:

$$V_{CE} = V_{CC} - \beta R_C I_B. \quad (2.73)$$

(The omission of the index 'N' implies that the normal current gains β and α are considered). Increasing the driving current I_B reduces the V_{CE} voltage down to the limiting value $V_{CE} = V_{CES}$ for $I_B = I_{BS}$ when the operating point is in the position *B* (Fig. 2.10b). If I_B further increases above the value I_{BS} , the collector–emitter voltage and the collector current do not change and are determined by:

$$V_{CE} = V_{CES}, \quad I_{CS} = \frac{V_{CC} - V_{CES}}{R_C} \quad (2.74)$$

It is said then that the transistor is in saturation, since the response (the collector current I_{CS} or the voltage V_{CES} , in saturation) does not change with the excitation (base current). This is because both of the p-n junctions are forward biased and the transistor loses its amplifying ability that it had in the active region owing to the reverse bias of the base–collector junction. A forward bias of the collector junction, i.e.,

$$V_{BC} > V_{BCt} \quad (2.75)$$

is, thus, the condition for the transistor saturation, where V_{BCt} is the conduction threshold of the collector junction. Since $V_{BC} = V_{BE} - V_{CE}$, from (2.73) and (2.75) one obtains that the transistor is in saturation if:

$$I_B \geq \frac{V_{CC} - (V_{BE} - V_{BCt})}{\beta R_C} \quad (2.76)$$

The collector–emitter voltage in saturation is:

$$V_{CES} = V_{BE} - V_{BC}. \quad (2.77)$$

By substitution of (2.77) in (2.76) the saturation condition can be expressed in the following form

$$I_B \geq I_{BS}, \quad (2.78)$$

where

$$I_{BS} = \frac{V_{CC} - V_{CES}}{\beta R_C} = \frac{I_{CS}}{\beta} \quad (2.79)$$

is the base current at the boundary between the active and the saturation region. Because maintaining a transistor in saturation requires a driving current not smaller than I_{BS} , the transistor is usually called a current controlled switch. As a measure of saturation, the factor or degree of transistor saturation is often defined

$$F_s = I_B/I_{BS} = \beta I_B/I_{CS},$$

where I_B is the base current keeping the transistor in saturation. To determine the saturation condition one may use (2.75) or (2.78). It should be emphasized that the condition (2.75) is more general because (2.78) is valid only if the load is not a complex impedance. From (2.77), (2.46), and (2.47) it follows

$$V_{CES} = \varphi_I \ln \frac{\alpha_N [I_B + I_{CS}(1 - \alpha_I)]}{\alpha_I [\alpha_N I_B - I_{CS}(1 - \alpha_N)]}. \quad (2.80)$$

It has been assumed that $m_c = m_e = 1$. For $I_{CS} = 0$ voltage V_{CES} is minimal and determined by

$$V_{CESmin} = V_{CES0} = \varphi_I \ln \frac{1}{\alpha_I}. \quad (2.81)$$

This means that compared to the origin the I_C - V_{CE} characteristics are shifted to the right by the value V_{CES0} (Fig. 2.18). For diffused transistors $0.3 \leq \alpha_I \leq 0.7$, and $9.3 \text{ mV} < V_{CES} < 31.3 \text{ mV}$. These limits should be increased by a factor of 1.2–1.5 because at small currents the correction factor is $m_c > 1$.

The temperature coefficient of the voltage V_{CES} is equal to the difference of the corresponding coefficients of the emitter and the collector diodes, i.e.:

$$\frac{d V_{CES}}{dT} = \frac{d V_{BE}}{dT} - \frac{d V_{BC}}{dT}. \quad (2.82)$$

In view of (2.24)

$$d V_{CES}/dT = V_{BE}/T - V_{BC}/T = V_{CES}/T. \quad (2.83)$$

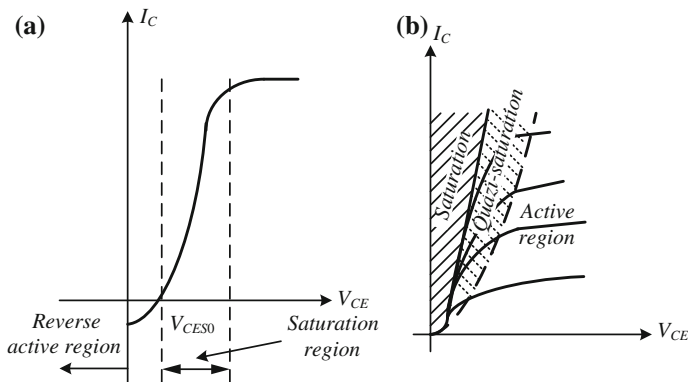


Fig. 2.18 The output characteristics in saturation of a transistor having a small (a) and large (b) collector body resistance

Therefore, the temperature coefficient of the voltage V_{CES} is positive and at room temperature ($T = 300^\circ\text{K}$) it is $dV_{CES}/dT = (0.33 - 0.66) \text{ mV}/^\circ\text{C}$.

The collector–emitter resistance of a transistor in saturation is determined by:

$$r_{ces} = \left. \frac{dV_{CES}}{dI_{CS}} \right|_{I_B=\text{const}} = \frac{\phi_I}{I_B} \left[\frac{1}{1 + \beta_I + I_{CS}/I_B} + \frac{1}{\beta - I_{CS}/I_B} \right] \quad (2.84)$$

For $\beta_I = 1$, $\beta = 50$, and $I_B = 1 \text{ mA}$ at $I_{CS} = 10 \text{ mA}$, $r_{ces} \approx 2.8 \Omega$ and at $I_{CS} = 40 \text{ mA}$, $r_{ces} \approx 3.2 \Omega$. This resistance should be increased by summing with the resistance of the collector body r_c . The total collector resistance in saturation $r_{cs} = r_{ces} + r_c$ is typically $5\text{--}10 \Omega$ (for low power transistors).

Over the major part of the saturation region the resistance r_{cs} is nearly constant. By approaching the active region (weak saturation), however, the second member in the brackets in (2.84) sharply rises with I_{CS} . At the boundary of the saturation region and the active region $I_{CS}/I_B = \beta$ and $r_{ces} \rightarrow \infty$ which, if the characteristic is ideal, corresponds to resistance r_{ce} of a transistor in the active region. The increase of r_{ces} in weak saturation, particularly for power transistors, is also a consequence of their technological structure. This region is often called the region of quasi-saturation (Fig. 2.18b). Namely, for high voltage power transistors the resistance of the epitaxial layer can be significant. When a transistor is strongly saturated, the collector p-n junction is strongly forward biased and the concentration of charge carriers is very high. The resistance of the epitaxial layer is low and does not influence the characteristics in saturation. In the region of quasi-saturation the collector p-n junction is weakly forward biased and the concentration of charge carriers is reduced which leads to an increase of the resistance. This is particularly characteristic for transistors having a wide epitaxial layer (power and high voltage transistors). In transistors having a narrow epitaxial layer, or having no epitaxial layer, the quasi-saturation region practically does not exist.

A transistor in saturation can be replaced by the collector and emitter diodes (Fig. 2.19a) because both of the p-n junctions are forward biased. The equivalent circuit is shown in Fig. 2.19b. The resistance r_{bs} ranges from several tens Ω up to several hundreds Ω and r_{cs} from several up to 10Ω . Most of the time these

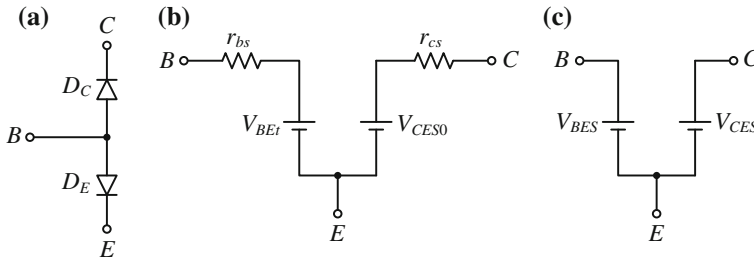


Fig. 2.19 The equivalent circuits of a transistor in saturation

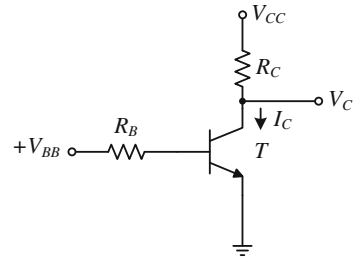
resistances can be neglected and thus the simplified equivalent circuit of a transistor in saturation can be used, as shown in Fig. 2.19c. Typical voltage values are: $V_{\text{BES}} = (0.7\text{--}0.8)$ V and $V_{\text{CES}} = (0.1\text{--}0.2)$ V.

Example 2.2

- For a switch shown in Fig. 2.20 calculate the collector–emitter voltage when the transistor is in saturation for $R_C \rightarrow \infty$ and $R_C = R_B$.
- Determine the collector–emitter resistance for the transistor in saturation region (r_{CES})

The circuit of Fig. 2.20 has: $R_B = 4.7$ k Ω , $\alpha_N = 0.952$, $\alpha_I = 0.3$, $\phi_t = 25$ mV, $V_{\text{BES}} = 0.75$ V and $V_{\text{CC}} = V_{\text{BB}} = 15$ V.

Fig. 2.20 Simple circuit with the bipolar transistor as a switch



- Based on the Ebers-Moll model, the voltage between the collector and the emitter of a bipolar transistor in the state of saturation (V_{CES}) (2.80) the following expression can be derived:

$$V_{\text{CES}} = \phi_t \ln \frac{\alpha_N [I_B + I_{\text{CS}}(1 - \alpha_I)]}{\alpha_I [\alpha_N I_B - I_{\text{CS}}(1 - \alpha_N)]} = \phi_t \ln \frac{\alpha_N \left[1 + \frac{\beta_N}{F_S}(1 - \alpha_I) \right]}{\alpha_I \left[\alpha_N - \frac{\beta_N}{F_S}(1 - \alpha_N) \right]}, \quad (2.85)$$

where

$$F_S = \frac{I_B}{I_{\text{BS}}} = \frac{\beta R_C}{R_B} \frac{V_{\text{BB}} - V_{\text{BES}}}{V_{\text{CC}} - V_{\text{CES}}}.$$

For $R_C \rightarrow \infty$, the current $I_{\text{CS}} \rightarrow 0$, and on the basis of (2.85) the voltage between the collector and the emitter in the state of saturation is

$$V_{\text{CES}} = \phi_t \ln \frac{1}{\alpha_I} = 31 \text{ mV}.$$

For $R_C = R_B$ the factor of transistor saturation $F_S \approx \beta = 20$. Based on expression (2.80), the collector–emitter voltage for a bipolar transistor in the saturation region is $V_{CES} = 44.6$ mV.

- (b) The collector–emitter dynamic resistance for a bipolar transistor in the saturation region r_{CES} is (2.84)

$$r_{CES} = \left. \frac{dV_{CES}}{dI_{CES}} \right|_{I_B=\text{const}} = \frac{\varphi_I}{I_B} \left[\frac{1}{1 + \beta_I + \frac{\beta_N}{F_S}} + \frac{1}{\beta_N - \frac{\beta_N}{F_S}} \right].$$

For $R_C \rightarrow \infty$ the dynamic resistance is

$$r_{CES} = \frac{\varphi_I}{I_B} \left[\frac{1}{1 + \beta_I} + \frac{1}{\beta_N} \right] = 6.18 \Omega.$$

For $R_C = R_B$ the collector–emitter resistance is

$$r_{CES} = \frac{\varphi_I}{I_B} \left[\frac{1}{2 + \beta_I} + \frac{1}{\beta_N - 1} \right] = 3.83 \Omega.$$

2.2.3 Static Transfer Characteristic

It is customary that the static states of a switching circuit are defined by the voltage transfer characteristic which represents the dependence of the output on the input voltage, i.e. $V_o = f(V_I)$. There are three parts of the characteristic (Fig. 2.20). In the first part $V_I < V_{BEt} \approx 0.5$ V and the transistor is off. In the vicinity of V_{BEt} the transistor is in the region of weak conduction. However, the collector current is still negligible compared to I_{CS} . Let $V_{BE}/(m_e \varphi_I) = 5$. Then, from (2.46) and (2.47)

$$I_C = \frac{1 + \alpha_I e^5}{1 - \alpha \alpha_I} I_{CO} \approx \alpha_I e^5 I_{CO}, \quad (2.86)$$

and the output voltage is

$$V_{OH} = V_O(V_{BEt}) = V_{CC} - R_C \alpha_I e^5 I_{CO}. \quad (2.87)$$

Let, e.g. $V_{CC} = 5$ V, $R_C = 1$ k Ω , and $\alpha_I = 0.3$. Then $V_{OH} = V_{CC} - 223 \times 10^{-6} \text{V} \approx V_{CC}$ for $I_{CO} = 5$ nA and $V_{OH} = V_{CC} - 223 \times 10^{-3} \text{V} \approx V_{CC}$ for $I_{CO} = 5$ μA . Thus, the voltage drop across this resistance is negligible compared to V_{CC} . For this

reason, it is taken that for all voltages $V_I < V_{BEt}$ the transistor is off and the output voltage is equal to the supply voltage V_{CC} .

In the second part of the characteristic the transistor is in the active region. According to (2.46), (2.47), and (2.50), the collector current is:

$$I_C = \frac{\alpha_I}{1 - \alpha\alpha_I} I_{C0} e^{\frac{V_I}{m_e \varphi_I}} + \frac{I_{C0}}{1 - \alpha\alpha_I}. \quad (2.88)$$

Since now $\alpha \approx 1$, $\alpha\alpha_I \approx \alpha_I$, the second member in (2.88) is negligible and

$$V_O = V_{CC} - \beta_I I_{C0} R_C e^{\frac{V_I}{m_e \varphi_I}}. \quad (2.89)$$

The output voltage drops quickly with the increase of V_I until the transistor enters the saturation region. The difference

$$\Delta V_I = V_{BESf} - V_{BEt} \quad (2.90)$$

is the transition region width of the transfer characteristic. V_{BESf} is the input voltage for which the transistor is at its boundary between the active and the saturation region. This voltage can be obtained from (2.89) for $V_O = V_{CES}$. This voltage should be increased by the voltage drop across the base resistance r_{bs} . At last one obtains

$$\Delta V_I = \frac{r_{bs} I_{CS}}{\beta} + \varphi_I \ln \frac{I_{CS}}{\beta_I I_{C0}} - V_{BEt}. \quad (2.91)$$

Typically $\Delta V_I = (0.1-0.2)$ V. In general, however, the width of the transition region is defined as the difference between the input voltages for which the voltage gain is -1 , i.e. $dV_O/dV_I = -1$.

The voltage difference between the high and the low output levels is the amplitude of the output voltage, i.e.,

$$V_m = V_{OH} - V_{OL} = V_{CC} - V_{CES} \approx V_{CC}.$$

The input voltage for which the unity gains straight line crosses the transfer characteristic (point T in Fig. 2.21) is called the threshold voltage V_t of the switching circuit. Consequently, here $V_{BEt} < V_t < V_{BESf}$. Owing to the small transition region width ΔV_I it is mainly taken that $V_t \approx V_{BEt}$ and for silicon transistors typically $V_t \approx 0.6$ V. The transfer characteristic (Fig. 2.21) is inverting (low input results in high output and vice versa) and the switching circuit is called an inverter. Since the transistor is a current controlled switch, but the voltage control predominates, a resistor R_B is inserted in the base (Fig. 2.22a).

A realistic inverter circuit, its drive, and the response are shown in Fig. 2.22. The high input level is $V_{IH} = V_{BB1}$. The transistor must then be in the saturation region, i.e.

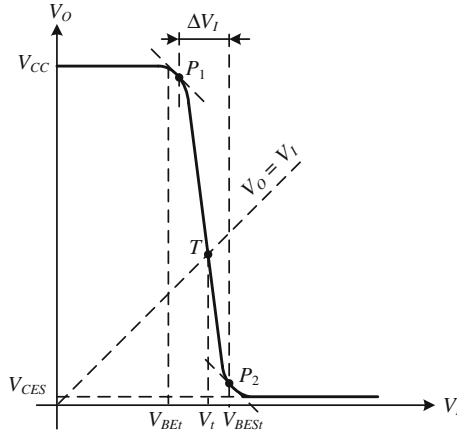


Fig. 2.21 Transfer characteristic

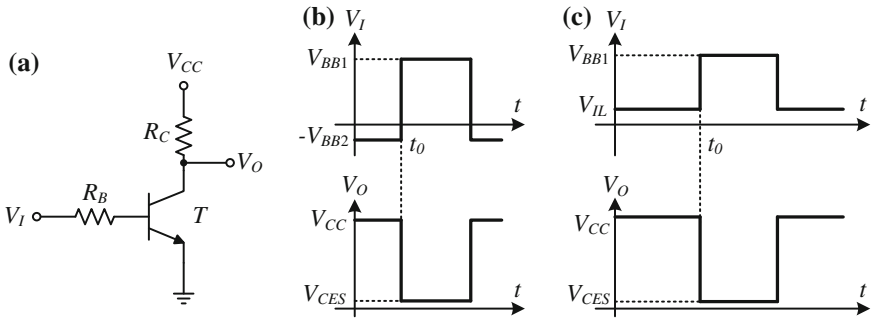


Fig. 2.22 Inverter (a) and idealized pulse waveforms of driving and response voltages (b, c)

$$I_B = \frac{V_{BB1} - V_{BES}}{R_B} \geq I_{BS}. \quad (2.92)$$

From (2.92) and (2.79) it follows:

$$R_B \geq \beta R_C \frac{V_{BB1} - V_{BES}}{V_{CC} - V_{CES}} \quad (2.93)$$

usually $V_{BB1} = V_{CC} \gg V_{BES}$. The current gain β depends on the collector current and temperature (Fig.2.21) and one should perform calculations using its minimum value. Therefore, under the specified operating conditions a transistor will be in saturation if

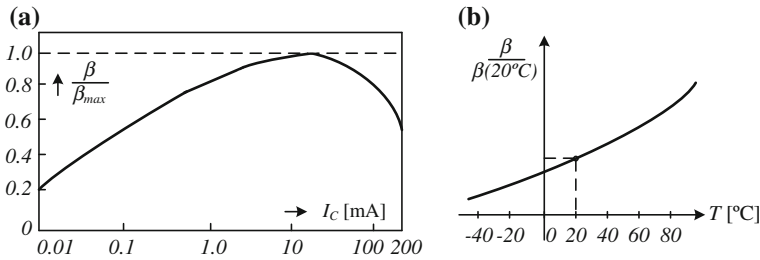


Fig. 2.23 The ratio $\beta/\beta_{\max}$ as function of collector current (a) and temperature (b)

$$R_B \geq \beta_{\min} R_C. \quad (2.94)$$

The temperature characteristic of the current gain β is a growing exponential function (Fig. 2.23b). However, over a wide range of temperatures (-20 to $+60$ °C) it is almost linear and can be approximated by

$$\beta(T) = \beta(T_0) + C_A[1 + \beta(T_0)](T - T_0), \quad (2.95)$$

where T_0 is the room temperature and:

$$C_A = \frac{d\beta}{\beta(T_0)dT} \quad (2.96)$$

is the relative temperature coefficient of the current gain β (it has been assumed that $\beta(T_0) \gg 1$) C_A ranges from 0.1 to 1 % per °C for silicon transistors.

Wherever possible one should try to make the low level input voltage negative (Fig. 2.22b). In practice, however, the input is as shown in Fig. 2.22c, where $V_{IL} < V_{BEt}$ must be satisfied.

2.2.4 Dynamic Inverter Characteristics

The response of an inverter to an abrupt input voltage change is not instantaneous, as shown in Fig. 2.22b, c. In reality, a certain amount of time is always required for the change of the output voltage. In other words, a transistor cannot be instantaneously switched on or off.

It is known that the transistor parameters depend upon the operating frequency. The transient regimes are analyzed at very fast changes of the input voltage, which correspond to very high frequencies. This means that in the analysis of transient regimes the high frequency equivalent circuits and the corresponding parameters should be used. For instance, owing to the influence of the emitter capacitance at high frequencies the common-base current gain is

$$\alpha = \frac{\alpha_0}{1 + j\omega C_e r_e}, \quad (2.97)$$

where α_0 is the low frequency current gain, ω is the circular frequency, C_e and r_e are the respective emitter capacitance and resistance. By putting the time constant

$$C_e r_e = 1/\omega_\alpha \quad (2.98)$$

one obtains

$$\alpha(\omega) = \frac{\alpha_0}{1 + j\omega/\omega_\alpha}. \quad (2.99)$$

Figure 2.24 illustrates the frequency characteristic of the current gain α . At the cut off frequency the gain is, by definition, 3 dB lower, i.e. $\sqrt{2}$ times lower. Thus, ω_α is the circular cut off frequency of a transistor in the common-base connection. The dominant influence on the emitter capacitance, while the transistor is on, is due to the diffusion capacitance. The time constant (2.98) is equal to the base time constant, τ_α . Since the diffusion capacitance is approximately:

$$C_{ed} \approx \frac{W_B^2}{2D_n r_e}, \quad (2.100)$$

then

$$\sigma_\alpha = \frac{1}{\omega_\alpha} \approx \frac{W_B^2}{2D_n}, \quad (2.101)$$

where W_B is the basewidth and D_n is the diffusion constant. Therefore, the narrower the base, the shorter the time constant τ_α , and the higher the cut off frequency ω_α .

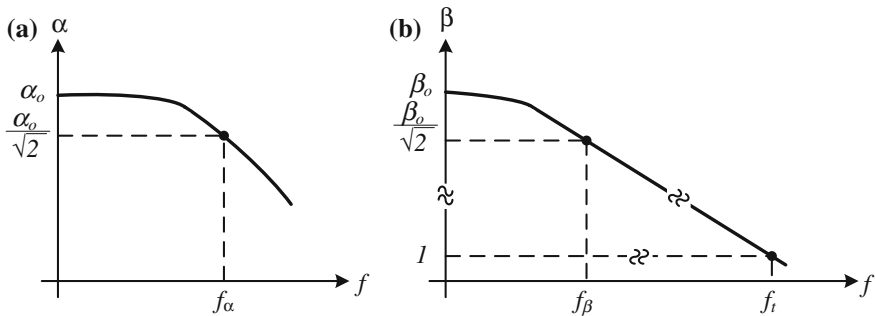


Fig. 2.24 Frequency characteristics $\alpha(\omega)$ (a) and $\beta(\omega)$ (b)

The diffusion constant of electrons in silicon is about 2.5 times higher than that of holes. Thus, an *nnp* transistor under the same conditions possesses about 2.5 times higher cut-off frequency compared to a PNP transistor.

The current gain of a transistor in the common-emitter connection is

$$\beta(\omega) = \frac{\alpha(\omega)}{1 - \alpha(\omega)} = \frac{\beta_0}{1 + j\omega/\omega_\beta}, \quad (2.102)$$

where $\beta_0 = \alpha_0/(1 - \alpha_0)$ is the low frequency signal gain,

$$\omega_\beta = (1 - \alpha_0)\omega_\alpha = \frac{\omega_\alpha}{\beta_0 + 1} \quad (2.103)$$

is the angular cut off frequency of the common-emitter connection, and its time constant is

$$\tau_\beta = 1/\omega_\beta = (\beta_0 + 1)/\omega_\alpha = (\beta_0 + 1)\tau_\alpha. \quad (2.104)$$

The cut off frequency ω_β is thus $\beta_0 + 1$ times lower than ω_α and the time constant is $\beta_0 + 1$ times higher than τ_α . Figure 2.23b shows the *frequency characteristic of the gain β* . The manufacturers often give the unity gain frequency f_T . This is the frequency at which $|\beta(f_T)| = 1$ and f_T is also called the frequency range of the transistor gain. From the condition $|\beta(f_T)| = 1$ and Eq. (2.102) it follows that

$$f_T = \sqrt{\frac{\beta_0 - 1}{\beta_0 + 1}} f_\alpha \approx f_\alpha, \quad (2.105)$$

because $\beta_0 \gg 1$. Typical values for f_T range from several hundreds MHz to several GHz.

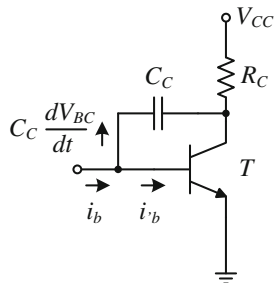
Equations (2.99) and (2.102) can be used for the analysis of the transient modes when the transistor is in the active region. In general, however, a transistor as a switch goes through all regions. For this reason the general charge control method is more suitable for the dynamic analysis of switches. Analogously to diode processes, a change of the charge of minority carriers in the base dQ/dt is caused by the change of the base current, $i_b(t)$, and the recombination of minority carriers in the base $-Q/\tau$, i.e.

$$\frac{dQ}{dt} = i_b(t) - \frac{Q}{\tau}. \quad (2.106)$$

In the active region of a transistor in the common-emitter connection $\tau = \tau_\beta$ and

$$\frac{dQ}{dt} + \frac{Q}{\tau_\beta} = i_b(t). \quad (2.107)$$

Fig. 2.25 Equivalent circuit in the active region



The collector current is proportional to the base charge, i.e.

$$i_c(t) = \frac{\beta}{\tau_\beta} Q(t). \quad (2.108)$$

Equation (2.107) applies for the active region if $R_C = 0$. However, $R_C > 0$ and it does have an influence on the time constant. Namely, in the active region the collector junction is reverse biased and behaves like a capacitor. If the average value of the capacitance of this junction is denoted by C_c , the transistor can be considered as a “pure” transistor plus the capacitor C_c (Fig. 2.25). The current i_b is expressed by (2.107) and

$$i_b(t) = C_c \frac{dV_{BC}}{dt} + \frac{dQ}{dt} + \frac{Q}{\tau_\beta}. \quad (2.109)$$

If the change of the voltage V_{BE} is neglected, then

$$\frac{dV_{BC}}{dt} = -\frac{dV_{CE}}{dt} \approx R_C \frac{di_c}{dt}. \quad (2.110)$$

In view of (2.108), from (2.109) and (2.110) it follows

$$\frac{dQ}{dt} + \frac{Q}{\tau_{\beta_e}} = \frac{\tau_\beta}{\tau_{\beta_e}} i_b(t), \quad (2.111)$$

where

$$\tau_{\beta_e} = \tau_\beta + \beta C_c R_C. \quad (2.112)$$

Thus, the influence of the collector capacitance manifests itself as an increase of the time constant. If a transistor is in the common-base connection, then, according to (2.112) and (2.104)

$$\tau_{\alpha e} = \tau_{\alpha} + C_c R_C. \quad (2.113)$$

The capacitance C_c depends upon the transistor type and usually is within the range from the order of pF to the order of fF . The general solution of (2.111) is given by:

$$Q(t) = e^{-\frac{t}{\tau_{\beta e}}} \left[\int_0^t \frac{\tau_{\beta}}{\tau} i_b(t) e^{\frac{t}{\tau_{\beta e}}} dt + Q(0) \right], \quad (2.114)$$

where $Q(0)$ is the integration constant and represents the charge at the beginning of the analyzed transient process.

2.2.4.1 Transistor Turn On

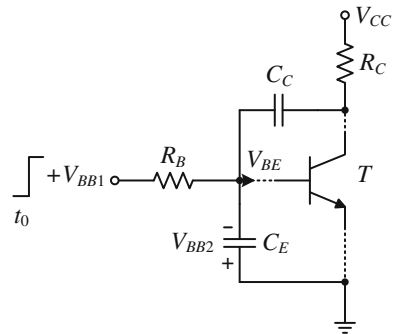
The transient regime of an inverter (Fig. 2.21) caused by an abrupt input drive (Fig. 2.22b) will be considered. Up to the instant t_0 the transistor is off. Both p-n junctions are reverse biased and can be considered capacitors of medium capacitances C_c and C_e . At t_0 the input voltage abruptly changes from $-V_{BB2}$ to $+V_{BB1}$ (Fig. 2.27a). At this instant the transistor turn-on process begins and unfolds in two phases. During the first phase (Fig. 2.27) the capacitor $C_t = C_c + C_e$ must be recharged. The collector current at this instant is zero so that C_c and C_e are practically connected in parallel. At the beginning

$$V_{BE}(t) = V_{BB1} - (V_{BB1} + V_{BB2}) e^{-\frac{t}{C_t R_B}}. \quad (2.115)$$

For $V_{BE}(t_{d1}) = V_{BEt}$ the emitter diode becomes conductive and

$$t_{d1} = C_t R_B \ln \frac{V_{BB1} + V_{BB2}}{V_{BB1} - V_{BEt}} \approx C_t R_B \ln \left(1 + \frac{V_{BB2}}{V_{BB1}} \right). \quad (2.116)$$

Fig. 2.26 Equivalent circuit for delay time t_{d1}



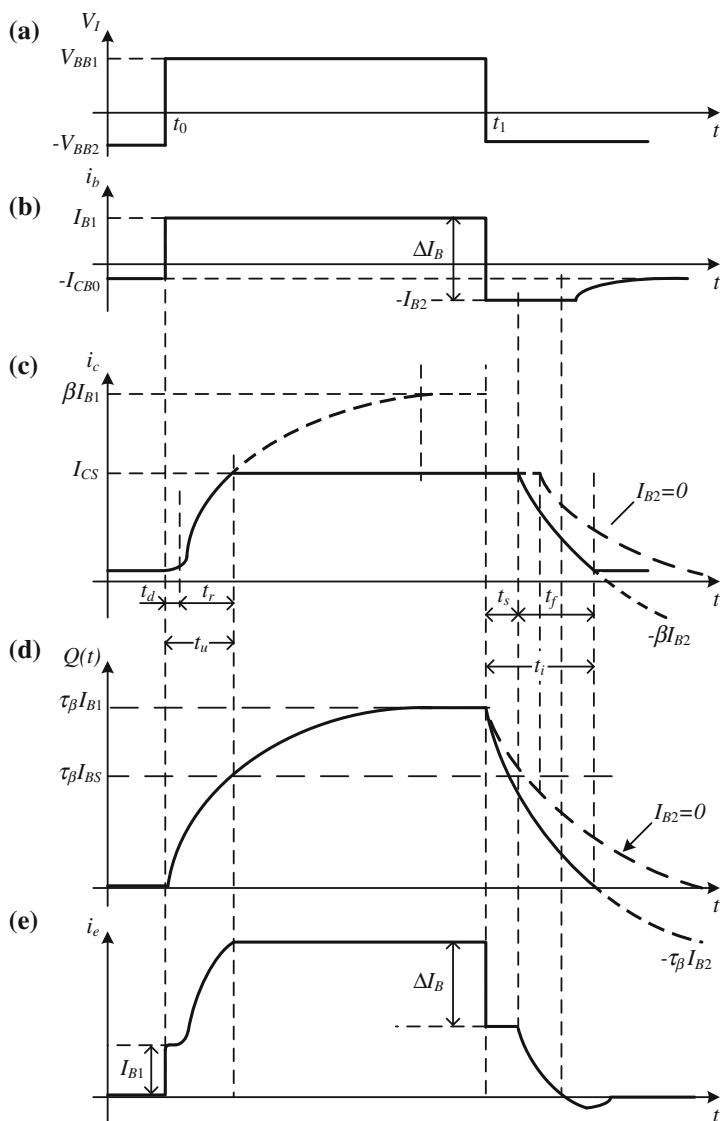


Fig. 2.27 Pulse waveforms of excitation voltage (a), base current (b), collector current (c), base charge (d) and emitter current (e)

After t_{d1} , during $t_{d2} \approx 0.22\tau_a$, the collector current is zero. This delay is the consequence of the finite time required for the transportation of charge carriers through the base. The total delay time of the beginning of the response (collector current or output voltage) is thus

$$t_d = t_{d1} + t_{d2}. \quad (2.117)$$

Usually $t_{d1} \gg t_{d2}$ and $t_d \approx t_{d1}$. After t_d the collector current increases. By introducing in (2.114)

$$i_b(t) = \frac{V_{BB1} - V_{BE}}{R_B} = I_{B1} \quad (2.118)$$

and $Q(0) = 0$, because there are still no excess minority charge carriers, from (2.114) and (2.108) it follows

$$i_c(t) = \beta I_{B1} \left(1 - e^{-\frac{t}{\tau_{\beta e}}} \right). \quad (2.119)$$

The increase of the collector current ends by turning the transistor enters saturation, i.e.

$$i_c(t_r) = I_{CS}. \quad (2.120)$$

From (2.119) and (2.120) the rise time is

$$t_r = \tau_{\beta e} \ln \frac{\beta I_{B1}}{\beta I_{B1} - I_{cs}} = \tau_{\beta e} \ln \frac{I_{B1}}{I_{B1} - I_{BS}}. \quad (2.121)$$

The total turn-on time of the transistor is

$$t_u = t_d + t_r. \quad (2.122)$$

After t_r the collector current is constant (Fig. 2.27c) and the charge in the base increases until a steady state is reached (Fig. 2.27d).

2.2.4.2 Transistor Turn Off

While in saturation, both p-n junctions of the transistor are forward biased. Both the emitter and the collector inject minority carriers into the base. By superimposing the charges of the normal and the reverse active modes the total distribution of charge in the base is obtained (Fig. 2.28a). The shaded part represents the charge in excess compared to the one at the boundary between the active and the saturation states.

The turn-off process of transistor is initiated at the instant $t = t_1$ by a negative change of input from $+V_{BB1}$ to $-V_{BB2}$. As long as the concentration of minority carriers at the emitter-junction boundary is greater than zero a negative base current will flow

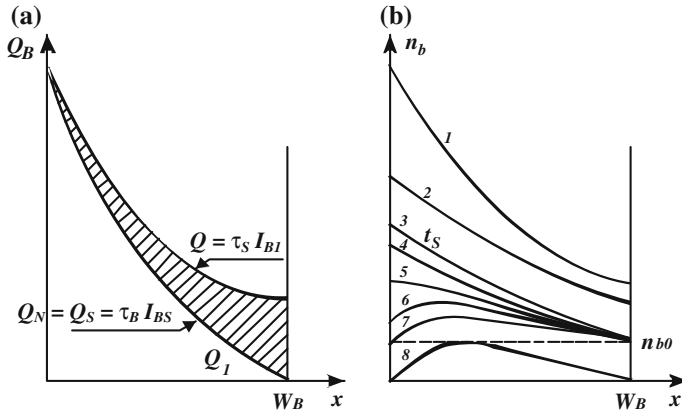


Fig. 2.28 The distributions in base: of the charge in saturation (a) and the concentration of electrons during the turn-off process (b)

$$I_{B2} \approx V_{BB2}/R_B. \quad (2.123)$$

This current “sweeps” the accumulated charge in the base. The turn-off process also unfolds in two phases. During the first phase the collector current remains constant, i.e. $I_C = I_{CS}$ (Fig. 2.27). During that time the excess charge (the shaded part in Fig. 2.28a) which is the consequence of the forward bias of the collector junction is “swept away”. This process lasts as long as the concentration of the minority carriers at the collector junction is greater than zero. The collector current is constant since the slope of the distribution at the end of the base is constant (curves 2 and 3 in Fig. 2.28b). At the end of this interval, which is called the storage time t_s , the concentration of minority carriers at the boundary of the collector junction is zero. Practically, the excess charge has been “swept away” and the transistor “returned” from saturation to the active region.

The change of $Q(t)$ in the base during t_s can be determined from (2.114). For this purpose: $i_b = -I_{B2}$ and the initial charge is $Q(0) = \tau_s I_{B1}$, where τ_s is the time constant of the transistor in saturation. This time constant depends upon time constants in the forward and the reverse modes. Usually $0.5\tau_\beta < \tau_s < 2\tau_\beta$. It is generally taken that $\tau_s \approx \tau_\beta$. During t_s the collector junction is forward biased and $\tau_{pe} \approx \tau_\beta$. Based on this, from (2.114) it follows:

$$Q(t) = -\tau_\beta I_{B2} + \tau_\beta (I_{B1} + I_{B2}) e^{-\frac{t}{\tau_\beta}}. \quad (2.124)$$

From the condition $Q(t) = Q_s = \tau_\beta I_{BS}$ and (2.124) t_s is

$$t_s = \tau_\beta \ln \frac{I_{B1} + I_{B2}}{I_{BS} + I_{B2}}. \quad (2.125)$$

After t_s the collector current decreases. The collector junction is reverse biased and the time constant $\tau_{\beta e}$ is valid. From (2.114) and (2.108) together with the initial condition $Q(0) = Q_s = \tau_{\beta} I_{BS}$ it follows

$$i_c(t) = \beta (I_{B2} + I_{BS}) e^{-t/\tau_{\beta e}} - \beta I_{B2}. \quad (2.126)$$

The turn-off process ends when $i_c(t_f) = 0$ and the fall-off time of the collector current is

$$t_f = \tau_{\beta e} \ln(1 + I_{BS}/I_{B2}). \quad (2.127)$$

The total turn-off time is

$$t_i = t_s + t_f. \quad (2.128)$$

In practice, it is often $V_{BB2} = 0$. This means that the base turn-off current is $I_{B2} = 0$. The process of clearing charge carriers from the base is then slower (dotted lines for the variations of i_c and Q in Fig. 2.27) and is practically due to recombination. The storage time in this case is approximately

$$t_s \approx \tau_{\beta} \ln \frac{I_{B1}}{I_{BS}} = \tau_{\beta} \ln F_s, \quad (2.129)$$

where F_s is the saturation factor. In theory, from the condition $i_c(t_f) = 0$ and for $I_{B2} = 0$, $t_f \rightarrow \infty$. For this reason the condition is $i_c(t_f) = 0.1 I_{CS}$ and

$$t_f \approx 2.3 \tau_{\beta e} = 2.3(\tau_{\beta} + \beta C_C R_C). \quad (2.130)$$

When $V_{BB2} = 0$, the resistance between the base and the emitter should be as small as possible in order to speed up the process of clearing the piled up charge. It should be pointed out that the above analysis is approximate. First of all the base current is not constant throughout the turn-off time. In addition, the time constant of the transistor changes. For $i_c = |I_{B2}|$, the slope of the minority carrier distribution in the base at the junction boundary is zero (curve 5 in Fig. 2.28b). Until then the basewidth is w_B . After that the concentration gradient at the junction boundary changes direction (curve 6 in Fig. 2.28b) and the emitter current becomes negative (Fig. 2.27). At $n_b = n_{b0}$ the effective base width decreases and so does the transistor time constant. All this is very complex for a mathematical description.

A particular attention should be paid to turning off the transistor by a large base current when $|I_{B2}| > I_{CS}$. The minority carrier distribution in the base and the pulse waveforms of the currents for this case are shown in Fig. 2.29. The emitter current is then negative $I_{ES2} = I_{CS} + I_{B2} = I_{CS} - |I_{B2}| < 0$. The minority carrier distribution curves in the base exhibit maxima (curves 2 and 3 in Fig. 2.29a). The minority carrier concentration decreases at both the emitter and the collector junctions. In that case, the equilibrium concentration may be reached at the emitter junction first (Fig. 2.29).

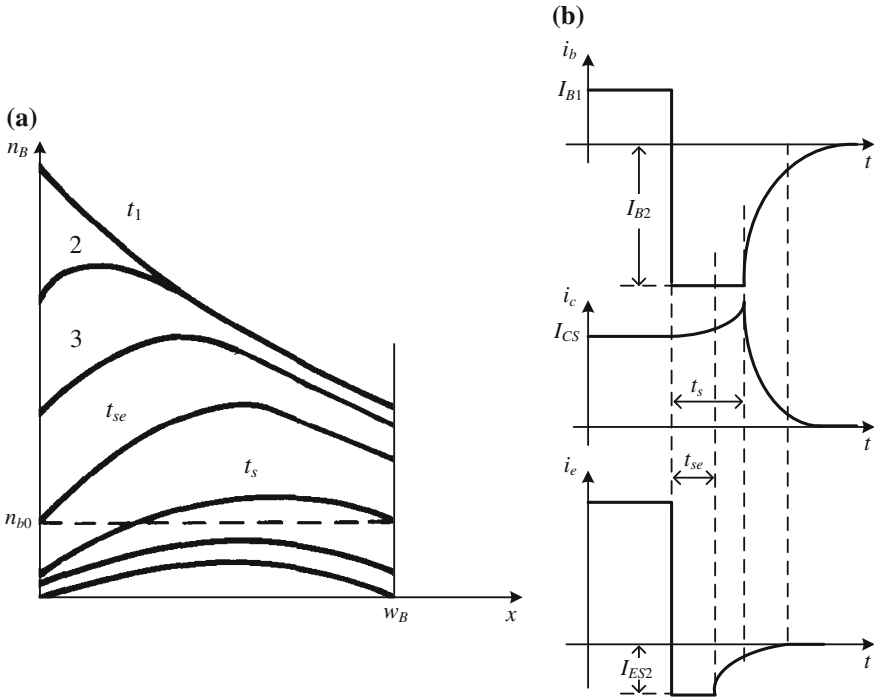


Fig. 2.29 Minority carrier distribution in the base (a) and transistor currents if $I_{B2} > I_{CS}$ (b)

One speaks then about the emitter clearance of the excess charge in the base. Since at t_{se} at the collector junction $n_b > n_{B0}$, the transistor goes to the reverse active mode (the emitter junction reverse biased and the collector junction forward biased). The emitter storage time can be determined from the condition

$$Q(t_{se}) = \frac{\tau_s}{\beta_I} I_{ES2} = \frac{\tau_s}{\beta_I} (I_{B2} - I_{CS}). \quad (2.131)$$

on the basis of (2.124) and (2.131) one obtains

$$t_{se} = \tau_s \ln \frac{I_{B1} + I_{B2}}{I_{B2}/\alpha_I - I_{CS}/\beta_I}. \quad (2.132)$$

The emitter clearance will happen if $t_{se} < t_s$, and from (2.125) and (2.132) it turns out that the base current in that case must be

$$I_{B2} > I_{CS}(1 + \beta_I/\beta). \quad (2.133)$$

After t_{se} the emitter current decreases and the collector current increases (Fig. 2.29b) until the minority carrier concentration at the collector junction equals

the equilibrium concentration. The transistor then goes from the reverse active region to the cut-off region. The currents fall to their steady state values ($I_C \approx I_{CBO}$, $I_B \approx -I_{CBO}$, $I_E \approx 0$). The effective basewidth narrows because both p-n junctions are reverse biased and the transistor time constant is several times smaller than τ_a . This means that the decrease of the currents I_B , I_C , and I_E is very fast.

Example 2.3 For the circuit from Fig. 2.30 and the excitation shown in Fig. 2.31 determine:

- the resistance R_C so the transistor is in saturation with a factor of saturation 5, and
- the transistor turn on (t_{ON}) and the turn off (t_{off}) time.

The circuit of Fig. 2.30 has $R = 2 \text{ k}\Omega$, $\beta_{\min} = 20$, $\tau_\beta = 100 \text{ ns}$, $C_c = 4 \text{ pF}$, $C_e = 10 \text{ pF}$, $V_{BE} = 0.6 \text{ V}$, $V_{BES} = 0.7 \text{ V}$, $V_{BE} = 0.6 \text{ V}$, $V_{CES} = 0.1 \text{ V}$ and $V_{CC} = 12 \text{ V}$.

- The coefficient of saturation is equal to the quotient of the base current that keeps the transistor in the saturation region and the base current of the transistor, which is the boundary between the active and the saturation region:

$$F_S = \frac{I'_{B1}}{I_{BS}}.$$

Fig. 2.30 Bipolar transistor switch

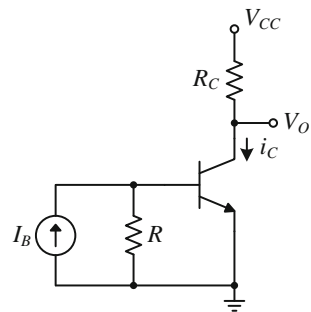
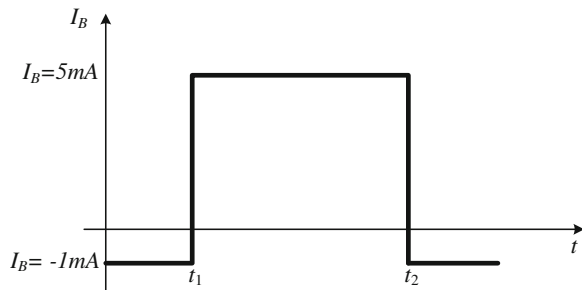


Fig. 2.31 Waveform of current excitation for the circuit shown in Fig. 2.30



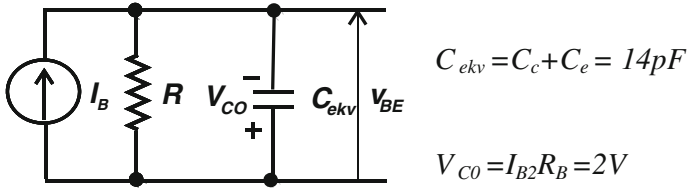


Fig. 2.32 Circuit of charging equivalent input parasitic capacitance while turning on the switch from Fig. 2.30

The base current when the transistor is in the saturation region is (Fig. 2.30)

$$I'_{B1} = I_{B1} - \frac{V_{BES}}{R} = 4.65 \text{ mA}. \quad (2.134)$$

The base current which holds the transistor at the boundary between the active and the saturation region is

$$I_{BS} = \frac{I_{CS}}{\beta} = \frac{V_{CC} - V_{CES}}{\beta R_C}. \quad (2.135)$$

From (2.134), (2.135) and the conditions of the task is obtained that

$$R_C = \frac{F_S(V_{CC} - V_{CES})}{\beta I'_{B1}} = 634 \Omega.$$

(b) The turning on time of the transistor is equal to the sum of t_d and t_r

Interval $t_1 < t < t_1 + t_d$ (time t_d)

To determine the time t_d the equivalent scheme shown in Fig. 2.32 can be used

The voltage between the emitter and the base is equal to (Fig. 2.32)

$$v_{BE}(t) = I_{B1}R - (I_{B1}R + V_{CO})e^{-\frac{t}{\tau_{ekv}}}.$$

From the condition $v_{BE}(t_d) = V_{Bet}$ one obtains

$$t_d = C_{ekv}R \ln \frac{I_{B1}R + V_{CO}}{I_{B1}R - V_{Bet}} = 6.83 \text{ ns}.$$

Interval $t_1 + t_d < t < t_1 + t_d + t_r$ (time t_r)

To determine the time t_r the general charge control method for the dynamic analysis of switches is suitable. Change of the minority carriers concentration in the base dQ/dt is caused by the change of the base current, i_b , and the recombination of minority carriers in the base. The current i_b is constant during this period and approximately equal to

I'_{B1} . In this time interval, the transistor is in the active mode, so the collector p-n junction is reverse biased and the capacitance of the p-n junction has to be taken into account. So, for the determination of the time t_r the following equation is used:

$$\frac{dQ(t)}{dt} = I'_{B1} - \frac{Q(t)}{\tau_{\beta e}}, \quad \text{where} \quad \tau_{\beta e} = \tau_{\beta} + \beta R_C C_C. \quad (2.136)$$

Based on the initial condition $Q(t_1 + t_d) = 0$, the condition for the transistor entering the saturation region $Q(t_1 + t_d + t_r) = \tau_{\beta} I_{BS}$ and on the solution of the Eq. (2.136) the time t_r is calculated as

$$t_r = \tau_{\beta e} \ln \frac{1}{1 - 1/F_S} = 33.4 \text{ ns}.$$

The turning on time of the transistor is equal to: $t_{ON} = t_d + t_r = 40.23 \text{ ns}$.

The turning off time of the transistor t_{OFF} is equal to the sum of t_s and t_f .

Interval $t_2 < t < t_2 + t_s$ (time t_s)

In this interval, the transistor is in saturation, both p-n junctions are forward biased and Eq. (2.106) can be applied. The initial condition is $Q(t_2) = \tau_{\beta} I'_{B1}$, and a prerequisite for the end of this interval is that the transistor is at the boundary between the saturation and active region $Q(t_2 + t_s) = \tau_{\beta} I_{BS}$. By solving Eq. (2.106) with the above mentioned conditions one obtains

$$t_s = \tau_{\beta} \ln \frac{I'_{B1} - I'_{B2}}{I_{BS} - I'_{B2}} = 149.2 \text{ ns}, \quad \text{where} \quad I'_{B2} = I_{B2} + V_{BES}/R.$$

Interval $t_2 + t_s < t < t_2 + t_s + t_f$ (time t_f)

At the beginning of this interval, the transistor is at the boundary between the saturation and the active region. The initial condition is $Q(t_2 + t_s) = \tau_{\beta} I'_{B1}$, and the prerequisite for the end of this interval is that the transistor is turned off $Q(t_2 + t_s + t_f) = 0$. By solving the equations

$$\frac{dQ(t)}{dt} = I'_{B2} - \frac{Q(t)}{\tau_{\beta e}}.$$

with the above conditions one obtains

$$t_f = \tau_{\beta e} \ln \frac{I'_{B2} + I_{BS}}{I'_{B2}} = 130 \text{ ns}.$$

The turning off time of the transistor is $t_{OFF} = t_s + t_f = 279.2 \text{ ns}$.

2.2.4.3 Optimum Drive

It has been shown that the times t_r , t_s , and t_f are dependent on the base currents I_{B1} and I_{B2} . The rise time can be written in the form

$$t_r = -\tau_{\beta e} \ln(1 - I_{BS}/I_{B1}). \quad (2.137)$$

The lower the ratio I_{BS}/I_{B1} the smaller t_r . If $I_{B1} \gg I_{BS}$, (2.137) can be expanded to a Maclaurin series and since it is known that $\ln(1 - x) \approx -x$ for $x \ll 1$, one obtains

$$t_r \approx \tau_{\beta e} I_{BS}/I_{B1} = (\tau_a + C_c R_C) I_{CS}/I_{B1}. \quad (2.138)$$

A small ratio $I_{BS}/I_{B1} = I_{CS}/\beta I_{B1} = 1/F_S \ll 1$ can be accomplished either by a small current I_{CS} or by a large current I_{B1} .

The condition $I_{B1} \gg I_{BS}$ for a small t_r means strong saturation of the transistor ($F_S \gg 1$) which implies a long storage time t_s . On the other hand, from (2.126) it follows that $t_s = 0$ for $I_{B1} = I_{BS}$, i.e., if the transistor is at the boundary between the active and the saturation region. In that case, however, $t_r \rightarrow \infty$. Therefore, the requirements for small t_r and t_s are mutually contradictory. The compromise is the drive shown in Fig. 2.33. While the transistor is being driven on, the base current is $I_B = I_{B1} \gg I_{BS}$, and upon reaching saturation it drops to $I_B = I_{BS}$ (Fig. 2.33). According to (2.127) the larger I_{B2} , the shorter t_f . Therefore, the optimum waveform of the base current is as shown in Fig. 2.33. If $I_{B2} \gg I_{BS}$, then, upon expansion of (2.127) to a Maclaurin series, it is approximately

$$t_f \approx (\tau_a + C_c R_C) I_{CS}/I_{B2}. \quad (2.139)$$

Both t_r and t_s are smaller if I_{BS} or I_{CS} are smaller. This current can be made smaller by increasing the resistance R_C . This, however, helps decreasing t_r and t_f only for small values of R_C (Fig. 2.34) when $C_c R_C \ll \tau_a$. If $C_c R_C \ll \tau_a$, times t_r and

Fig. 2.33 Optimum waveform of base current

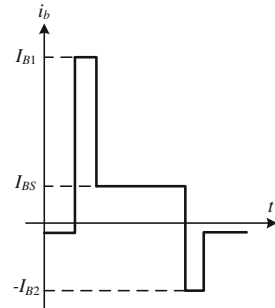
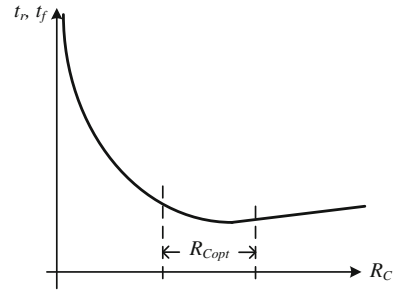


Fig. 2.34 Rise time and fall time as functions of collector load



t_f are almost independent of R_C . In practice, R_C is usually within several hundreds Ω to several $k\Omega$.

2.2.4.4 Speed Up Capacitor

In practice, the base current shown in Fig. 2.33 can only approximately be realized. One of the possibilities is the application of a speed up capacitor (Fig. 2.35a). Usually, R_1 is the internal resistance of the drive and

$$R_1 \ll R_B. \quad (2.140)$$

The variations of the base and the collector current are shown in Fig. 2.36b. The capacitor is a short circuit for abrupt changes and

$$i_b(0) = I_{B1} = \frac{V_{CC} - V_{BE}}{R_1} \approx \frac{V_{CC}}{R_1}. \quad (2.141)$$

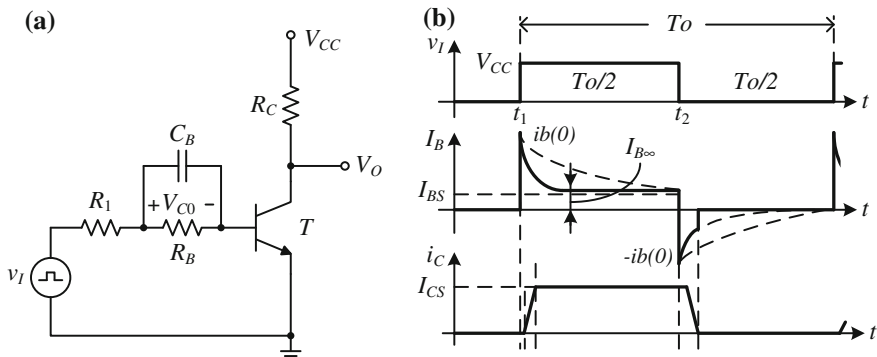
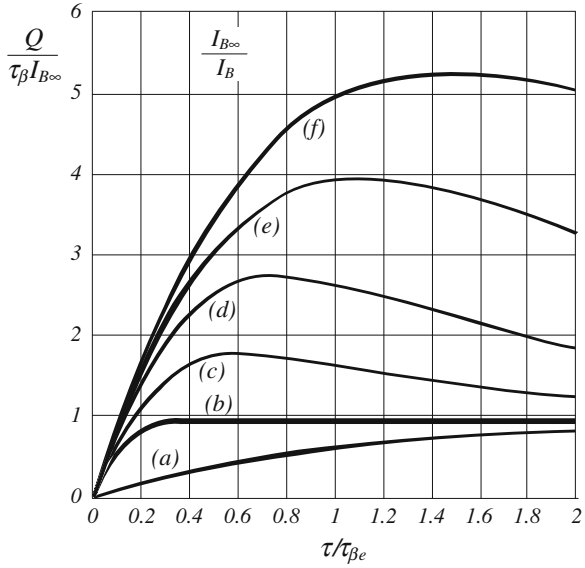


Fig. 2.35 Basic switching circuit comprising a speed up capacitor (a) and the pulse waveforms of the base and collector currents for a pulse drive (b)

Fig. 2.36 Relative base charge as function of time and the ratio $\tau/\tau_{\beta e}$: 0 (a); I_B/I_{B1} (b); 1 (c); 10 (d); 100 (e) with $I_B/I_{B1} = 0.1$



Usually, $R_1 < R_C$, so $i_b(0) \gg I_{BS}$, and according to (2.138)

$$t_r \approx (\tau_\alpha + C_c R_C) R_1 / R_C. \quad (2.142)$$

While the input pulse is on, the capacitor becomes charged and the base current is:

$$i_b = I_{B\infty} = \frac{V_{CC} - V_{BES}}{R_B + R_1} \approx \frac{V_{CC}}{R_B}. \quad (2.143)$$

If $I_B = I_{BS}$, at the instant t_2 the transistor will be at the boundary of the saturation region. However, R_B is usually calculated assuming that the transistor is weakly saturated. Thus

$$R_B = (1.2/1.5)\beta R_C. \quad (2.144)$$

In this way, it is ensured that the transistor is saturated even for the worst case of tolerances of β and R_C . At the instant t_2 the capacitor C_B ensures a negative base current. Since during the previous interval it has been charged to $V_{CO} \approx V_{CC} - V_{BES} \approx V_C$, in the direction marked in Fig. 2.35a, the initial negative base current is approximately given by (2.141). Namely, during the process of clearing the base charge the base-emitter resistance can be neglected. Since the transistor is weakly saturated, the storage time is negligible and the fall time is, according to (2.139), approximately equal to the rise time t_r (2.142). Owing to the capacitor C_B a negative base current is ensured for the fast turning off of the transistor even when $V_{BB} = 0$.

The capacitance of C_B can be determined on the basis of the following two criteria:

- the shortest possible times t_r and t_f and
- the highest possible frequency of the switching circuit.

For the first criterion, the cycle of the triggering pulses, T_0 , from the input generator is known in advance, with $T_0 \gg t_u + t_i$. The capacitance C_B is then determined from the condition that during $T_0/2$ the capacitor is charged while $V_I = V_{CC}$, and discharged while $V_I = 0$. The charging time constant $\tau = C_B(R_1 \parallel R_B) \approx C_B R_1$ is much lower than the discharging time constant. Namely, during the turn-off process, while the piled up base charge is being cleared away, the base-emitter resistance is small and the discharging time constant is $\tau_2 = \tau_1 \approx C_B R_1$. After t_i the base-emitter resistance is very high and the capacitor discharges only through R_B . Since $t_i \ll \tau_1 \ll C_B R_B$ it may be considered that $\tau_2 \approx C_B R_B$ throughout $T_0/2$, while $V_i = 0$. If it is assumed that the duration of the discharging time is five time constants, then from the condition $5C_B R_B < T_0/2$ it follows that

$$C_B < 0.1 \frac{T_0}{R_B}. \quad (2.145)$$

The variation of the base current is represented in Fig. 2.35 by the dotted line. During the transient mode of the transistor, the base current is changed a little compared to the optimum (Fig. 2.33).

Criterion of the Maximum Frequency

$$F_{0\max} = \frac{1}{T_{0\min}} = \frac{1}{t_u + t_i} \quad (2.146)$$

is considerably more general. It is used when the operating frequency of the switching is known in advance. During a positive input pulse, the base current is

$$i_b(t) = I_{B\infty} + (I_{B1} + I_{B\infty})e^{-t/\tau}, \quad (2.147)$$

where I_B and $I_{B\infty}$ are determined, respectively by (2.141) and (2.143) and

$$\tau = C_B \frac{R_B R_1}{R_B + R_1} \approx C_B R_1. \quad (2.148)$$

On the basis of (2.113) and (2.143), the relative base charge is determined by:

$$\frac{Q(t)}{\tau_\beta} = I_{B\infty} + \frac{\tau}{\tau - \tau_{\beta e}} (I_{B1} - I_{B\infty}) e^{-t/\tau} - \left[I_{B\infty} + \frac{\tau}{\tau - \tau_{\beta e}} (I_{B1} - I_{B\infty}) \right] e^{-t/\tau_{\beta e}}. \quad (2.149)$$

This function is represented in Fig. 2.36 for different ratios $\tau/\tau_{\beta e}$. Without the capacitor C_B ($\tau = 0$, curve *a*) the steady state charge $Q_\infty = \tau_\beta I_{B\infty}$ is established exponentially. The rise time in this case is by far the largest. If

$$\tau = \tau_k \geq \frac{I_{B\infty}}{I_{B1}} \tau_{\beta e}. \quad (2.150)$$

then the increase of $Q(t)$ to its steady state value is very fast. For $\tau > \tau_k$, $Q(t)$ exhibits a maximum (curves *c*, *d*, *e*). If the storage time t_s should be minimal, the positive input pulse must be present until a steady state in the base ($Q_\infty = \tau_\beta I_{B\infty}$) is established. From that point of view, the optimum is $\tau = \tau_k$ (curve *b* in Fig. 2.36). According to this, and bearing in mind (2.141) and (2.143) the optimum capacitance is

$$C_{B\text{opt}} = \tau_{\beta e}/R_B. \quad (2.151)$$

It is said then that the compensation of the charges in the base and the capacitor is achieved. If it is assumed that after a steady state in the base is established the transistor is in weak saturation, i.e., $R_B \approx \beta R_C$, then, bearing in mind (2.112)

$$C_{B\text{opt}} = C_c + \tau_\alpha/R_C. \quad (2.152)$$

It may be concluded that in the case $\tau \gg \tau_k$ (curves *d* and *e*) the storage time t_s can be very large if condition $T_0 > t_r$ is not satisfied. Thus, C_B according to (2.152) is the optimum value with respect to the maximum frequency of the switch.

2.2.5 Nonsaturated Switch

Another type of the switching circuit comprising an optimum drive is shown in Fig. 2.37a. The diode D keeps the base-collector voltage at the value $V_{BC} = V_D$ when the transistor is on. If $V_D < V_{BCr}$, where V_{BCr} is the threshold voltage of the collector p-n junction, then the transistor will be in the active region. A majority of the circuits of this type uses Schottky diodes because $V_{DS} \approx 0.4 \text{ V} < V_{BCr}$. This diode keeps the transistor in the active region, but close to saturation since

$$V_{oL} = V_{BE} - V_D = 0.7 - 0.4 = 0.3 \text{ V} \approx V_{CES},$$

thus these circuits are often called the circuits based on the nonsaturated switch circuits. On the other hand, when the diode becomes conductive, it activates the

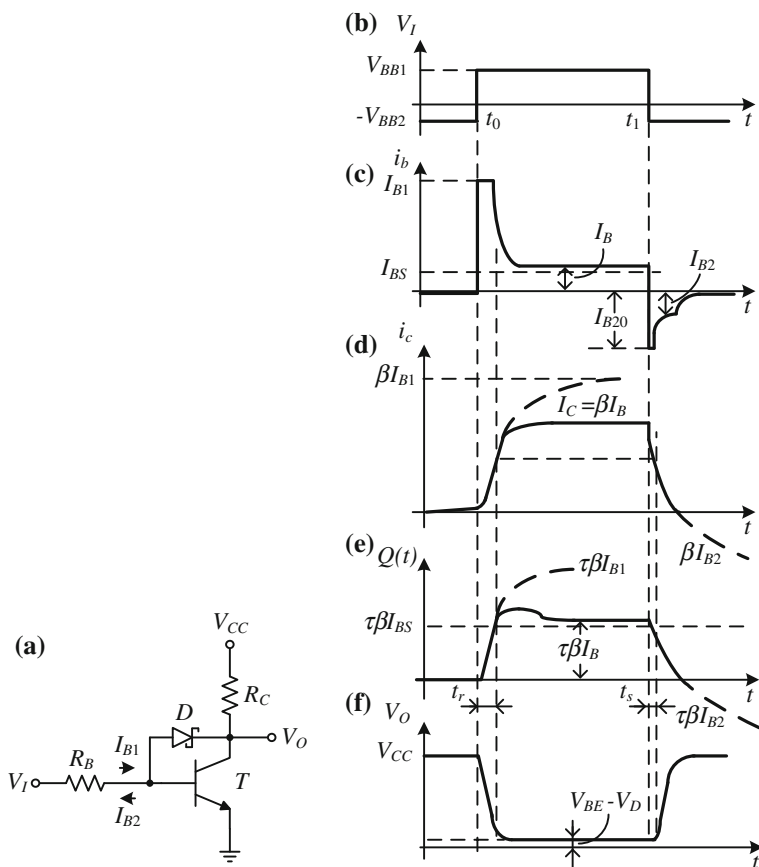


Fig. 2.37 Nonsaturated switch (a) and pulse waveforms of input (b) and output (f) voltages, base (c) and collector (d) currents, and base charge (e)

negative feedback loop which does not allow the transistor to go to saturation. For this reason these circuits are sometimes called the switching circuits comprising nonlinear feedback.

Let the drive be abrupt (Fig. 2.37b). For $t < t_0$ the transistor and the diode are off and $V_O = V_{CC}$. Upon a positive voltage step at the input at instant $t = t_0$, the transistor is switched on by the constant base current given by (2.118). The diode is off and the collector current is determined by (2.119). The output voltage is

$$V_O(t) = V_{CC} - \beta I_{B1} R_C (1 - e^{-t/\tau}), \quad (2.153)$$

where:

$$\tau'_{\beta e} = [\tau_{\beta} + \beta R_C (C_c + C_d)], \quad (2.154)$$

and C_d is the average capacitance of the reverse biased diode. The diode is turned on at instant t_1 when

$$V_d(t_1) = V_{BE} - V_O(t_1) = V_{Dt}. \quad (2.155)$$

From (2.154) and (2.155) it follows that

$$t_1 = \tau'_{\beta e} \ln \frac{\beta I_{B1}}{\beta I_{B1} - \frac{V_{CC} - (V_{BE} - V_{Dt})}{R_C}}. \quad (2.156)$$

Since the current I_{B1} through R_B is constant, upon switch-on of the diode, the base current will decrease by an amount corresponding to the diode current

$$I_{B1} = I_D + I_B. \quad (2.157)$$

After t_1 the current through R_C

$$I_{RC} = \frac{V_{CC} - (V_{BE} - V_D)}{R_C} \approx I_{CS} \quad (2.158)$$

is constant because the variations of V_{BE} and V_D are negligible. Since $V_{CE} = V_{BE} - V_D = 0.7 - 0.4 = 0.3$ V is only by 0.1 or 0.2 V greater than V_{CES} , it means that the transistor is nearly in the saturation region and that $I_{RC} \approx I_{CS}$. It can, therefore, be said that the switch-on of the diode ends the switch-on of the transistor. Indeed, expressions (2.121) and (2.156) are approximately the same since $I_{RC} \approx I_{CS}$. Thus, $t_1 = t_r$ is the rise time of the collector current.

The diode keeps the transistor in the active region, thus

$$I_C = \beta I_B = I_D + I_{RC}. \quad (2.159)$$

By combining (2.157) and (2.159) it follows that

$$I_B = \frac{I_{RC}}{\beta + 1} + I_B \frac{1}{\beta + 1}. \quad (2.160)$$

Since $I_{RC} \approx I_{CS} = \beta I_{BS}$, the base current is

$$I_B = \alpha I_{BS} + \frac{I_{B1}}{\beta + 1}. \quad (2.161)$$

This means that the base current is somewhat higher than I_{BS} and also than the collector current $I_C = I_{RC} + I_D > I_{CS}$ (Fig. 2.37d), and the transistor is certainly in the active region (I_{BS} and I_{CS} are the saturation currents of the transistor without the

diode). The waveform of the base current during the turn-on process is optimal (Figs. 2.37 and 2.33). Irrespective of the value of I_{B1} the transistor after t_r is close to the boundary between the active and the saturation region. This means that the turn-on may be established by a large base current

$$I_{B1} \gg \frac{V_{CC} - (V_{BE} - V_D)}{\beta R_C}, \quad (2.162)$$

and bearing in mind (2.138)

$$t_r \approx \tau_\alpha + (C_c + C_d) R_C I_{RC} / I_{B1}. \quad (2.163)$$

On the basis of (2.163) and (2.118) it follows that

$$R_B \ll \beta R_C \frac{V_{BB1} - V_{BE}}{V_{CC} - (V_{BE} - V_D)}. \quad (2.164)$$

If $V_{BB1} = V_{CC} \gg V_{BE}$, then $R_B \ll \beta R_C$. Usually, R_B and R_C are of the same order of magnitude, it is even possible that $R_B < R_C$.

After a negative step change of the input voltage at $t = t_1$, the base current becomes negative (Fig. 2.37c) and the transistor is turning off. The output voltage remains constant for some time until the collector current becomes equal to the current through R_C . During this time, the diode is conducting and

$$I_{B20} = I_{B2} + I_D = I_{B2} + \alpha(I_{B1} - I_{BS}), \quad (2.165)$$

where

$$I_{B2} \approx V_{BB2} / R_B. \quad (2.166)$$

Since the initial charge is $Q(0) = \tau_\beta I_B$, from the condition $Q(t_s) = \tau_\beta I_{BS}$ and on the basis of (2.114) the storage time is:

$$t_s = \tau_\beta \ln \frac{I_{B1} + I_{B2}}{\alpha I_{B1} + I_{B2} + I_{BS} / \beta + 1}. \quad (2.167)$$

The condition $I_{BS} / (1 + \beta) \ll \alpha I_{B1} + I_{B2}$ is always satisfied and

$$t_s = \tau_\beta \ln \frac{I_{B1} + I_{B2}}{\alpha I_{B1} + I_{B2}}. \quad (2.168)$$

Because $\alpha \approx 1$, $t_s \rightarrow 0$. If $V_{BB2} = 0$, then $I_{B2} = 0$ and:

$$t_s = \tau_\beta \ln 1 / \alpha = \tau_\beta \ln(1 + 1 / \beta) \approx \tau_\beta / \beta = \tau_\alpha. \quad (2.169)$$

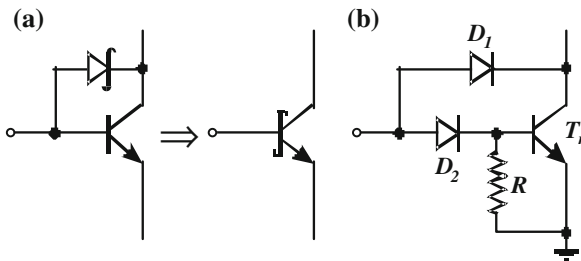


Fig. 2.38 Schottky transistor (a) and a nonsaturated switch comprising a silicon diode (b)

Therefore, although the transistor is in the active region, there exists a storage time but it is negligible.

After t_s , the diode is off and the fall-off time of the collector current is determined by (2.127) or (2.130) but C_c should be replaced by $C_c + C_d$.

The nonsaturated switches are most widely used in digital circuitry. A Schottky diode with a transistor makes a Schottky transistor (Fig. 2.38a). A common property of these circuits is high speed. However, the dissipation of the transistor is increased because while conducting it is in the active region, which is a weakness of this type of circuit.

If instead of a Schottky diode a silicon diode is used, it is necessary to use another diode (Fig. 2.38b). The collector junction here is not biased ($V_{BC} = -V_{D2} + V_{D1} \approx 0$) and the low level output voltage $V_{OL} = V_{BE}$ is increased. The resistor R reduces the base-emitter resistance when the transistor is off.

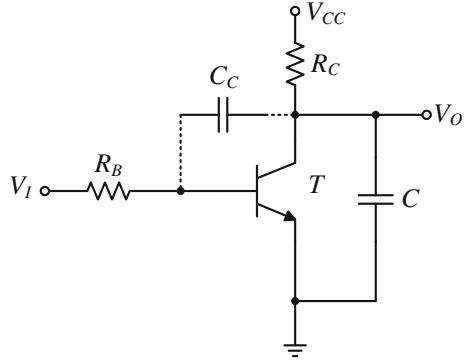
2.2.6 Capacitively Loaded Inverter

The output of an inverter is often loaded by a capacitor (Fig. 2.39). The influence of this capacitor on the transient mode is very noticeable. First of all, the transistor cannot go to saturation until this capacitor is discharged. The high level of the output voltage is not reached when the transistor is turned off, but when the capacitor is charged.

Let the drive be abrupt (Fig. 2.37b). Upon a positive voltage step at the input, the transistor turn-on process starts. Taking into account the collector junction capacitance, the collector current is

$$i_c(t) = \frac{V_{CC} - V_O}{R_C} - C \frac{dV_O}{dt} + C_c \frac{dV_{BC}}{dt} = \frac{\beta}{\tau_\beta} Q(t), \quad (2.170)$$

Fig. 2.39 Capacitively loaded inverter



where the charge $Q(t)$ in the base is determined by Eq. (2.109). If the variation of the voltage V_{BE} is neglected, then $dV_{BC}/dt = dV_O/dt$ and from (2.109) and (2.170) one obtains

$$\tau_\beta \tau \frac{d^2 V_O}{dt^2} + (\tau_{\beta e} + \tau) \frac{dV_O}{dt} + V_O = V_{CC} - \beta R_C I_{B1} \quad (2.171)$$

where

$$\tau = R_C(C_C + C), \quad (2.172)$$

and $\tau_{\beta e}$ is determined by (2.112). The solution of Eq. (2.171) can be written in the form

$$V_O(t) = A_1 e^{p_1 t} + A_2 e^{p_2 t} + V_{CC} - \beta R_C I_{B1}, \quad (2.173)$$

where p_1 and p_2 are the roots of the characteristic equation

$$p^2 + \frac{\tau_{\beta e} + \tau}{\tau_\beta \tau} p + \frac{1}{\tau_\beta \tau} = 0. \quad (2.174)$$

The constants A_1 and A_2 are determined from the initial conditions

$$V_O(0) = V_{CO} = V_{CC}; \quad (dV_O/dt)_{t=0} = 0,$$

thus

$$A_1 = \frac{p_2 \beta R_C I_{B1}}{p_2 - p_1}, \quad A_2 = \frac{p_1 \beta R_C I_{B1}}{p_1 - p_2}. \quad (2.175)$$

The rise time t_r in this case is determined from the condition that the collector junction is forward biased, i.e.,

$$V_{BC}(t_r) = V_{BE} - V_O(t_r) = V_{BC1},$$

that is

$$V_O(t_r) = V_{BE} - V_{BC1} = V_{CES}. \quad (2.176)$$

Equation (2.173) is transcendent and in general cannot be solved explicitly. If, however, the condition

$$x = 4\tau_\beta\tau / (\tau_{\beta e} + \tau)^2 \ll 1, \quad (2.177)$$

is fulfilled, then the roots of the characteristic equation are:

$$p_1 \approx \frac{\tau_{\beta e} + \tau}{\tau_\beta\tau}, \quad p_2 \approx \frac{1}{\tau_{\beta e} + \tau}. \quad (2.178)$$

Since the condition (2.177) applies, $|p_1| \gg |p_2|$ and the influence of the root p_1 can be neglected. Then, (2.173) reduces to

$$V_O(t) = V_{CC} - \beta I_{B1} R_C \left(1 - e^{-\frac{t}{\tau + \tau_{\beta e}}} \right), \quad (2.179)$$

and on the basis of (2.172) one obtains

$$t_r = \tau_{\beta c} \ln \frac{\beta I_{B1}}{\beta I_{B1} - (V_{CC} - V_{CES})/R_C} = \tau_{\beta c} \ln \frac{\beta I_{B1}}{\beta I_{B1} - I_{CS}}, \quad (2.180)$$

where

$$\tau_{\beta c} = \tau_{\beta e} + \tau = \tau_\beta + (\beta + 1) C_c R_C + C R_C. \quad (2.181)$$

By comparing (2.180) and (2.121) it may be noticed that the influence of the capacitance C reduces to the increase of the time constant by $C R_C$. Of course, this conclusion is correct only if condition (2.177) applies. The left-hand side in (2.177) is maximal for $\tau = \tau_{\beta e}$, amounting

$$x_{\max} = \frac{\tau_{\beta e}}{\tau_\beta + \beta C_c R_C}. \quad (2.182)$$

Thus, $x_{\max} < 1$ meaning that (2.180) applies for a wide range of C values. The maximum error is around the capacitance value

$$C = \tau_\beta / R_c + (\beta - 1) C_c \quad (2.183)$$

which is obtained for $\tau = \tau_{\beta e}$.

The capacitor C does not have any influence on the storage time t_s , because in that interval $V_o = V_{CES} = \text{const.}$ During t_f Eq. (2.171) applies but I_{B1} should be replaced by $I_{B2} = V_{BB2}/R_B$. It can be shown that if (2.177) applies

$$V_O(t) \approx V_{CC} + \beta R_c I_{B2} - R_c (I_{CS} + \beta I_{B2}) e^{-t/\tau_{\beta e}}. \quad (2.184)$$

Charging of the capacitor ends when $V_O = V_{CC}$ and from (2.179) one obtains:

$$t_f \approx [\tau_\beta + (\beta + 1) C_c R_c + CR_c] \ln(1 + I_{BS}/I_{B2}). \quad (2.185)$$

If $V_{BB2} = 0$, i.e. $I_{B2} = 0$, then t_f is determined from the condition $V_O = 0.9V_{CC}$, and

$$t_f \approx 2.3 \cdot [\tau_\beta + (\beta + 1) C_c R_c + CR_c]. \quad (2.186)$$

By comparing t_r and t_f of the inverter with and without a capacitor, it may be concluded that the influence of C reduces to increasing the time constant of the transistor. It should be emphasized that (2.185) and (2.186) are approximate since it is possible that the transistor is off ($i_c = 0$) before the capacitor is charged. Then t_f consists of two intervals: the first t_1 ending at $i_c(t_f) = 0$ and the second when C is being charged through the resistor R_c .

In practice it is often

$$CR_c \gg \tau_\beta + (\beta + 1) C_c R_c. \quad (2.187)$$

In such a case, the transistor can be considered an ideal switch. During the turn-on process the operating point will instantaneously move from the position A to the position B (Fig. 2.40a). The transistor is in the active region and the collector current is $I_C = \beta I_{B1}$ (Fig. 2.40b). The fall time of the collector voltage t_r is determined by (2.180) where, in view of (2.187), $\tau_{\beta c} \approx CR_c$.

For a negative input voltage step the transistor is instantaneously turned off ($i_c = 0$ Fig. 2.40b). The capacitor C charges through R_c and

$$t_f \approx 3R_c C. \quad (2.188)$$

For fast switching circuits, this time is unacceptably large. For this reason, more complex inverters, having lower output resistance when the output voltage is high, are used.

Two versions of such circuits are most frequently used (Fig. 2.41). In the circuit of Fig. 2.41a when T_{r1} is off, T_{r2} is on in the active region. The output resistance is $R_{OH} = R_c/(1 + \beta_2)$ and the rise time of the output voltage is

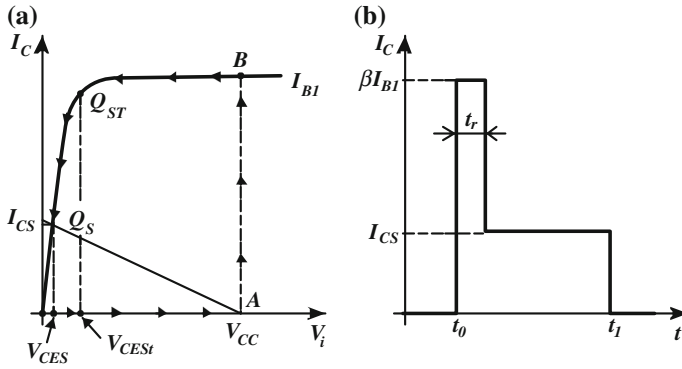


Fig. 2.40 Path of the operating point (a) and change of collector current when $CR_C \gg \tau_\beta + (\beta + 1)C_c R_C$ (b)

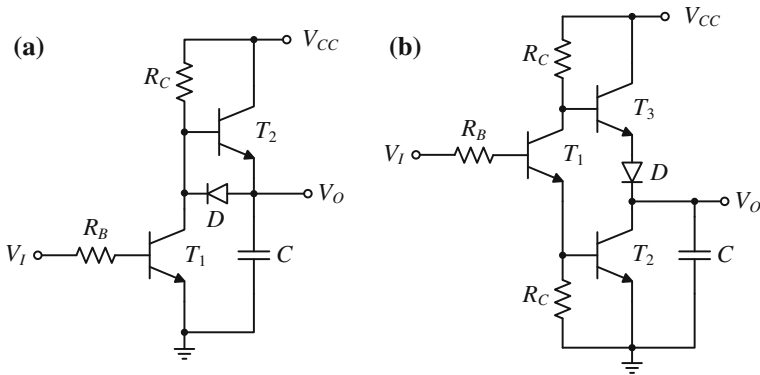


Fig. 2.41 Inverters with low output resistance in both static states

$$t_f \approx 3CR_C/(\beta_2 + 1). \quad (2.189)$$

The shortcoming of this circuit is that the low level of the output voltage is increased. Namely, when T_{r1} is in saturation, the diode D is conducting, T_{r2} is off and

$$V_{OL} = V_D + V_{CES1}. \quad (2.190)$$

For this reason, the more complex inverter of Fig. 2.41b is more frequently used. While T_{r1} and T_{r2} are in saturation, T_{r3} is off. The only purpose of the diode D here is that I_{r3} is to be off while T_{r1} and T_{r2} are conducting. If T_{r1} and T_{r2} are off, T_{r3} is in the active region and the output resistance is $R_{OH} \approx R_C/(1 + \beta_3)$, and the charging time of the capacitor is determined by (2.189).

2.2.7 Inductively Loaded Switch

In practice, the switch is sometimes inductively loaded. Typical examples of such loads are electromagnetic relays, motors, and various types of pulse circuits having transformer coupling. Figure 2.42a shows an inverter having an inductive load. Most often the collector winding is inductively coupled with a secondary winding driving a load whose resistance referred to the primary is denoted by R_0 . The peculiarity of an inductive load is that for fast variations (high frequencies) it behaves like a large resistance and in the quasi-stationary states it accumulates the electromagnetic energy which may exert a considerable influence upon the converter characteristics. The collector current i_c is determined by (2.119). For the circuit of Fig. 2.42a, it is

$$i_c(t) = \frac{V_{CC} - V_O}{R_0} + \frac{1}{L} \int_0^t (V_{CC} - V_O) dt. \quad (2.191)$$

Upon differentiation of (2.191) one obtains a differential equation whose solution, with initial condition $V_O(0) = V_{CC}$, is

$$V_O(t) = V_{CC} - \frac{\tau}{\tau - \tau_{\beta e}} \beta I_{B1} R_0 (e^{-t/\tau} - e^{-t/\tau_{\beta e}}), \quad (2.192)$$

where

$$\tau = L/R_0. \quad (2.193)$$

The time t_r required by the transistor to go to saturation is determined from condition (2.176). Equation (2.192), however, is transcendent and in general can

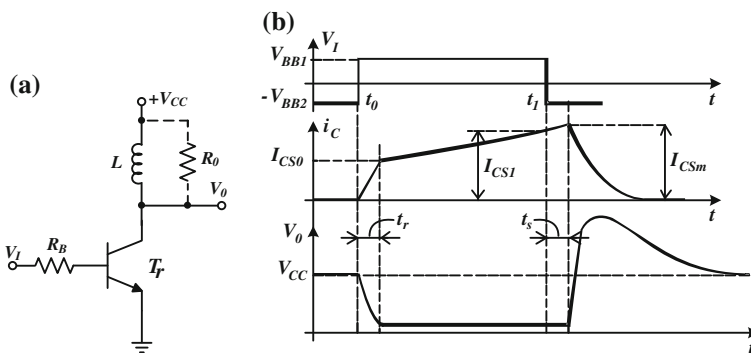


Fig. 2.42 Inverter having an inductive load (a) and the responses of collector current and voltage to a pulse drive (b)

not be solved explicitly. On the other hand, usually $\tau \gg \tau_{\beta e}$, i.e. $t_r \ll \tau$. Then $\exp(-t/\tau) \approx 1$ and

$$V_O(t) \approx V_{CC} - \beta I_{B1} R_0 (1 - e^{-t/\tau_{\beta e}}). \quad (2.194)$$

Now, from (2.176) and (2.194) it follows that

$$t_r \approx \tau_{\beta e} \ln \frac{\beta I_{B1}}{\beta I_{B1} - I_{CSO}}, \quad (2.195)$$

where

$$I_{CSO} = \frac{V_{CC} - V_{CES}}{R_0}. \quad (2.196)$$

Therefore, t_r is the same as if the collector load were $R_C = R_0$. This is due to the fact that the resistivity of the winding during t_r is very high and its influence can be neglected.

However, the situation $\tau \ll \tau_{\beta e}$ is possible. This occurs when the resistance R_0 is very high ($R_0 \rightarrow \infty$) as in the case of electromagnetic relays. Then $t_r \ll \tau_{\beta}$, and $\exp(-t/\tau) \approx 1$ so

$$V_O(t) \approx V_{CC} - \frac{\beta I_{B1} L}{\tau_{\beta}} (1 - e^{-t/\tau}). \quad (2.197)$$

By taking $\ln(1 - x) \approx -x$ for $x \ll 1$, from (2.195) it is approximately

$$t_r \approx \tau_{\beta} \frac{V_{CC}}{\beta I_{B1} R_0} = \tau_{\alpha} \frac{V_{CC}}{I_{B1} R_0}. \quad (2.198)$$

Therefore, if $R_0 \rightarrow \infty$, then $t \rightarrow 0$. This means that a transistor loaded by an electromagnetic relay is practically turned on instantly.

After t_r the transistor is in saturation. The voltage across the winding $V_{CC} - V_{CES}$ is constant and the winding current will increase linearly. The collector current (Fig. 2.42b) is

$$i_c(t) = I_{CSO} + \frac{V_{CC} - V_{CES}}{L} t. \quad (2.199)$$

During the time interval $t_1 - t_0 = T_1$, the transient regime in the winding does not have to be completed. More frequent is the other case (Fig. 2.42b). Then the

resistance R_B is determined from the condition that for $t = T_1$ the transistor is weakly saturated, i.e.

$$I_{B1} = \frac{V_{BB1} - V_{BES}}{R_B} \geq \frac{1}{\beta} I_{CS1} = \frac{1}{\beta} \left[I_{CS0} + \frac{V_{CC} - V_{CES}}{L} T_1 \right], \quad (2.200)$$

giving

$$R_B \leq \beta \frac{V_{BB1} - V_{BES}}{\frac{V_{CC} - V_{CES}}{R_0} + \frac{V_{CC} - V_{CES}}{L} T_1}. \quad (2.201)$$

At an instant $t = t_1$, when the input voltage becomes negative, the output voltage remains constant while the excess charge piled up in the base is cleared. This is the storage time t_s , during which the collector current increases according to (2.199). Since the base charge is controlled by the base current, the change of $Q(t)$ is as for the inverter loaded by R_C . Therefore, the time t_s is determined by (2.125) and

$$I_{BS} = \frac{I_{CSm}}{\beta} = \frac{1}{\beta} i_c (T_1 + t_s). \quad (2.202)$$

Usually $t_s \ll T_1$ and the maximum collector current is

$$I_{CSm} = I_{CS0} + \frac{V_{CC} - V_{CES}}{L} (T_1 + t_s) \approx I_{CS0} + \frac{V_{CC} - V_{CES}}{L} T_1. \quad (2.203)$$

This current must be lower than the maximum permitted collector current ($I_{CSm} < I_{CD}$), resulting in the condition

$$L > \frac{V_{CC} - V_{CES}}{I_{CD} - I_{CS0}} T_1. \quad (2.204)$$

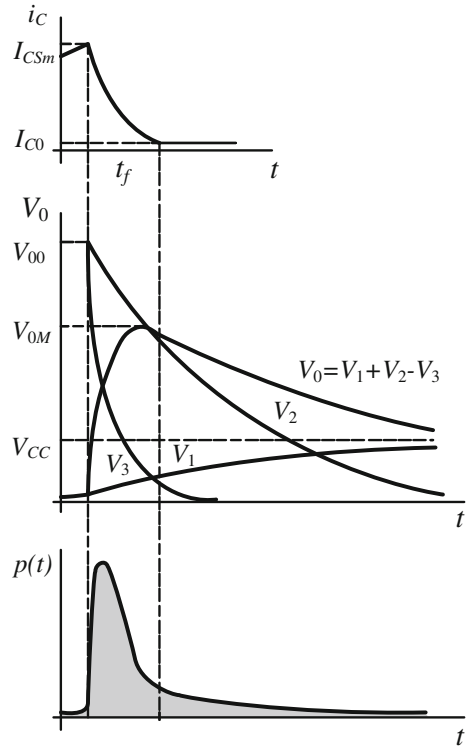
After t_s expires, the collector current decreases and is determined by (2.126). By introducing (2.126) in (2.191), differentiating the obtained equation and solving it for V_o , and using the initial condition $V_o(0) = V_{CES} \approx 0$, one obtains

$$V_o(t) = V_{CC}(1 - e^{-t/\tau}) + \frac{R_0(I_{CSm} + \beta I_{B2})}{\tau - \tau_{\beta e}} \tau (e^{-t/\tau} - e^{-t/\tau_{\beta e}}). \quad (2.205)$$

If the factor in front of the second bracket is denoted by V_{O0} , then (2.205) can be written as:

$$v_o(t) = V_{CC}(1 - e^{-t/\tau}) + V_{O0} e^{-t/\tau} - V_{O0} e^{-t/\tau_{\beta e}} = v_1 + v_2 - v_3. \quad (2.206)$$

Fig. 2.43 Collector current, output voltage V_o , and power of dissipation P during the turn-off process of transistor



The dependence (2.206) for $\tau \gg \tau_{\beta e}$ is shown in Fig. 2.43 and the following conclusions may be drawn. The output voltage increases faster than the collector current decreases. During the fall time t_f , given by (2.127), a situation when $V_o \gg V_{CC}$ is possible. The maximum output voltage is approximately

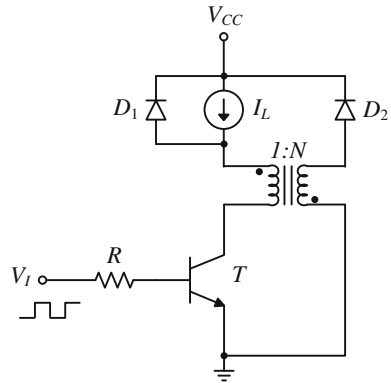
$$V_{OM} \approx V_{CC} + R_0(V_{CC} T_1/L + \beta I_{B2}). \quad (2.207)$$

Owing to this the dissipation of the transistor $P(t) = i_c(t)V_o(t)$ is rather high (Fig. 2.43).

Example 2.4 For the circuit of Fig. 2.44

- Explain how the accumulated electromagnetic energy returns to the source
- Determine the maximum inverse voltage that appears at the diode D_2 .
- Determine the time of core transformer demagnetization t_x assuming that all the energy accumulated in the magnetization inductance returns to the source.
- Show the waveforms of the voltage on the transistor collector, the voltage on the secondary winding and the current through that winding using PSPICE software package.

Fig. 2.44 Switch with bipolar transistor and inductive load at which the accumulated electromagnetic energy returns to the source



The circuit of Fig. 2.44 has $V_{CC} = 80$ V, $N = 5$, $I_L = 5$ A, $L_m = 100$ μ H, $f = 10$ kHz and $D = 0.5$

- During the turning off process of the transistor T, a negative change of current occurs through the magnetizing inductance what induces a corresponding voltage. This voltage is transferred to the secondary side in the ratio 1:N, and in dependence on how transformer is wound, it provides direct polarization of the diode D_2 . If we ignore the voltage drop on the diode while it conducts, during the period the diode D_2 conducts the secondary winding voltage is V_{CC} . This voltage transferred to the primary side is V_{CC}/N , so the maximum voltage at the collector of the transistor is equal to $V_{CC}(1 + 1/N)$.
- The maximum inverse voltage on a diode is reached when the transistor is on. In this case the voltage on the anode is equal to $-NV_{CC}$, and the maximum inverse voltage on the diode is
-

$$\frac{1}{2} L_m I_L^2 = V_{CC} \frac{I_L t_x}{N} \Rightarrow t_x = \frac{N I_L L_m}{V_{CC}} = 31.25 \mu\text{s}.$$

- See Fig. 2.45.

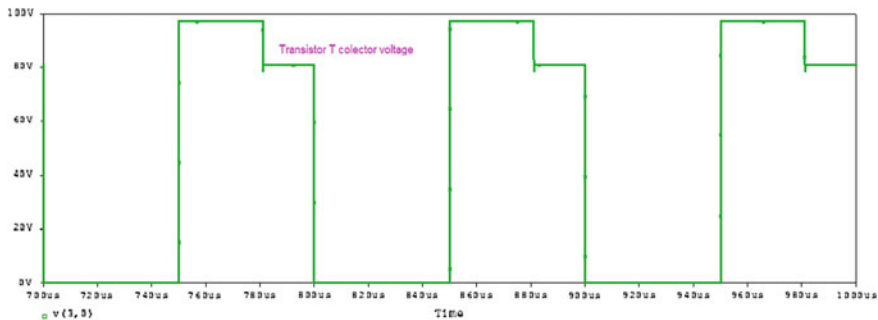


Fig. 2.45 Waveform of voltage on the transistor collector

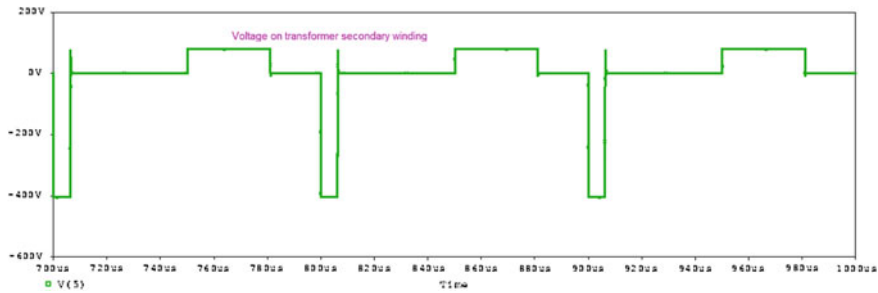


Fig. 2.46 Waveform of voltage on transformer secondary winding

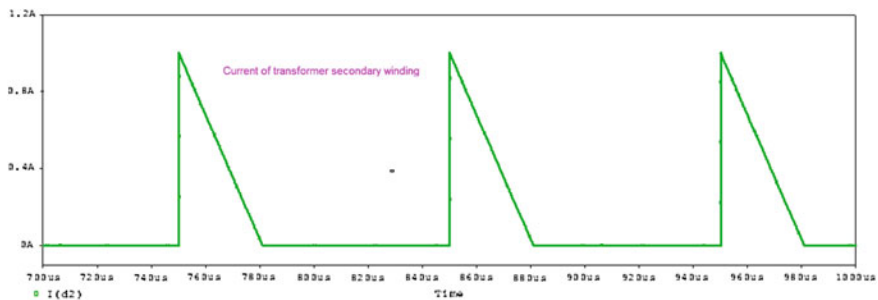


Fig. 2.47 Waveform of current through transformer secondary winding

$$V_{D,inv} = V_{CC} - (-NV_{CC}) = (1 + N)V_{CC} = 480 \text{ V}.$$

Assuming that all accumulated energy in the magnetizing inductance returns to the source, the following expression can be written (Figs. 2.46 and 2.47)

2.2.7.1 Transistor Protection

The voltage V_{OM} must be lower than the collector-base breakdown voltage

$$V_{OM} < BV_{CBO}. \quad (2.208)$$

Otherwise, the transistor must be protected. The switching circuits in relays and in blocking generators are protected by adding a diode (Fig. 2.48a). When $V_o > V_{CC} + V_{Dt}$, the diode is conducting and it limits the output voltage (Fig. 2.48b). The use of a Schottky diode is recommendable. The collector current (Fig. 2.48b) increases exponentially because the resistance of the winding, r_L , cannot be neglected.

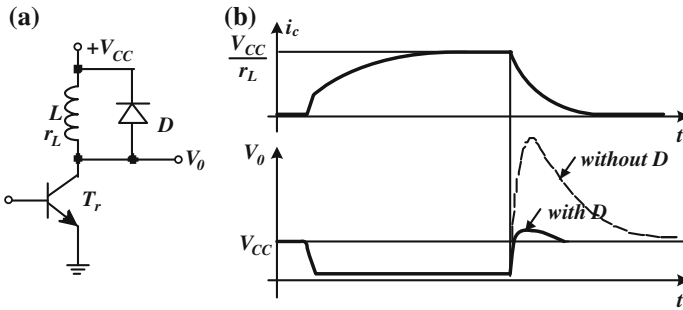


Fig. 2.48 Protection of transistor (a) and pulse waveforms of the collector current and output voltage when a relay is the load (b)

The increased dissipation during the turn-off process of the transistor is another problem. The dynamic losses are exactly then at the maximum. In order to reduce them, the increase of the collector voltage should be slowed down until the current falls to zero. This is accomplished by using the so called dv/dt or snubber circuits (Fig. 2.49a). These circuits are often referred to as the circuits for shaping the transistor load line or the transistor turn-off protection circuits. An efficient snubber circuit should: limit the maximum collector voltage below the breakdown voltage, slow down the output voltage ascent until collector current falls and ensure that the total losses in the transistor and the dv/dt circuit are minimal. All this, to a good degree, is provided by the DRC dv/dt circuit (Fig. 2.49a). During the turn-off process the diode is conducting and the capacitor C is charged, thus slowing down the rate of ascent of the output voltage. An accurate analysis would be quite complicated. Therefore only the approximate relations satisfactory for practical

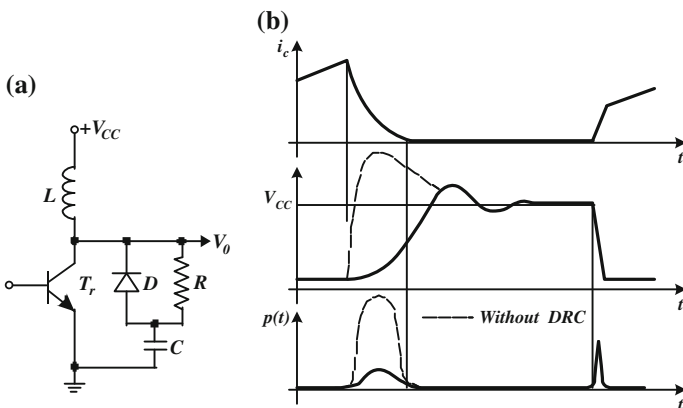


Fig. 2.49 Protection DRC circuit during transistor turn-off process (a) and the corresponding pulse waveforms (b)

calculations are given here. The accumulated electromagnetic energy is transferred to the capacitor, so it can be written that

$$\frac{1}{2} L I_{LM}^2 = \frac{1}{2} C V_{OM}^2, \quad (2.209)$$

where $I_{LM} = I_{CSM}$ is the maximum current of the winding. From (2.209) and (2.199) it follows that the maximum output voltage is

$$V_{OM} = V_{CC} \frac{\tau + T_1}{\sqrt{LC}}. \quad (2.210)$$

where $\tau = L/R_o$. On the other hand, if t_r and t_f are the maximum rise time of the output voltage and the maximum fall time of the collector current, respectively, then it can be written that

$$\frac{1}{2} C V_{OM}^2 = \frac{I_{CSM} V_{OM} (t_r + t_f)}{2}. \quad (2.211)$$

On the basis of (2.211) and (2.209) the capacitance is approximately

$$C = (t_r + t_f)^2 / L. \quad (2.212)$$

In practice the values of the capacitance C are between several nF and several hundreds nF . When the transistor is on, the diode is off and the capacitor discharges through the resistor R . If the discharge time is taken to be $3RC$, then it has to be:

Fig. 2.50 Turn-on protection circuit at a switch with bipolar transistor

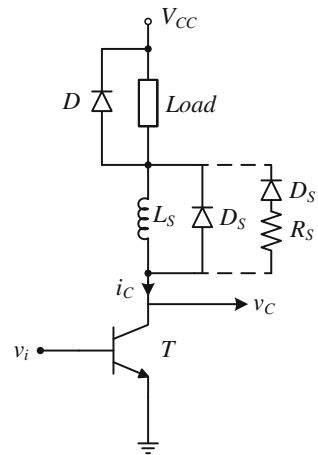
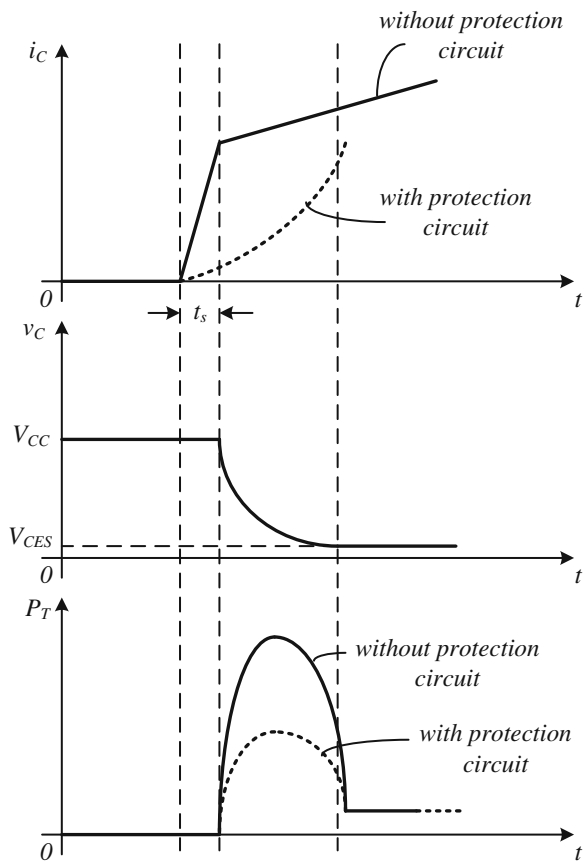


Fig. 2.51 Waveforms of the collector current, the collector voltage and power dissipation on bipolar transistor during the switch turn on process without turn on protection circuits and with a turn on protection circuit



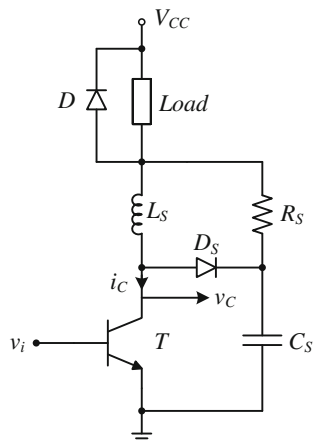
$$R \leq \frac{T_{1min}}{3C}, \quad (2.213)$$

where T_{1min} is the minimum conduction time of the transistor.

Besides the turn-off, there is the turn-on protection circuit (Fig. 2.50). The aim of this protective circuit is to reduce the speed of increase of the collector current and thus to reduce the dissipation on the transistor when the switch is turning on (Fig. 2.51). This protection circuit consists of the inductance L_S connected in the collector circuit of the switching transistor and the diode D_S connected in anti-parallel with the inductance L_S .

Due to a rather large time constant $\tau = L_S/r_S$ (r_S —series connection of the diode resistance in on state and the resistance of the inductor L_S), the resistance R_S can be connected in series with the diode D_S . The goal is to increase the time constant, so the inductor can ensure the use of accumulated energy in the time interval when the transistor T is turned off. In this case it is necessary to take into account the maximum collector voltage of the transistor, because the discharge current of the

Fig. 2.52 Combined protection circuit of switch with bipolar transistor



inductance L_S generates voltage on the resistor R_S which increases the total voltage on the collector of the transistor.

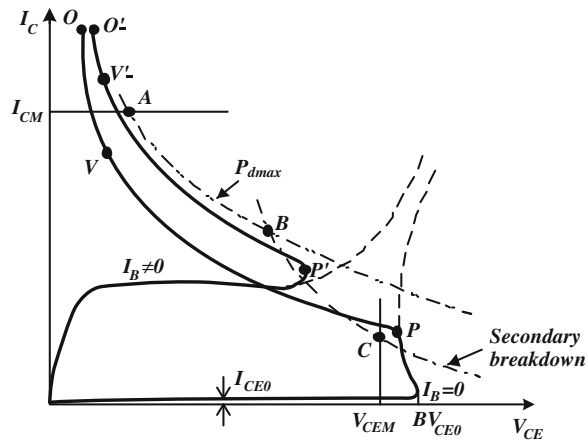
There is also a combined protection circuit that reduces losses in the bipolar transistor when the switch is turning on and turning off (Fig. 2.52). The function of the turn-on protection circuits is assumed by the inductance L_S , the diode D_S and the resistor R_S . On the other hand, the role of the turn-off protective circuits is played by the capacitance C_S , the diode D_S and the resistor R_S . These elements ensure a protective function in the same manner as already described for the turn-on and turn-off protection circuits.

2.2.8 Transistor Selection

The key element in the pulse converters and voltage stabilizers is the switching transistor. As a rule, it is in a heavy duty operating mode (high current while on, high voltage while off, and significant voltages and currents during transients). For this reason considerable attention should be paid to the design of the optimum driving and dv/dt circuits and to the selection of the transistor. If the transistor is to operate reliably, its limitations must be strictly taken into consideration. This primarily concerns the limitations as regards the voltage, current, and dissipation.

The maximum voltage is limited by the breakdown voltages BV_{CB0} and BV_{CE0} (Sect. 2.2.1.1). In power transistors a secondary breakdown may appear. It manifests itself by an abrupt decrease of the collector–emitter voltage accompanied by a simultaneous increase of the collector current (Fig. 2.53). It occurs when both the voltage and the current are large simultaneously. The secondary breakdown starts when the current concentrates to a small area of the junction which leads to a considerable rise in temperature, creating a so called “hot spot”. This gives rise to

Fig. 2.53 Output characteristics of a power transistor in the region of secondary breakdown



the thermal regenerative process which is a characteristic of power transistors. However, in addition to the thermal instability at high collector currents, an electrical instability appears there, which creates the conditions for avalanche injection of majority carriers at the collector junction. This is particularly marked in the high voltage switching transistors having a lightly doped collector region. The ionic electric field appears exactly at the surface between the light doped regions and causes the avalanche injection of the charge carriers. In order to eliminate as much as possible the mechanisms leading to thermal and electrical instabilities, efforts are being made to eliminate any crystal defects, metallic impurities, interstitials, etc. In addition, a maximally efficient heat removal should be ensured. Figure 2.53 shows the transistor output characteristics for $I_B = 0$ and $I_B \neq 0$.

In Fig. 2.53 the characteristics are extended by dotted lines in order to show what they would be like if there were no secondary breakdown which appears at the points P and P' . Between the points V and O and V' and O' the collector-emitter resistance is very low. If the transistor were then switched off, it would return to the original characteristics without a visible damage. If, however, the current is not limited and the operating point reaches the position O or O' , the junction temperature may reach the melting point causing failure and permanent damage to the transistor. Figure 2.53 also shows the limitations: the maximum current I_{CM} , the maximum voltage V_{CEM} ($V_{CEM} < BV_{CE0}$), the maximum dissipation, and the hyperbola limiting the appearance of the secondary breakdown. They all make the region of reliable operation of the transistor as represented by the surface $V_{CEM}-C-B-A-I_{CM}$. Therefore, at high V_{CE} the limitation is the breakdown voltage, at low V_{CE} the limitation is the maximum current, and between the points A and B the limitation is the maximum dissipation.

The maximum permitted dissipation is determined by the maximum junction temperature which is for silicon transistors between 170 and 200 °C. Namely, the power $P = V_{CE}I_C$ generated in the transistor is converted to heat. For this reason the

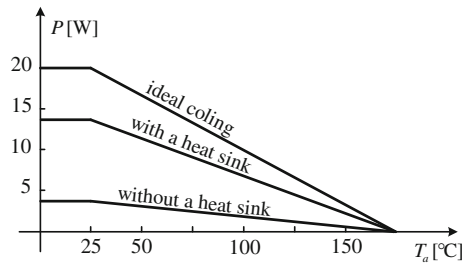


Fig. 2.54 An illustration of the dependence of the permitted power on temperature for different thermal resistances

temperature of the crystal is always higher than that of the environment. At excessive temperatures the transistor will either be suddenly destroyed or its characteristics will degrade gradually.

The heat developed in the transistor is transferred through the case and the heat sink to the environment. In steady state:

$$P_d = VI = \frac{T_j - T_a}{R_{jc} + R_{ca}}, \quad (2.214)$$

where T_j and T_a are the temperatures of the junction and ambient temperature, respectively. R_{jc} is often called the internal thermal resistance. It is constant and ranges from several tenths of $^{\circ}\text{C}/\text{W}$ for low power transistors up to several tens of $^{\circ}\text{C}/\text{W}$ for high power transistors. The external thermal resistance depends upon the means of heat transfer from the case to the environment. It is highest when the case is free in the air. The heat transfer can be considerably improved by means of heat sinks. In principle, heat sink is a metal surface on which the transistor is mounted. In this way R_{ca} is considerably decreased. Good dimensioning and mounting of a heat sink are very important, particularly if the dissipation is high. As a rule, as soon as the power generated in a transistor exceeds 100 mW, an adequate heat sink should be used.

Manufacturers often give diagrams showing the dependence of the maximum permitted power on ambient temperature for different values of R_{ca} . A typical example of such a diagram is shown in Fig. 2.54. Ideal cooling is obtained when the external thermal resistance is zero ($R_{ca} = 0$) and the case temperature is equal to the ambient temperature ($T_c = T_a$). Such cooling is possible if the transistor is for example immersed in oil. At low temperatures up to 25 $^{\circ}\text{C}$ the permitted power is constant.

Manufacturers give the Safe Operating Area (SOA) for a given ambient temperature. SOA respects all the limitations mentioned previously. It is different for DC and pulse operating modes (Fig. 2.55a). The narrower the pulse, the wider the area of reliable operation.

Manufacturers often give SOA separately when the device is conducting (Fig. 2.55a) and also when it is off (Fig. 2.55b).

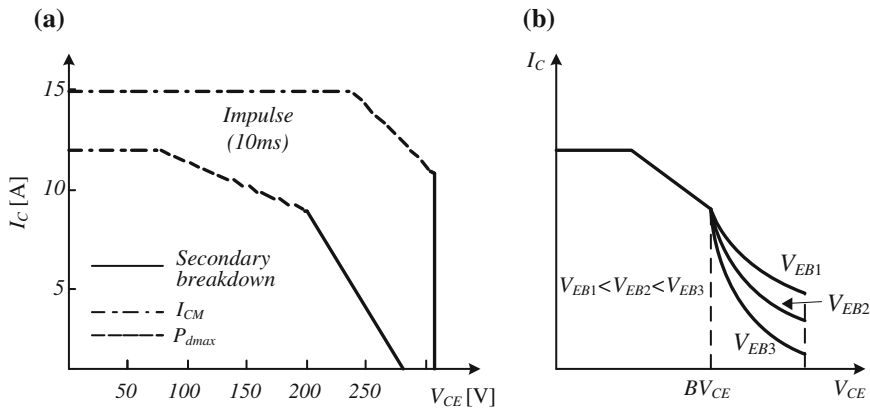


Fig. 2.55 Safe Operating Area at forward bias (a) and reverse bias of the emitter p-n junction (b)

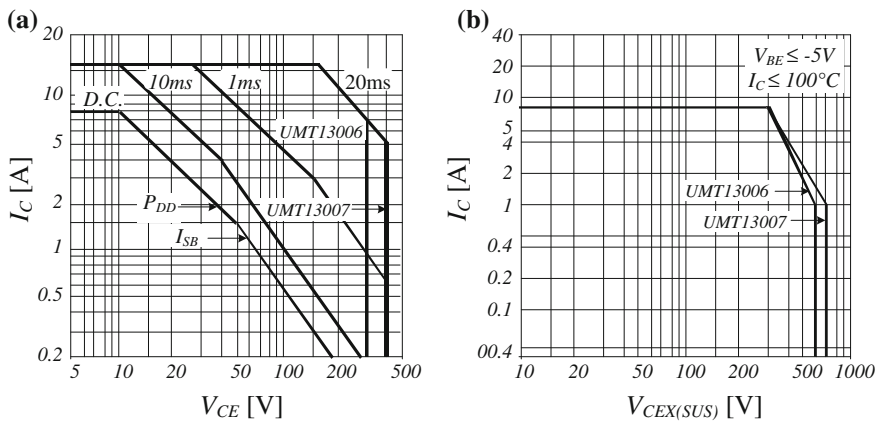


Fig. 2.56 SOA of switching transistors UMT 13006 and 13007 manufactured by UNITRODE, when on (a) and when off (b)

The region of operation at reverse bias is extended because the collector current is then very low and the breakdown voltage is higher. This region is often called the Reverse-Bias Safe Operating Area (RBSOA). Figure 2.56 shows SOA and RBSOA of the power transistors UMT 13006 and UMT 13007.

The dependencies of the current gain and saturation voltage on the collector current (Fig. 2.57) are very important for the selection of a good transistor. They are important since here β is lower and V_{CES} is higher than the corresponding parameters of low power transistors (below 1 W). The maximum frequency of the switching transistors depends on the turn-on and turn-off times. These characteristics too are usually given as functions of the collector current (Fig. 2.58) for a specified test circuit. The curves in Fig. 2.55 are given for an inverter comprising resistors $R_B = 5 \text{ V}/I_B$ and $R_C = 125 \text{ V}/I_C$ for $I_C/I_B = 5$ (Fig. 2.56).

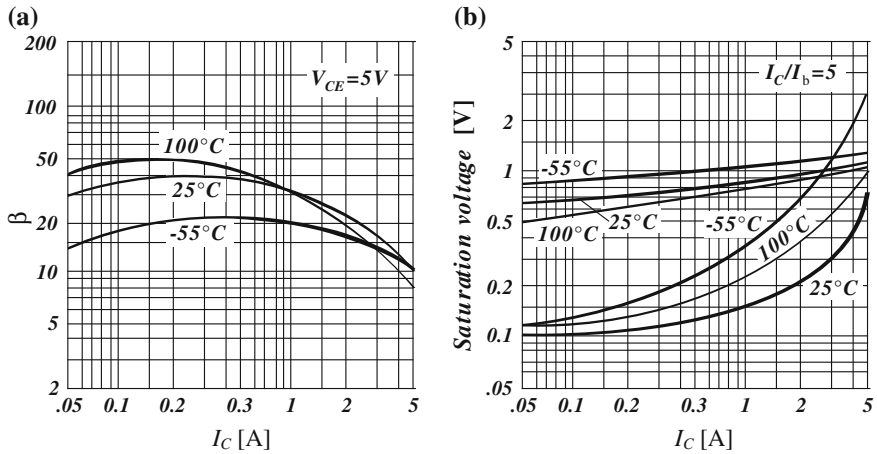


Fig. 2.57 Current gain β (a) and saturation voltages V_{BES} and V_{CES} (b) as functions of collector current for power transistors UMT 13006 and UMT 13007

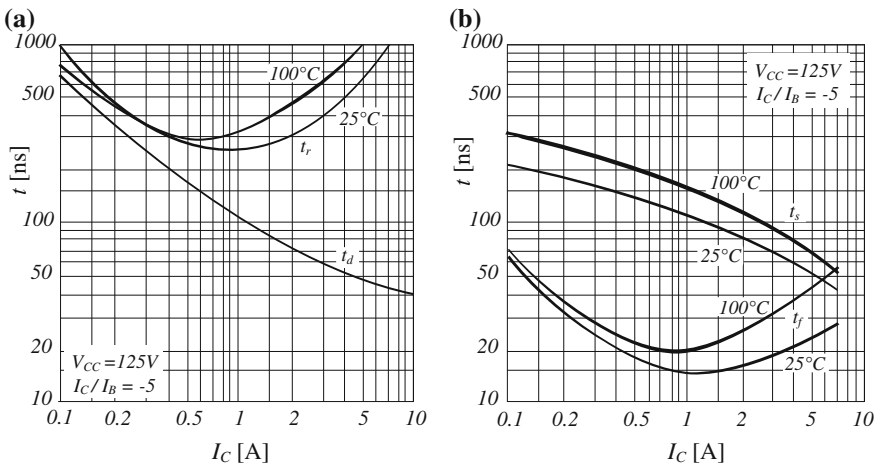


Fig. 2.58 The transient times at turn-on (a) and turn-off (b) as functions of collector current for transistors UMT 13006 and UMT 13007 for a pulse drive by $V_{BB1} = +6V$ and $V_{BB2} = -4V$

The minimum cycle of the control pulses of a switching transistor should be five to ten times longer than the sum of the turn-on and the turn-off times, i.e. $T_{min} = (5-10)(t_d + t_r + t_s + t_f)$.

For an optimum use of a power transistor the snubber and driving circuits should be designed very carefully. An optimum driving circuit should have the following properties:

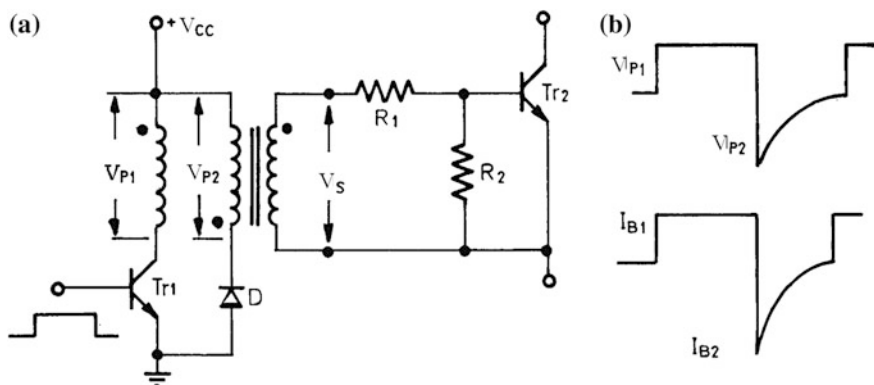


Fig. 2.59 Transformer driving circuit (a) and pulse waveforms of voltage V_{P1} and base current (b)

- The driving current should be sufficiently high to render dynamic losses as low as possible. Upon turn-on of the transistor, the driving circuit should provide the control of the degree of saturation.
- In order to render the falloff time of the collector current as short as possible and to minimize dynamic losses, turning off of the transistor should be “forced” by a large negative current. In doing so, care should be taken that the emitter clearance does not occur. It is desirable that the emitter junction is reverse biased while the transistor is off. If this is not possible, then the emitter-base resistance should be low so that the collector current is approximately I_{CO} and the breakdown voltage is maximal.
- The consumption of the driving circuit should be as low as possible.
- The circuit should be as simple as possible.

Usually the optimum drive is accomplished by a speed up capacitor. Its capacitance is determined by the criterion of the minimum duration of the transient mode (Sect. 2.2.4). Very often, for very powerful converters the power and the control parts are galvanically separated by a transformer coupling in the driving circuit. In that case the role of the speed up capacitor may be taken over by the third winding (Fig. 2.59a).

During the turn-off process of the transistor Tr_1 , the previously accumulated energy in the transformer primary is returned to the power source V_{CC} via the third winding. Since this winding is wound up in the opposite direction compared to the other two, a negative voltage is induced in the secondary and it provides a negative base current of the power transistor Tr_2 which is quickly turned off. The resistance R_1 is determined from the condition that at the end of the interval of conduction the transistor Tr_2 is in weak saturation. Tr_2 is actively cut off by the resistor R_2 . Typically, its value is from 50 to 100 Ω .

2.2.9 Driver Circuits

In order to improve the dynamic characteristics of the switch adequate excitation and driver circuits are used. The Baker clamp circuit is shown in Fig. 2.60. This circuit not only ensures better dynamic characteristics but also when the transistor is in off state, causes that both of the p-n junctions are reversely biased. The diode D_2 and D_1 provide the collector p-n junction voltage around 0 V.

The transistor does not enter saturation, but works instead in the active region close to the saturation region, so that it has a shorter turn off time for the same excitation ($t_S = 0$). When the input voltage is negative, the base is not broken, but the diode D_3 provides a negative polarization of the emitter p-n junction.

A Totem pole drive is shown in Figure 2.61. The dynamic characteristics of the switch are significantly improved by such a circuit. In this driver circuit using a speed up capacitor and a complementary pair of transistors T_2 and T_3 an

Fig. 2.60 Baker clamp circuit

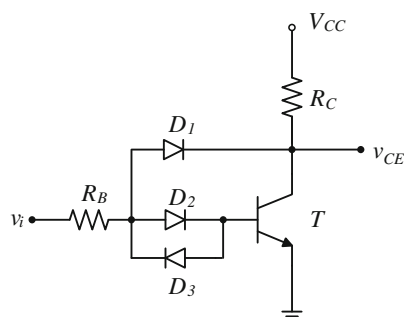
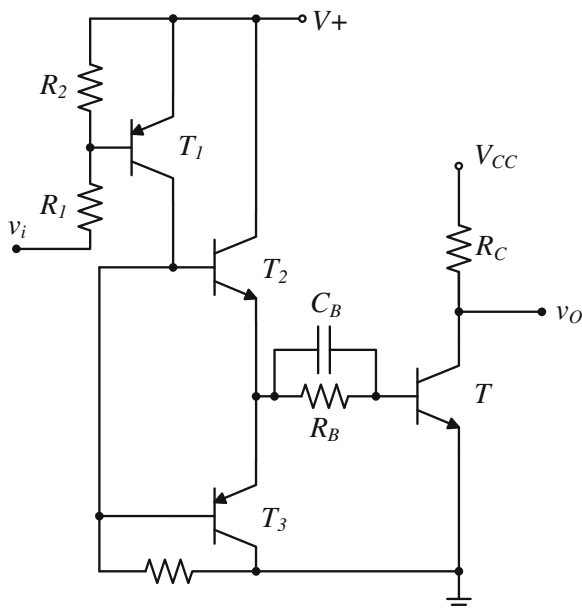


Fig. 2.61 Totem pole driver



approximately $\beta + 1$ times higher base current is obtained during the transistor transition processes compared to the case when only a speed up capacitor is used. The circuit works as follows. When the input v_i is low, the transistor T_1 leads and its collector current excites the transistor T_2 . The transistor T_2 provides the base current through the speed up capacitor which turns on the transistor T .

When the transistor T turns off the input v_i is high, and the transistor T_1 is turned off, as well as the transistor T_2 . The voltage on the speed up capacitor C_B provides direct polarization of the transistor T_3 and ensures the flow of the base current of the transistor T , which turns it off.

2.3 Power MOS Transistor as Switch

MOS transistors are increasingly replacing bipolar transistors in the pulse power supplies. A significant advantage of a MOS power transistor over a bipolar one is in that their input resistance is very high (of the order of 10^8 – $10^9 \Omega$) so that the input currents are of the order of nA. Thanks to this the consumption of the driving circuit is negligible, since for control purposes it is necessary to provide only the corresponding gate—source voltage. For this reason these transistors are called the voltage controlled components. Since the MOS transistors are unipolar, they do not incorporate the effect of storage of minority charge carriers, and consequently there is no storage time in the turn-off process. The duration of the transient mode is almost one order of magnitude shorter compared to that of the bipolar transistors. Thanks to this, the operating frequency is increased from several tens of kHz for bipolar transistors to hundreds (100–200) kHz for MOS transistors. The drain current is characterized by a negative temperature coefficient, so the MOS transistors are thermally very stable. Therefore, the conditions for the appearance of the secondary breakdown are reduced to minimum. The main shortcoming of the MOS transistors is a higher on-resistance and therefore a higher quasi-stationary dissipation. Table 2.2 presents the comparative characteristics of the bipolar and MOS power transistors.

Owing to large voltages and currents in the operating modes of power transistors there exist significant peculiarities in the manufacturing technology of the conventional MOS transistors. Fortunately, the static V-I characteristics are of nearly of the same form for all of them:

$$I_D = \beta_n f(V_{gs}, V_{ds}), \quad (2.215)$$

where $f(V_{gs}, V_{ds})$ is the function of the bias voltages depending upon the position of the operating point, and

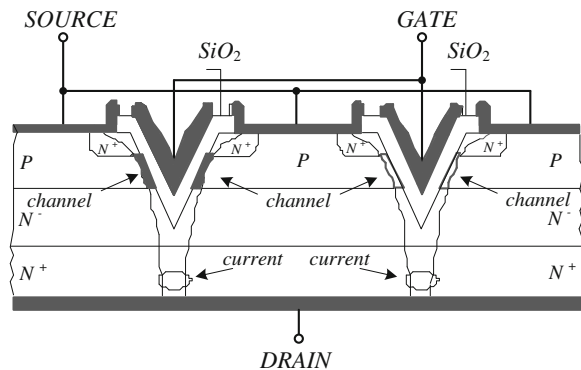
Table 2.2 Comparative characteristics of the power bipolar and MOS transistors

Parameter	Bipolar	MOS
Input resistance	Low	High (of the order $10^9 \Omega$)
Drive	Current controlled	Voltage controlled
Gain	100–2000	Not defined
Turn-on time	(50–500) ns	(10–200) ns
Turn-off time	(500–2000) ns	(10–600) ns
Charge carriers	Minority	Majority
Storage time	(1–5) μ s	Does not exist
Cut off frequency	Below 100 MHz	Of the order of GHz
Substrate resistance	0.3 Ω	(0.03–2) Ω
SOA	Poor (the appearance of the secondary breakdown)	Good (there is no secondary breakdown)
Thermal stability	Circuit additions required	No additions required
Parallel operation	With special coupling only	No additions required
Adjustable to LSI circuits	No	Yes
Driving signal	(0.1–10) A	Max 100 mA at $R_c = 50 \Omega$, $V_G = 5$ V
Driving circuit	Complex	Simple
Reverse voltage	High ($V_R > 1,500$ V)	Low ($V_R < 1,000$ V)
Transfer characteristic ($I_C = f(V_{BE})$, $I_D = f(V_{GS})$)	Exponential	At small currents quadratic, at high currents linear
Transconductance	High	Low

$$\beta_n = \frac{\mu_n \epsilon_{ox}}{2t_{ox}} \frac{W}{L} \quad (2.216)$$

is a constant of MOS transistors expressed in A/V^2 and does not have the meaning of the gain as it does for bipolar transistors. This constant thus depends on electron mobility in the channel μ_n , the dielectric constant of the oxide ϵ_{ox} , the thickness of the oxide below the gate t_{ox} , the width W and the length L of the channel. The parameters μ_n and ϵ_{ox} are constants of the technological process. Therefore, the drain current can be increased if the width of the channel, W , is increased, the length of the channel, L , is decreased, or the thickness of the oxide, t_{ox} , is decreased. The decrease of t_{ox} is limited by the gate breakdown voltage. If the length of the channel is decreased below a certain limit, the drain-source breakdown voltage will be decreased because the breakdown would occur as a punch-through. In this way instead of increasing the power one would decrease it. At the beginning of the development of the power MOS transistors (the first ones appeared in 1978) large drain currents have been obtained by increasing the channel width. However, this does have its shortcomings. First of all, this increases the necessary surface of the silicon wafer which reduces the production yield.

Fig. 2.62 Cross section of a power VMOS transistor



Currently, MOS power transistors are produced by connecting in parallel a large number of transistors on the same wafer. Usually this is done by using the so called vertical structure where the contacts of the drain and the source are on the opposite sides and the current flows vertically through the substrate. This allows a higher density of MOS cells since the depletion region spreads through the substrate vertically not laterally.

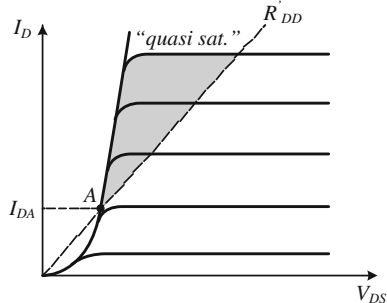
The VMOS transistor was among the first MOS power transistors based on the above principle (Fig. 2.62). The letter V originates from the shape of the profile of the grooves made in silicon by etching. The deficiency of these transistors is related to the problems of controlling this technical process. In addition, the channel is in the (111) plane so the mobility of carriers is reduced by 25 % and a higher threshold voltage is required. These are the main reasons that the production of these transistors has exhibited a decline.

2.3.1 Power VDMOS Transistor

To make a short channel one needs a double diffusion: a deep diffusion of *p*-type impurities first and then a shallow diffusion of *n*-type impurities. Both diffusions are carried out through the same opening. The length of the channel is the difference between the lateral diffusions of the *p*-type and *n*-type impurities, i.e. $L = X_{jp} - X_{jn}$. There are two types of these transistors lateral—LDMOS and vertical—VDMOS. At present the use of the polysilicon-gate VDMOS (Vertical Double-diffused MOS) prevails (Fig. 2.63).

The gate and the source contacts are on the upper side and the drain is on the lower side of the silicon wafer. The source and the drain are separated by a low doped *n* type epitaxial layer so that the breakdown voltage BV_{DS} is quite high (several hundreds V). The length of the channel is shorter than 1 μm and the drain current of the transistor is large (several tens A). The source and substrate are short circuited so that these transistors always operate at $V_{BS} = 0$. The substrate and the

Fig. 2.66 Output characteristics of IGBT



are connected as in a VDMOS transistor. If, on the other hand, R_{BE} and α_{npn} are sufficiently high, the structure from Fig. 2.65 behaves like an MOS thyristor (Fig. 2.67a, b). The thyristor effect already appears at gate voltages of the order of 3 V. Then, the PNP transistor starts conducting first, and it is followed by the *NPN* transistor. The positive feedback will act if $\alpha_{npn} + \alpha_{pnp} > 1$. The advantage of an MOS thyristor over a standard thyristor is that it can be switched on by a very low power. Another type of *BiMOS* switch is the cascade connection of the MOS and the bipolar transistors (Fig. 2.67c). This is often called the emitter switch.

The switch is controlled by the gate of the MOS transistor, M_n . When M_n is off, the bipolar transistors are also off. Since the emitter is now “open”, the breakdown voltage of the transistor T_{r1} is maximal and amounts to BV_{CBO} . On the other hand, during the turn-off all current flows into the base circuit since $I_E = 0$. Thanks to this the storage and the falloff times of the collector current are very short. The drain-source voltage of T_{r1} when off is practically V_{BB} . This means that one can use a low breakdown voltage MOS transistor (up to several tens of V), so its on resistance is very small (less than 0.1Ω). If M_n is on, T_{r1} is also on because of the base current from the battery V_{BB} . Therefore, in this switch the use is made of the advantages that include a low breakdown voltage *MOSFET*, simple control, a low R_{DS} resistance, and a high speed as well as the advantages of the common-base bipolar

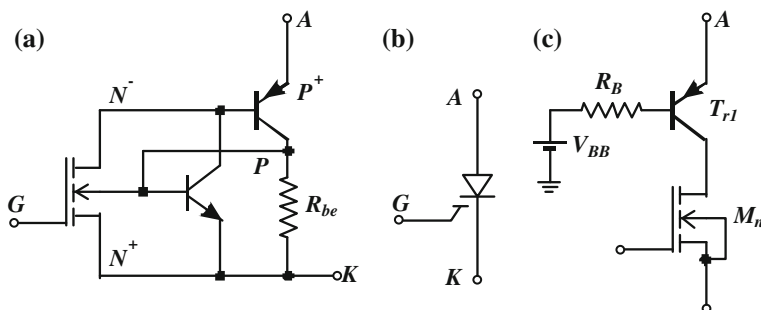


Fig. 2.67 Equivalent circuit (a), symbol of MOS thyristor (b), and emitter BiCMOS switch (c)

transistor (high breakdown voltage and high speed). A serious shortcoming of this switch is that it can be realized only by discrete components. Two transistors are therefore required, one bipolar and one *MOS*.

2.3.3 Static Parameters

The static characteristics of the standard *MOS* transistors (long channel transistors) can be described by the following equations

$$I_D = \beta_n [2(V_{GS} - V_{tn}) V_{DS} - V_{DS}^2], \quad V_{DS} < V_{GS} - V_{tn} \quad (2.217)$$

in the nonsaturated (Ohmic) region, and by

$$I_D = \beta_n (V_{GS} - V_{tn})^2, \quad V_{DS} > V_{GS} - V_{tn} \quad (2.218)$$

in the saturated region (constant current region). V_{tn} is the threshold voltage of the transistor (the gate-source voltage at which the inversion layer, i.e. a channel, is formed). The constant β_n is given by (2.216). The boundary between the saturated and the nonsaturated region is determined by

$$V_{DS} = V_{GS} - V_{tn}. \quad (2.219)$$

Due to a very short length of the channel, the characteristic $I_D = f(V_{DS})$ of power *MOS* transistors is somewhat modified. At small values of the voltage V_{DS} (2.217) applies to a good approximation. In this part the function $I_D = f(V_{DS})$ is almost linear. Since the channel is very short, it is subjected to a very high electric field and the electron mobility is decreased. At a certain critical field K_c the critical speed is reached and after that the drain current is almost constant. The voltage $V_{DSC} = LK_c$, at which the saturation is reached, is lower than the voltage V_{DS} determined by (2.217) except for small values of V_{GS} .

The static output characteristics are shown in Fig. 2.68a. For $V_{GS} < V_{tn}$ the transistor is off. The drain current I_{DSS} is then equal to the reverse saturation current of the diode between the drain and the source. I_{DSS} is of the order of μA and usually can be neglected. The breakdown occurs at a voltage BV_{DS} equal to the breakdown voltage of the mentioned diode. Its value is within limits of several tens of V up to several hundreds of V (500–600 V). The appearance of the second breakdown is possible owing to the parasitic bipolar structure, but this occurs very rarely.

The transfer characteristic $I_D = f(V_{GS})$, at $V_{DS} = \text{const.}$ (Fig. 2.68b), at the beginning of the active region (between the points A and B) is parabolic and afterwards it is approximately linear. Here also the power and the standard *MOS* transistors are different.

The linearity of the function $I_D = f(V_{GS})$ in the saturation region is particularly significant when the *MOS* transistor is used in power amplifiers.

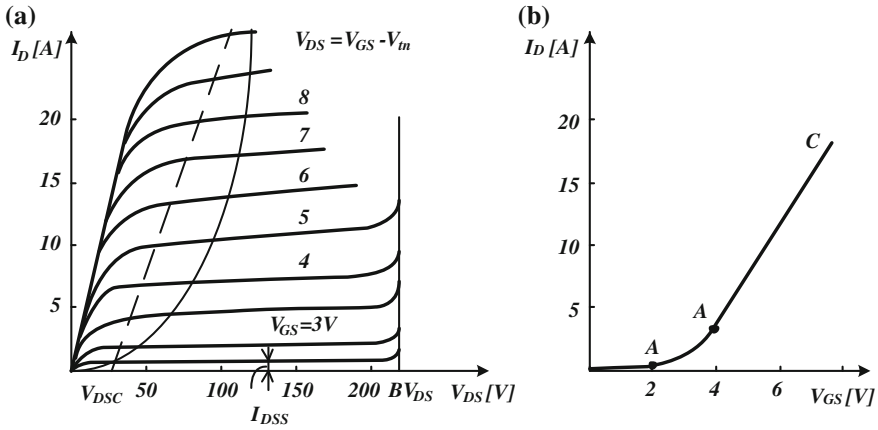


Fig. 2.68 Static characteristics of a power MOS transistor—output (a) and transfer (b)

For the switching functions of the MOS transistor only the cut off and the linear (Ohmic) regions are of interest. When off, the transistor can be replaced by a current generator I_{DSS} (Fig. 2.69a). Typically the threshold voltage V_{tn} is from 2 to 4 V and its temperature coefficient k_t is negative, ranging from 4 to 6 mV/°C. It can, thus, be written that V_{tn} temperature is

$$V_{tn} = V_{tn0} - k_t(T - T_0), \quad (2.220)$$

where T and T_0 are the actual and the room temperature, respectively, and $V_{tn0} = V_{tn}(T_0)$.

The output voltage V_{DS} of a turned-on transistor should be as small as possible. Then, $V_{GS} - V_{tn} \gg V_{DS}$ and the quadratic member in (2.217) can be neglected

$$I_D \approx 2\beta_n(V_{GS} - V_{tn})V_{DS}. \quad (2.221)$$

The constant β_n depends on temperature because electron mobility is a function of temperature

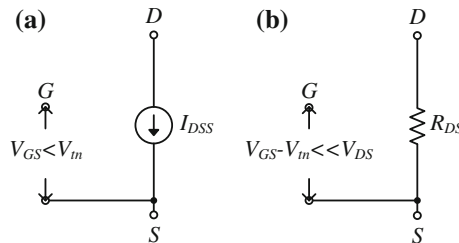


Fig. 2.69 Equivalent circuits of a power MOS transistor in the on (a) and off (b) states

$$\mu_n(T) = \mu_{on} (T/T_0)^{-n}, \quad (2.222)$$

where n is within limits $1.52 < n < 2.5$, $\mu_{on} = \mu_n(T_0)$, and T_0 [K] is the room temperature. Now, on the basis of (2.214) and (2.218)

$$\beta_n(T) = \beta_{n0} (T/T_0)^{-n}, \quad (2.223)$$

where $\beta_{n0} = \beta_n(T_0)$. Finally, it turns out that the drain current versus temperature is

$$I_D = 2 \beta_{n0} (V_{GS} - V_{tn0}) V_{DS} (T/T_0)^{-n} \left[1 + \frac{k_t}{V_{GS} - V_{tn0}} (T - T_0) \right]. \quad (2.224)$$

The temperature coefficient of this current is obtained by differentiating (2.224) over T , at $V_{GS} = \text{const.}$ and $V_{DS} = \text{const.}$

After rearrangement one obtains:

$$\frac{dI_D}{dT} = 2 \beta_{n0} V_{DS} \left[\left(1 - n + n \frac{T_0}{T} \right) k_t - \frac{n}{T} (V_{GS} - V_{tn0}) \right]. \quad (2.225)$$

Figure 2.70 shows the function $I_D = f(V_{GS})$ and the normalized temperature coefficient of this current as functions of V_{GS} at different temperatures for $V_{DS} = 0.5$ V. It can be seen that at low values of I_D the temperature coefficient is positive, whereas at higher values of I_D it is negative. The zero temperature coefficient is at V_{GSO} which is obtained by equating (2.225) to zero

$$V_{GSO} = V_{tn} + \frac{T}{n} k_t. \quad (2.226)$$

For instance, for $n = 2$, $k_t = -6$ mV/°C, $V_{tn0} = 2$ V, and at room temperature $T = 300$ K from (2.226) it follows $V_{GSO} = 2.9$ V. In practice, as a rule, when a

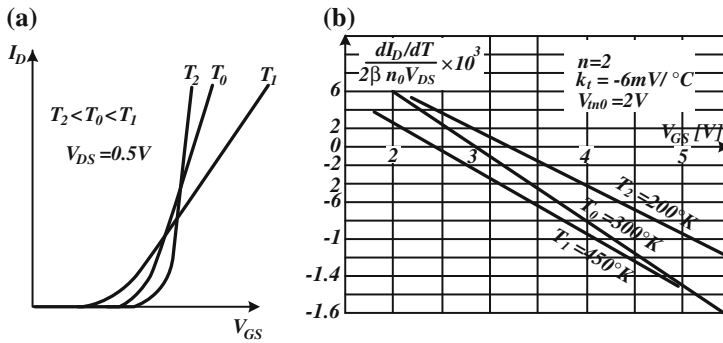


Fig. 2.70 Drain current (a) and normalized temperature coefficient of drain current (b) as functions of V_{GS} at different temperatures according to (2.220) and (2.221), respectively

transistor is on, $V_{GS} \gg V_{GSO}$ and the drain temperature coefficient is negative. This is an important property. Thanks to this, *MOS* components are temperature self-compensating. This means that a positive internal thermal feedback cannot possibly arise which leads bipolar transistors to the secondary breakdown. In other words, *MOS* transistors are not prone to the “thermal run-away”.

The most important parameter of an *MOS* power transistor while conducting is the on resistance, R_{DS} . It consists of several components such as the resistance of the metal and the metal contacts of the source, the resistance of the n^+ regions of the drain and source. Those prevailing, however, are the channel resistance, R_{DL} , and the resistance of the drain region, R_{DD} . Therefore

$$R_{DS} = R_{DL} + R_{DD}. \quad (2.227)$$

Using (2.217), the channel resistance is:

$$R_{DL} = \frac{1}{dI_D/dV_{DS}} \approx \frac{1}{2\beta_n(V_{GS} - V_{tn})} \quad (2.228)$$

and it decreases with increasing V_{GS} . However, the influence of R_{DD} is more important, i.e. $R_{DD} \gg R_{DL}$. This is the resistance of the n -epitaxial layer of the drain, determined by

$$R_{DD} \approx \frac{1}{q\mu_n N_D} \frac{d}{S}, \quad (2.229)$$

where N_D is the donor concentration in the n -layer of the drain, d is the thickness of this layer, and S is the total surface of the *MOSFET*. Since the breakdown voltage BV_{DS} also depends on μ_n and N_D of the epitaxial layer, then also $R_{DD} = f(BV_{DS})$. For instance, for *SGS* power transistors it is approximately

$$R_{DD}(BV_{DS}) = R_{DD}(BV_{DSO}) \left(\frac{BV_{DS}}{BV_{DSO}} \right)^K, \quad (2.230)$$

where the constant K depends on the voltage range of BV_{DS} :

- $K = 1.8$ for low voltage transistors (50–100 V),
- $K = 2.5$ for high voltages (100 up to 500 V) and
- $K = 2.7$ for breakdown voltages greater than 500 V.

BV_{DSO} is the lowest breakdown voltage in the range considered. For *SGS* power *MOS* transistors with breakdown voltages from 500 up to 1000 V

$$R_{DD}(1000 \text{ V}) = R_{DD}(500 \text{ V}) \left(\frac{1000 \text{ V}}{500 \text{ V}} \right)^{2.7} = 7.3 R_{DD}(500 \text{ V}). \quad (2.231)$$

Thus, the resistance R_{DD} , and consequently the resistance R_{DS} increase exponentially with the breakdown voltage. For instance, R_{DS} is typically from several tenths of Ω to several Ω if $BV_{DS} < 100$ V, whereas for transistors having a breakdown voltage in the range of $300 \text{ V} < BV_{DS} < 500$ V this resistance is from several Ω up to 10Ω .

The resistance R_{DS} is highly temperature dependent. Namely, in view of (2.228), (2.229), (2.223), and (2.220) one can write

$$\begin{aligned} R_{DL} &= \frac{1}{2\beta_{n0}(V_{GS} - V_{tn0})} \frac{(T/T_0)^n}{1 + \frac{k_t}{V_{GS} - V_{tn0}}(T - T_0)} = \\ &= R_{DL}(T_0) \frac{(T/T_0)^n}{1 + \frac{k_t}{V_{GS} - V_{tn0}}(T - T_0)}, \end{aligned} \quad (2.232)$$

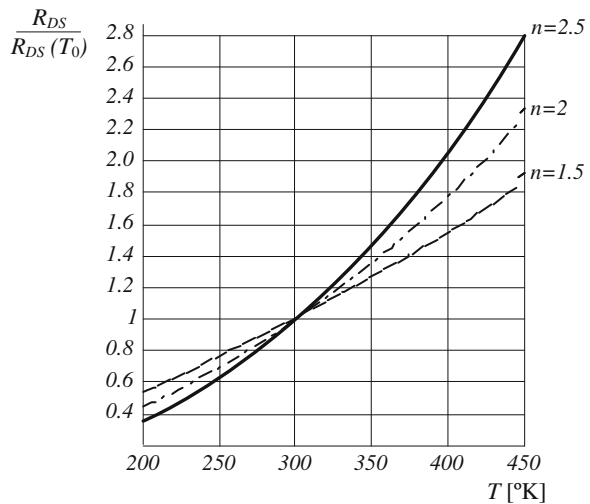
$$R_{DD} = \frac{d}{qN_d S \mu_{n0}} \left(\frac{T}{T_0}\right)^n = R_{DD}(T_0) \left(\frac{T}{T_0}\right)^n. \quad (2.233)$$

Since $k_1(T - T_0)/(V_{GS} - V_{tn0}) \ll 1$, then

$$R_{DS} = [R_{DL}(T_0) + R_{DD}(T_0)] (T/T_0)^n = R_{DS}(T_0) (T/T_0)^n. \quad (2.234)$$

Figure 2.71 shows the normalized drain-source on resistance R_{DS} as a function of temperature for different values of the constant n . For instance, for $n = 2$ an increase of temperature from 300 to 450 K results in the increase of the resistance R_{DS} 2.25 times. It should be emphasized that the voltage V_{DS} of a conducting transistor is almost temperature-independent because R_{DS} increases with temperature and I_D decreases with temperature.

Fig. 2.71 Normalized drain-source on-resistance of an MOS transistor as a function of temperature for $n = 1.5$, $n = 2$, $n = 2.5$ if $T_0 = 300$ K



2.3.3.1 Dynamic Parameters

The parasitic inter-electrode capacitances have a dominant influence on the transient mode of *MOS* switching circuits (Fig. 2.72a). At the places where the metallic electrode of the gate overlaps with the diffused n^+ regions of the source and drain, parasitic capacitances C_{gs} and C_{gd} exist between the gate and the source and between the gate and the drain, respectively. In addition, there is also a capacitance C_{ds} of the reverse biased drain-substrate p-n junction (the source and the substrate of power *MOS* transistors are short circuited). All these capacitances are dependent on the drain-source voltage. Owing to the large surface areas of power transistors, the average values of these capacitances are quite high, typically from a hundred to several hundreds of pF.

For power transistors, the manufacturers give data for the input

$$C_{iss} = C_{gs} + C_{gd}, \quad (2.235)$$

feedback

$$C_{rss} = C_{gd} \quad (2.236)$$

and output capacitance

$$C_{oss} = C_{ds} + C_{gd}. \quad (2.237)$$

The dependencies of these capacitances on voltage V_{DS} are shown in Fig. 2.72b. All this applies only for the static conditions. During transients, however, the input and the output capacitance are increased due to Miller's effect. The transient mode will be analyzed on an example of a switch loaded by a resistor R_D (Fig. 2.73a). It is assumed that the generator with an internal resistance R_g produces a driving voltage V_g , which undergoes step changes.

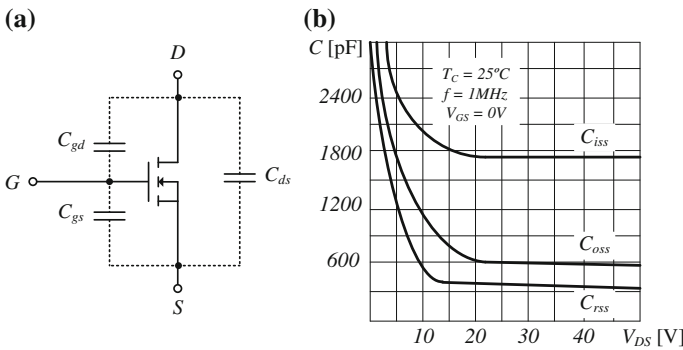


Fig. 2.72 Inter-electrode capacitances (a) and dependencies of input, feedback, and output capacitances on the drain-source voltage (b)

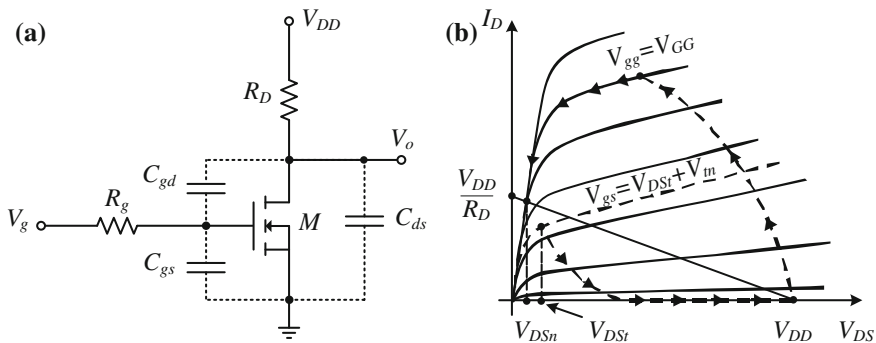


Fig. 2.73 Inverter based on a power MOS transistor (a) and the trajectory of the operating point during transient (b) denoted by dotted lines

The channel of power MOS transistors is very short so that the transition time of the electric charge between the source and the drain is negligible. In other words, this means that the transition mode is determined primarily by the charging and discharging times of the inter-electrode capacitances.

Figure 2.74 shows the pulse waveforms of the responses of the voltages gate-source, drain-source, and drain current to a step-voltage drive. At the instant t_1 when $V_g = V_{GG}$ the input capacitance C_{iss} starts charging,

$$v_{gs}(t) = V_{GG} \left(1 - e^{-\frac{t}{C_{iss}R_g}} \right). \quad (2.238)$$

As long as $V_{GS} < V_{tn}$, the transistor is off, i.e. $I_D = 0$ and $V_{DS} = V_{DD}$. Therefore, there is a delay in the turn-on process of the transistor. From (2.238) and condition $V_{GS}(t_{dr}) = V_{tn}$, it follows that

$$t_{dr} = C_{iss} R_g \ln \frac{V_{GG}}{V_{GG} - V_{tn}}. \quad (2.239)$$

After t_{dr} the drain current increases rapidly. The voltage V_{DS} slowly decreases until the operating point reaches the Ohmic region. Then both the drain current and the drain-source voltage decrease rapidly as the resistance R_{DS} is very small (several tenths of Ω up to several Ω). The trajectory of the operating point in Fig. 2.73b is denoted by dotted lines. Thus, time t_r can be determined from the condition that the voltage drain-source is at the boundary between the active and the saturation region. In practice, however, the approximate expression

$$t_r \approx 2.2 R_g C_{iss}. \quad (2.240)$$

is often used. Upon application of a negative drive at ($t = t_2$), the voltage V_{DS} and the current I_D are changed little. Here too, similarly to bipolar transistors, there exists a delay time, which is not caused by the piled-up charge but by the fact that

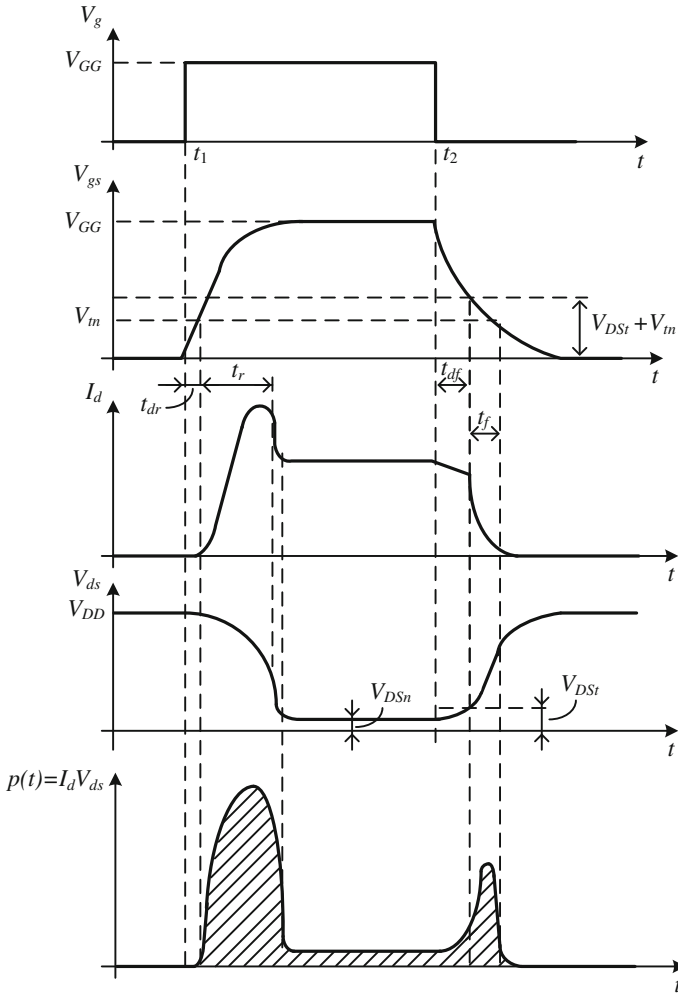


Fig. 2.74 Pulse waveforms of voltages V_{GS} and V_{DS} , current I_D , and dissipation $P(t)$ for a step drive if the internal resistance of the generator is R_g

the transistor remains in the saturated region as long as $V_{DS} < V_{GS} - V_{tn}$. Because in that region the characteristic is almost identical for different values of V_{GS} , the current I_D and the voltage V_{DS} will change very little. The delay time t_{df} at the falloff of V_{GS} can be determined from the condition

$$v_{gs}(t_{df}) = V_{GG} e^{-\frac{t_{df}}{C_{iss} R_g}} = V_{DSs} + V_{tn}, \quad (2.241)$$

where V_{DSs} is the voltage V_{DS} at the boundary between the active and the saturated region. From (2.237) one obtains

$$t_{df} = C_{iss} R_g \ln \frac{V_{GG}}{V_{DSf} + V_{tn}}. \quad (2.242)$$

After t_{df} the current I_D decreases and the voltage V_{DS} increases. When $V_{GS}(t) = V_{tn}$, the transistor is at the turn-on/turn-off threshold, thus $I_D \approx 0$. The falloff time of the drain current is determined by

$$t_f = C_{iss} R_g \ln(1 + V_{DSf}/V_{DSf}). \quad (2.243)$$

After t_f the output capacitance is charged by the load current.

During both delays, t_{dr} and t_{df} , power dissipation in the transistor is small so that these times are not critical. During t_r and t_f power dissipation is significant (Fig. 2.74) and it is important that these times are short. Obviously, the rate of change of the voltage V_{GS} will have a considerable influence on the transient mode. For this reason, one should keep the resistance R_g as low as possible.

If the voltage V_{GS} changed abruptly like V_g ($R_g = 0$), the delay times and t_f would be negligible. The time t_r would be determined by the time of discharging the output capacitance C_{oss} by a large drain current of the transistor in the saturation region.

Finally, it should be emphasized that the waveforms in Fig. 2.74 are approximate and that they illustrate only qualitatively the transient process. Namely, the Miller's effect and the voltage dependencies of the inter-electrode capacitances have not been taken into account. For instance, during t_r and t_f the capacitance C_{gd} due to Miller's effect is transferred to the input with a multiplying factor of $(1 + A_v)$, where $A_v = |dV_{DS}/dV_{GS}|$ is the voltage gain. Then $C_{iss} = C_{gs} + (1 + A_v)C_{gd}$, and its dependence on V_{GS} at $V_{DS} = 5$ V and $V_{DS} = 10$ V is shown in Fig. 2.75.

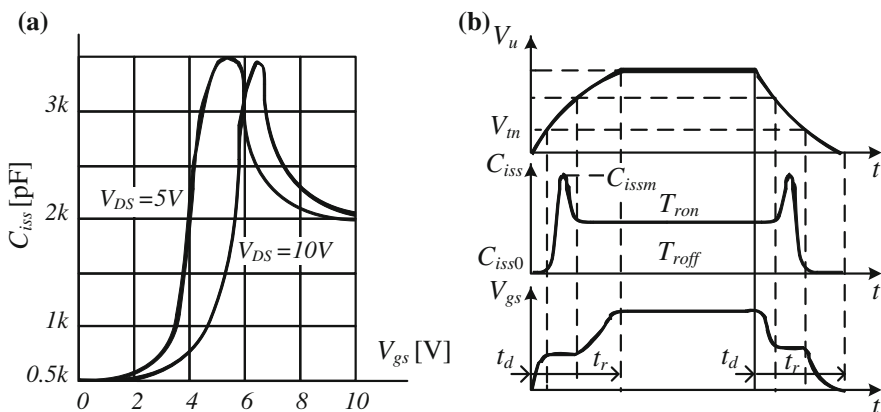


Fig. 2.75 Input capacitance of transistor MTM5N40 as a function of gate-source voltage (a) and real variations of input capacitance and gate-source voltage for an exponential drive (b)

The real variation of the voltage V_{GS} is shown in Fig. 2.75b. Namely, after t_d , the voltage across the capacitor C_{gs} remains for some time almost constant because the input current re-polarizes the feedback capacitance C_{gd} .

Even though the mentioned effects have not been taken into account in the derived equations, they are significant because they indicate the character of the dependence of the transient mode.

2.3.3.2 Driving Circuits

On the basis of the previous analysis, it may be concluded that the drive will be optimal if the following conditions are met:

- the internal resistance of the driving generator is very low,
- the driving generator has a large current capacity so that it can very quickly charge and discharge the input capacitance of the transistor, and
- the voltage of the driving generator V_{GG} is sufficiently high so that the transistor is fully on (the operating point is in the region of constant resistance R_{DS}).

It is difficult to meet all these conditions. The driving circuits are, as a rule, much simpler than they are for bipolar transistors. Since the static input resistance of an *MOS* transistor is very high, it can be driven directly by the output of a *CMOS* buffer (Fig. 2.73). For this purpose, the *CMOS* buffers having equal sink and source currents, like *CD4007*, *CD4041*, and *CD4069*, are recommended. Otherwise, the rise and the fall time of the drive of the power *MOS* transistor will be different.

Here, only the changes of the output voltage $V_o = V_{GS}$ of a *CMOS* buffer-inverter will be considered as their influence on the transient mode of a power transistor is the greatest. The corresponding inter-electrode capacitances are denoted in Fig. 2.76a. Their variations with the voltage V_{DS} will be neglected.

All inter-electrode capacitances can, by means of Miller's theorem, be reduced to the equivalent input and output capacitances (Fig. 2.76b). According to this theorem, if two branches are coupled by a capacitance C , they can be decoupled in such a way that C is referred to the input capacitance C_{e1} and the output capacitance C_{e2} ,

$$C_{e1} = C(1-A_v), \quad C_{e2} = C(A_v-1)/A_v,$$

where A_v is the voltage gain. The total voltage changes at the input and at the output of a *CMOS* inverter are equal, but of the opposite signs, so $A_{v1} = -1$. If the gain of a power transistor is denoted by A_{v2} , one obtains

$$C_I = C_{gsn} + C_{gsp} + 2(C_{gdn} + C_{gdp}) \quad \text{and} \quad (2.244)$$

$$C_O = C_{dsn} + C_{gsp} + 2(C_{gdn} + C_{gdp}) + C_{gs} + (1 + |A_v|) C_{gd}. \quad (2.245)$$

The capacitances of a *CMOS* transistor are at least two orders of magnitude lower, thus their influence on the transient mode can be neglected. Therefore,

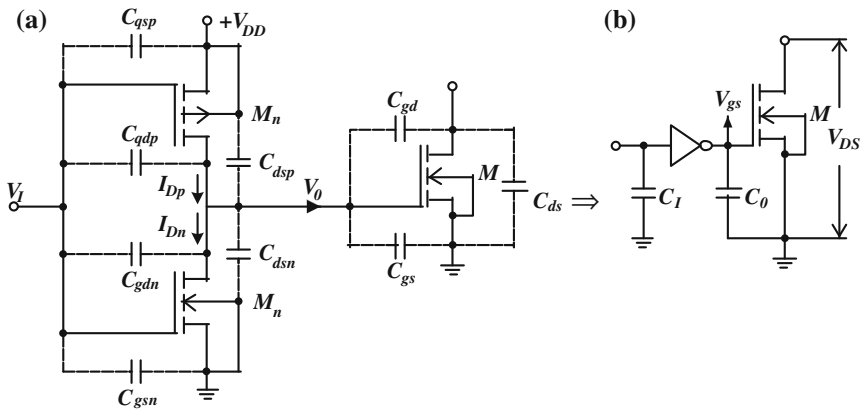


Fig. 2.76 CMOS inverter driving circuit (a) including the parasitic capacitances and the equivalent circuit for analyzing the transient mode (b)

$$C_O \approx C_{gs} + (1 + |A_v|) C_{gd} . \quad (2.246)$$

On the other hand, the charging and discharging times of the input capacitance C_I can also be neglected. This means that the gate voltage of a CMOS inverter will be abrupt if the input voltage change V_I is abrupt. In this case, the trajectory of the operating point of a CMOS inverter during transient mode is as shown in Fig. 2.77a.

While $V_I = 0$ ($t < t_1$) M_n is off and M_p is on, so $V_O = V_{GS} = V_{DD}$. At $t = t_1$ M_p is switched off and M_n is switched on. Practically, it may be considered that the channel of the PMOS transistor is instantaneously cut off, and $I_{Dp} = 0$. The capacitor C_O is being discharged by the current of the NMOS transistor, and

$$V_{gs} = V_{DD} - \frac{1}{C_i} \int_0^t I_{dn} dt \quad (2.247)$$

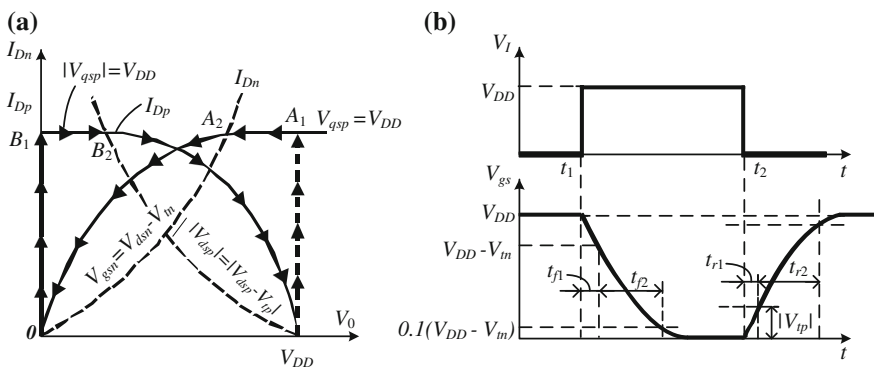


Fig. 2.77 Trajectory of the operating point of a CMOS inverter (a) and its output voltage (b) for a step input drive

At $t = t_1 + 0$ the operating point is in the position A_1 (Fig. 2.77a). Thus, M_n is in the saturated region and

$$I_{dn} = \beta_n (V_{DD} - V_{tn})^2. \quad (2.248)$$

From (2.243) and (2.244) it follows that

$$V_{gs} = V_{DD} - \frac{\beta_n (V_{DD} - V_{tn})^2}{C_o} t. \quad (2.249)$$

This variation of the voltage V_{GS} proceeds during the time t_{f1} , while M_n is in the saturated region (between points A_1 and A_2). This time is determined from the condition:

$$V_{gs}(t_f) = V_{DD} - V_{tn} \quad (2.250)$$

and the Eq. (2.245).

Finally,

$$t_{f1} = \frac{C_o}{\beta_n (V_{DD} - V_{tn})} \frac{V_{tn}}{V_{DD} - V_{tn}}. \quad (2.251)$$

For $t > t_{f1}$ M_n is in the nonsaturated region, and:

$$V_{gs}(t) = V_{DD} - V_{tn} - \frac{\beta_n}{C_o} \int_0^t [2(V_{DD} - V_{tn}) V_{gs} - V_{gs}^2] dt \quad (2.252)$$

Upon differentiation of (2.248), after the separation of the variables V_{GS} and t and reintegration, it follows that

$$V_{gs}(t) = \frac{2(V_{DD} - V_{tn})}{1 + e^{t/\tau_n}}, \quad (2.253)$$

where the time constant is

$$\tau_n = \frac{C_o}{2 \beta_n (V_{DD} - V_{tn})}. \quad (2.254)$$

The transient mode ends when the capacitor C_o is fully discharged ($V_{GS} = 0$). Theoretically this implies an infinite time. For this reason, the practical condition for the completion of the transient mode is when the voltage across the capacitor reaches 10 % of the voltage at the start of the considered interval, i.e.,

$$V_{gs}(t_f) = 0.1(V_{DD} - V_{tn}). \quad (2.255)$$

From (2.253) and (2.255), it follows that

$$t_{f2} = 2.9 \tau_n. \quad (2.256)$$

The total fall time of V_{gs} is $t_f = t_{f1} + t_{f2}$. In view of (2.251) and (2.256)

$$t_f = 2\tau_n \left(1.45 + \frac{V_{tn}}{V_{DD} - V_{tn}} \right). \quad (2.257)$$

From $t = t_2$, when again $V_1 = 0$, the process of charging of C_O starts, but this time by the current I_{Dp} of the transistor M_p . Namely, it may be assumed that M_n is off instantaneously, and

$$V_{gs}(t) = V_{co} + \frac{1}{C_i} \int_0^t I_{dp} dt \quad (2.258)$$

where $V_{Co} = V_{GS}(t_2 - 0) = 0$ is the initial voltage across the capacitor C_O . The operating point follows the trajectory $O - B_1 - B_2 - V_{DD}$ (Fig. 2.77a). Thus, the rise time of the voltage V_{GS} consists of two-time intervals, t_{r1} and t_{r2} . During the first interval, M_p is saturated and

$$I_{dp} = \beta_p (V_{DD} + V_{tp})^2. \quad (2.259)$$

Now, on the basis of (2.258) and (2.259) and from condition $|V_{DSp}| = |V_{GSp} - V_{tp}|$ or $V_{GS}(t_{r1}) = |V_{tp}|$, there follows:

$$t_{r1} = \frac{C_O}{\beta_p (V_{DD} + V_{tp})} \frac{|V_{tp}|}{V_{DD} + V_{tp}}. \quad (2.260)$$

During the interval, t_{r2} M_p is in the active region, so

$$I_{dp} = \beta_p [2(V_{DD} + V_{tp})(V_{DD} - V_{gs}) - (V_{DD} - V_{gs})^2]. \quad (2.261)$$

On the basis of (2.258) and (2.259) and with the initial condition $V_{Co} = V_{GS}(t_{r1}) = |V_{tp}|$ one obtains

$$V_{gs} = V_{DD} - 2 \frac{V_{DD} + V_{tp}}{1 + e^{t/\tau_p}}, \quad (2.262)$$

where

$$\tau_p = \frac{C_O}{2 \beta_p (V_{DD} + V_{tp})}. \quad (2.263)$$

According to (2.262) the steady state, when $V_{gs} = V_{DD}$, will be reached after an infinite time. For this reason, t_{r2} will be determined using a practical condition, according to which

$$V_{DD} - V_{gs}(t_{r2}) = 0.1(V_{DD} + V_{tp}). \quad (2.264)$$

Thus, like in the case of the determination of t_{f2} , t_{r2} is the interval during which the operating point completes 90 % of the trajectory while M_p is in the active region. Now, from (2.262) and (2.264)

$$t_{r2} = 2.9\tau_p. \quad (2.265)$$

The total rise time $t_{r1} + t_{r2}$ is thus

$$t_r = 2\tau_p \left(1.45 + \frac{|V_{tp}|}{V_{DD} + V_{tp}} \right). \quad (2.266)$$

If the CMOS transistors are symmetrical, i.e., $\beta_n = \beta_p$ and $V_{tn} = |V_{tp}|$, then $\tau_n = \tau_p$ and $t_f = t_r$. Typical for the CD4000 series of CMOS integrated circuits is that $V_{tn} = |V_{tp}| = 1.5$ V and the supply voltage is within limits $3 \text{ V} < V_{DD} < 18 \text{ V}$. The practical values are, however, $V_{DD} > 5 \text{ V}$. Now, the rise and the fall time are:

$$t_r = k_{vp} \tau_p, \quad t_f = k_{vn} \tau_n, \quad (2.267)$$

where the constants k_{vn} and k_{vp} depend on V_{DD} and range from 3.1 up to 3.75. The denominators in (2.254) and (2.263) are respectively equal to the reciprocal values of the channel resistance of NMOS and PMOS transistors in the active region. Therefore, it can be written that

$$t_f = k_{vn} C_O R_{DSN}, \quad t_r = k_{vp} C_O R_{DSP}. \quad (2.268)$$

The manufacturers give the output currents I_{DSN} and I_{DSP} for certain values of V_{DSN} , V_{DSP} , and V_{DD} . Most often $V_{DSN} = |V_{DSP}| = 0.5 \text{ V}$. On this basis, one can calculate the approximate values of the resistances R_{DSN} and R_{DSP} . Namely

$$R_{DSN} \approx V_{DSN}/I_{DSN}, \quad R_{DSP} \approx V_{DSP}/I_{DSP}. \quad (2.269)$$

Thus, e.g. for CMOS inverters CD4069 at $V_{DD} = 10 \text{ V}$ and $V_{DSN} = |V_{DSP}| = 0.5 \text{ V}$, $I_{DSN} = |I_{DSP}| = 2.6 \text{ mA}$, and

$$t_f = t_r = 3.6 C_O * 0.5 / 2.6 \approx 0.7 C_O [\text{ns}]; C_O \text{ in } [\text{pF}].$$

On the basis of the previous simple expressions the rise and the fall time of the gate-source voltage of a power MOS transistor can easily be calculated. If the reduction

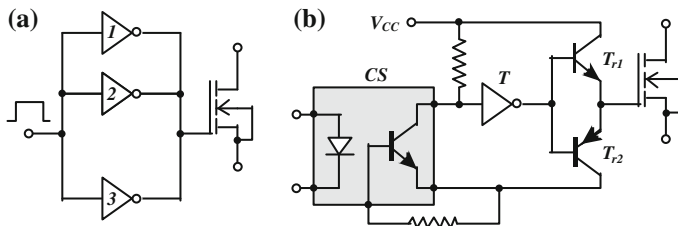


Fig. 2.78 Driving circuit for M CMOS inverters (a) and for a complimentary pair of bipolar transistors (b) when galvanically separated from the control circuit by an opto-coupler

of these times is required, two alternatives (Fig. 2.78) are recommended. In the first instant, the M inverters are connected in parallel. Then, the transistor resistances and times t_r and t_f are also M times lower, i.e.,

$$t_f = k_{vn} C_O \frac{V_{DSN}}{M I_{DSN}}, t_r = k_{vp} C_O \frac{V_{DSP}}{M I_{DSP}} \quad (2.270)$$

In the second alternative (Fig. 2.75b), a complimentary pair of these transistors is used. The current gains of these transistors should be as high as to ensure faster charging or discharging of the capacitor C_O . The method of galvanic isolation of the control circuit of the DC/DC converter from the driving circuit is also shown (Fig. 2.75b). The isolation is carried out by an opto-coupler (OC). Pulse transformers are also used for this purpose. The Schmitt trigger reshapes the pulses of the opto-coupler output and filters out the slow-varying noise components. Thanks to the regenerative character of the Schmitt trigger operation the drive of the bipolar transistors as a function of time is almost ideal.

Example 2.5 Compare the dynamic characteristics of the switch from Fig. 2.73a with those from Fig. 2.79 for the same excitation using PSPICE software package. The supply voltage is $V_{DD} = 100$ V, $\beta_n = \beta_p = 100$ and the excitation voltage is the pulse with an amplitude 15 V, frequency 50 kHz and $R_g = 100 \Omega$.

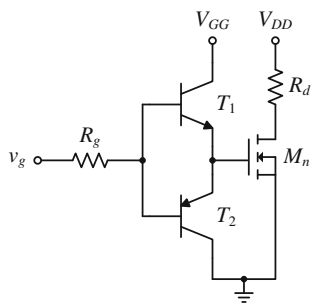


Fig. 2.79 Inverter with MOS transistor and a pair of complementary bipolar transistors in excitation circuit

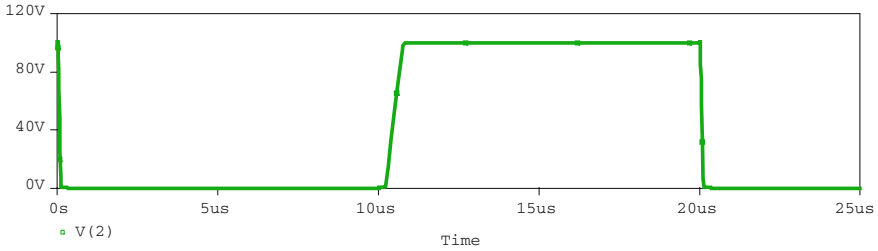


Fig. 2.80 Waveform of output voltage for a switch with MOS transistor and a circuit to speed up transition processes

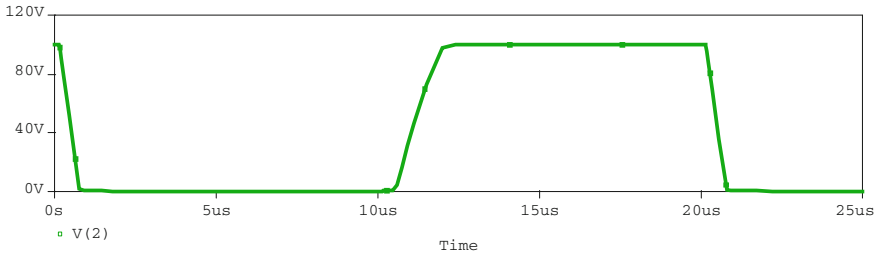


Fig. 2.81 Waveform of output voltage for a switch with MOS transistor and without circuit to speed up transition processes

- (a) Comparison of dynamic characteristics of the switch from Fig. 2.73a with those from Fig. 2.79 for the same excitation and using PSPICE software package are presented in Figs. 2.80 and 2.81.

2.3.4 Safe Operation Area

In the course of transistor selection, care must be taken that the operating point does not leave the safe operation area. Like in the case of the bipolar transistors this area is limited by the breakdown voltage, the maximum current, the permitted dissipation and, for MOS transistors also by the maximum on resistance (Fig. 2.82).

The maximum drain voltage is determined by the drain-source breakdown voltage BV_{DS} when the gate and source are short circuited. As already mentioned, the secondary breakdown is a rare phenomenon in MOS transistors. Also, care must be taken with the maximum gate voltage BV_{GS} even though this parameter is not included in the *SOA* definition. BV_{GS} is the breakdown voltage of the gate oxide that results in a permanent damage to the transistor. The thickness of the oxide is around $0.1 \mu\text{m}$ and the gate breakdown voltage is $20 \text{ V} < BV_{GS} < 40 \text{ V}$. In low power transistors, a Zener diode is built into protect the gate against breakdown.

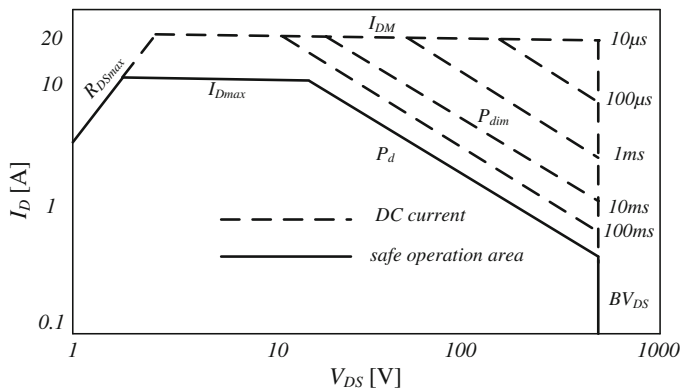


Fig. 2.82 Safe operation area of a power MOSFET

The gate-source capacitance of MOS transistors intended for currents of several A and higher is large (from several hundreds to several thousands pF) so that these devices do not need a Zener diode. Practical experience, however, shows that the gate breakdown is the most frequent cause of failure. For this reason, an external protection of the gate by fast diodes is recommendable. This is particularly relevant for circuits likely to undergo fast variations of currents and voltages with significant amplitudes (spikes). It is good practice that the driving circuit is sufficiently powerful in order to be able to share the load of possible “spikes”.

The maximum drain current is limited by the maximum junction temperature and depends on the case temperature T_c , or on the power of dissipation P_d and the cooling efficiency. The junction temperature can be written as:

$$T_j = T_c + R_{jc} P_d, \quad (2.271)$$

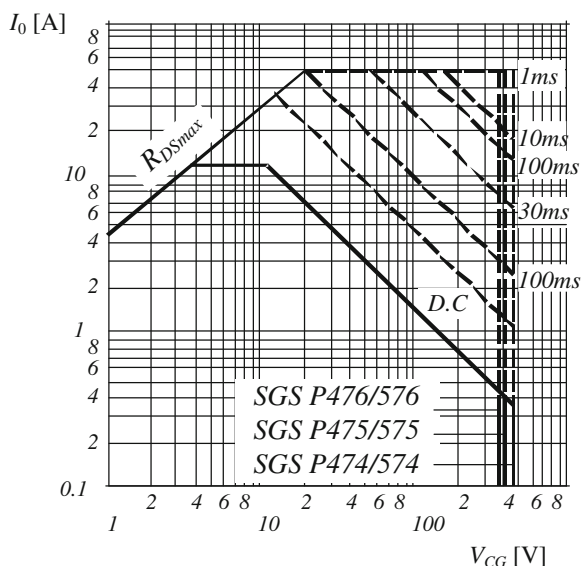
where R_{jc} is the junction-case thermal resistance. Since the power of dissipation in a transistor is $P_d = I_D^2 R_{DS}$, the maximum transistor current is

$$I_{Dmax} = \sqrt{\frac{T_{jmax} - T_c}{R_{DS} R_{jc}}}. \quad (2.272)$$

In the pulse mode of operation, the maximum current is increased because the temperatures of the crystal and the case are decreased.

The maximum dissipation is limited by the thermal stability. Namely, the greatest losses are in the resistance R_{DS} . As shown (Fig. 2.71), this resistance increases exponentially with temperature. Due to this dissipation increases and it is possible that, if cooling is not properly designed, a thermal instability may occur causing junction burn up. In the pulse mode, the permitted dissipation depends upon the duty cycle. For shorter pulses, the permitted dissipation is higher (Fig. 2.83).

Fig. 2.83 Safe operation areas of power VDMOS transistors manufactured by SGS



The maximum value of the resistance R_{DS} also limits the safe operation area. This limitation becomes significant at high drain currents and it is proportionally less significant as R_{DS} is lower.

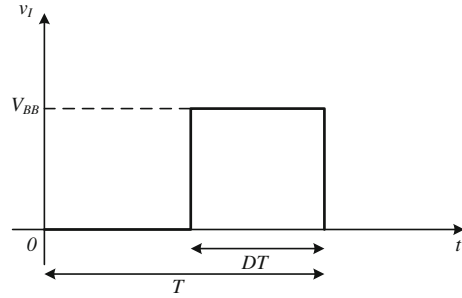
Figure 2.83 shows the operating areas of three types of power MOS transistors manufactured by SGS. The differences are only in the values of breakdown voltages.

It should be emphasized that the catalogue data on SOA curves are not very reliable in practical applications. First of all, they do not include limitations due to the gate voltage. They also do not take into account the speeds of the current or voltage changes, etc. The restrictions given are primarily the boundaries beyond, which the reliable operation of the device cannot be guaranteed. In any specific case, the designer should determine the safe operation area taking into account the device ratings and the peculiarities of the application.

Problems

- 2.1 It is known that $\alpha_F = 0.99$, $\alpha_R = 0.01$, $BV_{CBO} = 80$ V and $n = 4$. Determine the breakdown voltage of a bipolar transistor with ZE, if:
 - (a) both p-n junctions are reversely biased,
 - (b) the base is broken, and
 - (c) the base and the emitter are short-circuited.
- 2.2 For the circuit from Fig. 2.48a determine the minimum value of resistance R in the circuit to avoid transistor breakdown. The parameters of the circuit are: $V_{CC} = 15$ V, $BV_{CBO} = 60$ V, $L = 10$ mH, $f = 20$ kHz, $V_{CES} = 0.2$ V and $D = 0.5$. Assume that the transistor turn off time is much shorter than the time constant L/R_0 . The transistor excitation signal is shown in Fig. 2.84.

Fig. 2.84 Excitation signal for the circuit from Fig. 2.48a



2.3 For the circuit from Fig. 2.48a determine:

- (a) the required on time of the switch for which the peak energy stored in the inductor is 1 J, and
- (b) the value of the resistance R_0 connected in a series with the diode D to obtain a switching frequency of 100 kHz.

The circuit has $V_{CC} = 12$ V and $L = 10$ mH. Assume that the transistor and the diode are ideal.

- 2.4 Design the turn off snubber circuit shown in Fig. 2.49a if $V_S = 150$ V, $I_L = 10$ A and $t_f = 0.6$ μ s. The switching frequency is $f = 100$ kHz, and the duty factor is $D = 0.4$. The voltage on the switch should reach V_S , when the current through the switch reaches 0. A time equal to 5 time constants is necessary to discharge the capacitor when the switch is closed.
- 2.5 For the circuit from Fig. 2.60 determine the resistance R_B so that $I_{D1} = 2I_{D2}$ in steady state if $V_{CC} = 60$ V, $R_C = 50$ Ω , $\beta = 20$ and $V_{pn} = 0.7$ V. The excitation signal is a pulse with an amplitude of 10 V.
- 2.6 Determine the turn on time for the switch from Fig. 2.73 if $C_{iss} = 5$ nF, $V_{CC} = 80$ V, $R_D = 10$ Ω and $R_g = 100$ Ω . The excitation signal is a pulse with $V_{GG} = 15$ V.
- 2.7 Determine the turn off time for the switch from Fig. 2.79 if the supply voltage is $V_{DD} = 100$ V, $\beta_n = \beta_p = 100$ and the excitation voltage is a bipolar pulse with an amplitude of 15 V, frequency 50 kHz and $R_g = 100$ Ω .

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