

## Chapter 2

# Designing Inductors

Spiral inductors are commonly used in radio-frequency integrated circuits (RFICs) to act as series or shunt elements in the matching, tank or choke circuits. The quality factor (Q) is among the most important parameters in order to evaluate an inductor's performance. Unfortunately, quality factor and frequency limitations limit RF front-end circuitry to a large number of discrete passive components and make RF front-end module integration difficult. High-quality-factor inductor design and fabrication remains a challenge for applications that depend on passive components performance, e.g. low phase-noise voltage-controlled oscillator (VCO), power amplifier (PA), low noise amplifier (LNA) and double-balanced Gilbert-cell mixers.

Here two libraries of inductors have been designed. The libraries were designed for 24 and 35 GHz. These two along with 77 GHz are among the frequencies of interest in the RF Platform project. The inductors were designed to achieve a quality factor as high as possible at these frequencies using the ISiT technology, while at the same time occupying the smallest possible area. In total 8 inductors were designed.

In order to enhance the quality factor of the inductors, a suspended structure was used. In all of the structures there is  $3\text{ }\mu\text{m}$  distance between the spiral part and the surface of the substrate. This is done by conventional MEMS micro-machining, i.e. electroplating of the structures and removal of the sacrificial layer. Later the measurements of the fabricated inductors revealed that this suspension would not have a considerable effect if the inversion layer on the silicon surface is not eliminated using poly-silicon or Argon traps. This will be presented later.

The sacrificial layer material used is copper which is named OS1 (German: "Opfer Schicht 1" meaning sacrificial layer (1) in the ISiT technology).

### 2.1 The Underlying Theory

The optimization of RF inductor performance requires the identification of the relevant parasitic components and their effects. Physical modeling leads to in-depth understanding of the devices [13].

A rough model that will be discussed throughout the optimization procedure is depicted in Fig. 2.1.  $L_S$  and  $R_S$  are the inductance and the conductor resistance.  $C_S$  models the capacitive coupling between neighboring turns.  $C_{SUB1}$  and  $C_{SUB2}$  model the capacitive coupling between the substrate and the ports. The substrate losses are neglected here.

With the help of the  $\pi$ -model of Fig. 2.2 which includes the Y-parameters (admittance parameters) the model elements can be calculated. The parameters  $L_S$ ,  $R_S$ , and  $C_{SUB1}$  and  $C_{SUB2}$  are determined.

The impedance of  $C_S$  is high at the frequencies under the self-resonance frequency of the inductor and is thus negligible in the parallel connection. For  $L_S$  and  $R_S$ :

$$-Y_{21} = \frac{1}{R_S + j\omega L_S} \Leftrightarrow R_S + j\omega L_S = -\frac{1}{Y_{21}} \quad (2.1)$$

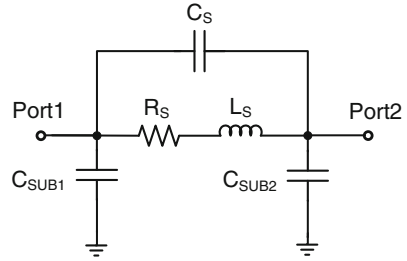
Therefore:

$$R_S = -\text{Real}\left(\frac{1}{Y_{21}}\right) \quad (2.2)$$

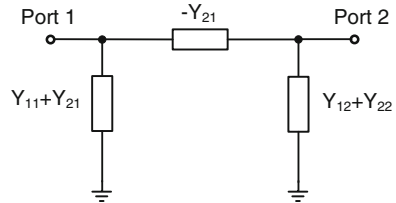
and

$$L_S = -\frac{1}{\omega} \cdot \text{Imag}\left(\frac{1}{Y_{21}}\right) \quad (2.3)$$

**Fig. 2.1** The simple inductor model, substrate losses are neglected



**Fig. 2.2**  $\pi$ -model consisting of the Y-parameters



For  $C_{SUB1}$ :

$$Y_{11} + Y_{21} = j\omega C_{SUB1} \quad (2.4)$$

Therefore:

$$C_{SUB1} = \text{Imag}\left(\frac{Y_{11} + Y_{21}}{\omega}\right) \quad (2.5)$$

With the same method  $C_{SUB2}$  can be calculated:

$$C_{SUB2} = \text{Imag}\left(\frac{Y_{12} + Y_{22}}{\omega}\right) \quad (2.6)$$

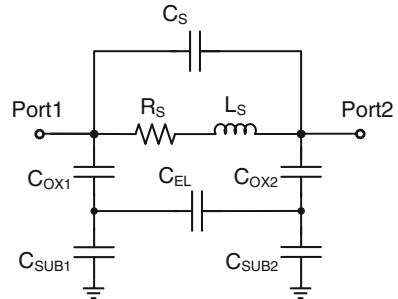
A more complete model that can also explain the decrease of the measured series resistance of the inductor with rising frequency despite of the skin effect and eddy currents is seen in Fig. 2.3 [8]. It arises when the inductors are built on a substrate which has an additional oxide layer on top, as is the case in the ISiT technology. While it is expected that the measured series resistance of the inductor increases with frequency, because of the effect of the capacitor  $C_{EL}$ , it decreases in reality [8].  $C_{EL}$  models the capacitive coupling between the neighboring turns through the silicon substrate.  $C_{OX1}$  and  $C_{OX2}$  model the coupling between the inductor and the substrate. It can be shown that the presence of  $C_{EL}$  causes the measured series resistance of the inductor to begin to decrease at frequencies around the peak of the quality factor of the inductor.

However, in this essay the first model is considered as valid enough.

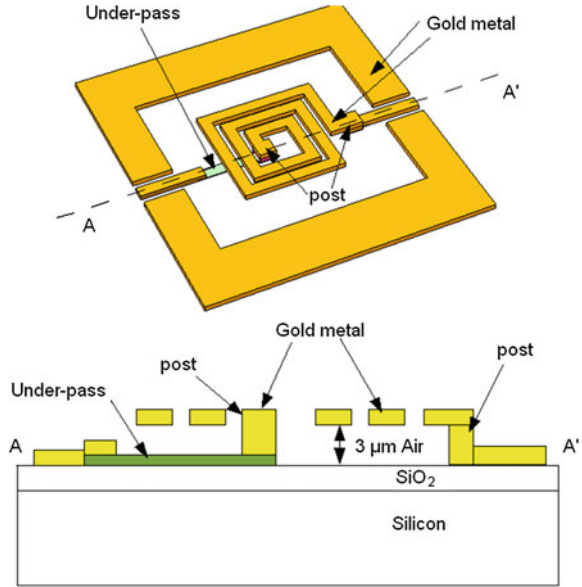
In order to have a high resonance frequency and thus a high operation frequency (i.e. frequency of maximum Q), the parasitic capacitance  $C_S$  which resonates with the inductor (in Fig. 2.1, parallel to the series connection of the resistor and the inductor) must have values as small as possible. This parasitic capacitor can be calculated from the resonance frequency ( $f_0$ ) of the inductor with the following formula:

$$C_S = \frac{1}{L_S \cdot (2\pi f_0)^2} \quad (2.7)$$

**Fig. 2.3** The more complete model for inductor (substrate losses are neglected)



**Fig. 2.4** The 3-dimensional view of one of the designed inductors and its cross-section in the AA' plane (not to scale)



The parasitic capacitor  $C_S$  can be calculated from mathematical formulas available to calculate the capacitance between parallel stripes of metal. Figure 2.4 shows the structure of one of the inductors. The inductor is made of several straight pieces of gold metal. It is possible to consider the turns of the inductor as pieces of microstrip lines that have capacitive coupling to each other, and calculate the “per length” capacitance between the two microstrip lines with the same geometrical characteristics and the same distance as the inductor turns, and then multiply the result by the total length on which the two turns neighbor each other. One method to calculate this capacitance between coupled microstrip lines is described in [9]. The parasitic capacitance from this method matches the values calculated from Eq. 2.7 for different inductors quite well. The calculated values for  $C_S$  are quite small, and for the structures designed here they range from 20 to 50 fF.

Therefore, one major goal in the design strategy would be designing inductors with trivial  $C_S$  values. For example, a long length of adjacent turns and too wide metal stripes must be avoided (wide stripes result in a lot of capacitive coupling).

As an attempt to have low parasitic capacitance, it was tried to minimize it by using a narrower metal stripe for the under-pass, which connects the termination of the inner turn of the inductor to the outside with a metal layer that is directly on the substrate (the whole structure is in the air). These two metal layers, i.e. the structure in the air and the under-pass, are directly on top of one another (as is seen in Fig. 2.4), so making the under-pass narrower would potentially reduce the parasitic capacitance. However, simulations showed that the structure with a narrower under-pass does not

have a considerably higher resonance frequency. Consequently, this was ignored in the design.

Capacitor  $C_S$ , albeit being small, is large enough to prevent using spiral inductors for 77 GHz. So according to the simulations it is not possible to use spiral inductors here. The only way to have a passive inductor in ISiT technology at this frequency is to use a transmission line.

## 2.2 Accurate Formula for the Q-factor in Two-Port Configuration

Usually in the literature the Q-factor is formulated rigorously as the ratio of imaginary part to real part of input impedance of the inductor in a one port configuration while the other port is shorted to ground [5]:

$$Q = \frac{\text{Imag}\{Z_{in}\}}{\text{Real}\{Z_{in}\}} \quad (2.8)$$

This Q-factor formulation is proper for spiral inductors when serving as shunt elements. However, spiral inductors are also used frequently as series elements in many applications and their performance is lower than anticipated by the one-port formulation in these cases. The formulas required in these conditions are usually very large [5], but when the reflection coefficients ( $\Gamma$ ) at the two inductor ports are zero meaning that the inductor is completely matched to the transmission lines connected to it, the following short expression can be used (S are the scattering parameters):

$$Q = \frac{2\text{Imag}(S_{11})}{1 - |S_{11}|^2 - |S_{21}|^2} \quad (2.9)$$

## 2.3 Labeling Method of the Inductor Structures

In the following for designating the inductors special labels are used. Let's explain this by an example. Consider the following label:

1.5\_120\_20\_10

This means that the corresponding inductor has one and a half turns, has an inner diameter of 120  $\mu\text{m}$ , a conductor metal width of 20  $\mu\text{m}$  and a turn-to-turn spacing of 10  $\mu\text{m}$ .

## 2.4 Design Parameters

There are four important parameters affecting the inductors' performance [10]:

### 2.4.1 Inner Diameter

Inner diameter has a significant effect on the quality and the area consumption of the inductor [10].

There is an optimum inner diameter at which the Q-factor attains higher values [10]. This depends on the technology being used. In [10] for example, it was 100  $\mu\text{m}$ . For diameters less than this value, Q will be smaller at the operating frequency. The reason: When the inner diameter is small, the majority of the changing magnetic flux due to the current in outer turns passes through the metal conductor of the inner turns, inducing eddy currents there. These eddy currents end up in increased losses in the inductor, lowering the Q-factor. Increasing the inner diameter causes this changing magnetic flux to pass through the empty area in the middle of the inductor instead, thus decreasing the losses.

As the technology and material were different here, especially that here high resistivity silicon and in [10] low resistivity silicon was used, simulations were necessary to extract this optimum inner diameter. It proved that in ISiT technology this diameter amounts to 120  $\mu\text{m}$ .

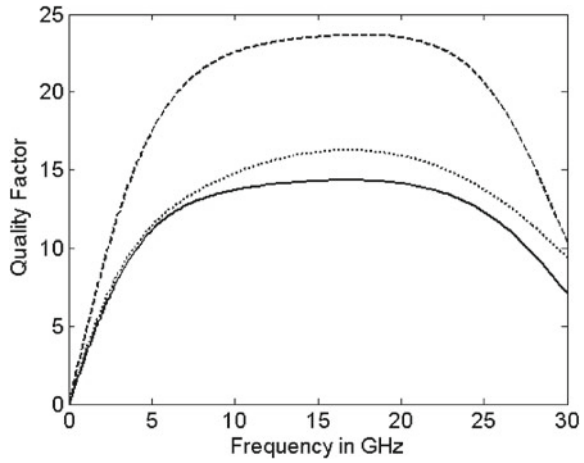
Many simulations were run to verify that 120  $\mu\text{m}$  is the best inner diameter. As an example the results of simulations for several different inductors are shown in Table 2.1. The Q-factor curves for 2\_60\_20\_10, 1.5\_120\_20\_10 and 1.5\_80\_20\_10 are seen in Fig. 2.5. As it is seen in this figure, the Q-factor curve versus frequency increases with increasing inner diameter, so it seems reasonable to increase this parameter up to a value of 120  $\mu\text{m}$  to acquire a better performance for the inductor.

As it is visible in Table 2.1, with increasing the diameter of the spiral inductor up to 120  $\mu\text{m}$ , the Q-factor and the inductance value increase simultaneously. However from 120  $\mu\text{m}$  on, although the inductance increases, Q-factor starts to decrease due to additional parasitic effects and high losses caused by the long length of the conductor. Therefore, from the point of view of both Q-factor and inductance, 120  $\mu\text{m}$  is the optimal inner diameter in ISiT technology. Anyway, other inner diameters are sometimes necessary to achieve various values for the inductance.

**Table 2.1** Comparison between inductors having different inner diameters

Inductor label	Q at 24 GHz	L (nH)	Inner diameter ( $\mu\text{m}$ )
2_60_20_10	12.9	0.69	60
1.5_80_20_10	14.3	0.65	80
1.5_100_20_10	20	0.8	100
1.5_120_20_10	21.6	0.88	120
1.5_140_20_10	15.9	0.99	140

**Fig. 2.5** Q-factor versus frequency for **a** 2\_60\_20\_10: inner diameter 60  $\mu\text{m}$  (*solid line*), **b** 1.5\_80\_20\_10: inner diameter 80  $\mu\text{m}$  (*dotted line*), **c** 1.5\_120\_20\_10: inner diameter 120  $\mu\text{m}$  (*dashed line*), as it is seen here up to a diameter of 120  $\mu\text{m}$ , adding the inner diameter increases the quality factor versus frequency

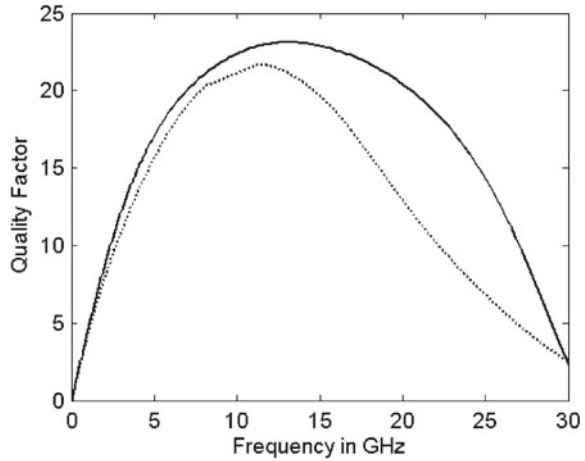


### 2.4.2 Turn-to-Turn Spacing

The metal conductor-to-conductor spacing does not have a major effect on the quality factor [10]. With decreasing spacing, on one hand the inductance increases due to a higher turn-to-turn inductive coupling. However, on the other hand the high frequency resistance also rises due to proximity effects. The quality factor is determined by the resulting inductive and resistive behavior of the inductor. Consequently, in theory, the counter-compensation between the inductance and the resistance results in similar quality factors for inductors having different turn-to-turn spacing. Since minimum spacing leads to least chip area consumption and highest inductance, it seems to be the best option.

The simulations showed that lower spacing, for the same inductance values, provides a better Q-factor behavior. For example in Fig. 2.6, which compares the Q-factor of 1.5\_140\_20\_10 with 1.5\_120\_20\_20 over frequency, although they have the same inductance of 1 nH, the one with smaller spacing has much higher Q values. Other simulations confirmed that always the inductors with lower spacing are superior. Consequently, the lowest spacing was almost always used, with one exception. Among the final inductors, the 0.5 nH inductor at 35 GHz has a larger turn-to-turn spacing of 20  $\mu\text{m}$ , while the others have a spacing of 10  $\mu\text{m}$ . This inductor is very small (geometrically) compared to the others. Concerning the fact that the structures are elevated and as is shown in Fig. 2.4, posts are needed to maintain them in the air, for a very small inductor like this which has a very small inner diameter, the two posts on the two sides of the structure would be quite near to each other. In order to prevent the two posts from causing a large capacitive coupling to each other and to the inductor body, higher spacing was chosen in this case. The posts were consequently farther from each other.

**Fig. 2.6** Q-factor versus frequency for two inductors with equal inductance of 1 nH and with turn-to-turn spacing of **a** 10  $\mu\text{m}$  (*solid line*), **b** 20  $\mu\text{m}$  (*dotted line*), as it is shown here, a smaller spacing results in higher quality factor over frequency



### 2.4.3 Conductor Metal Width

Conductor metal width is at first glance the most complicated parameter of all. A smaller conductor width would mean less substrate and eddy current losses but at the same time higher skin effect losses. From another point of view, more width results in higher turn-to-turn capacitive coupling, and thus higher  $C_S$ . An optimum metal width at which the best compromise between these different effects exists must be determined. The simulations show that here, the best width is the least possible width in the technology (20  $\mu\text{m}$  for the LINES layer), giving highest Q-factor values and resonance frequencies. There were no exceptions here. Attention that these results may only hold for this technology. It is possible that in another technology the least possible metal width is not the optimal metal width, because of for example, too high conductor losses due to a too narrow metal width.

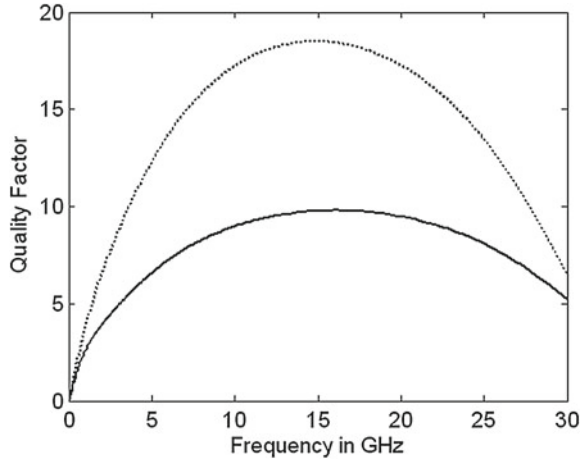
In addition to the above parameters, another important parameter to be considered in the inductor design is the used material:

### 2.4.4 The Material Used

In the ISiT technology there are two metal layers that could be used for building the inductors: thick nickel (SPRING) and gold lines (LINES). The UPATH layer was completely ignored due to its small thickness and high material resistivity. Simulations showed that the inductors made of nickel exhibit much lower Q-factor. Fig. 2.7 illustrates the Q-diagrams of two inductors with equal inductances, one made of nickel and the other made of gold. The inductor made of gold has a much better Q performance. This is due to the higher resistivity of nickel compared to gold. All of



**Fig. 2.7** The Q-factor versus frequency for two inductors with equal inductance made of **a** gold (dotted line) and **b** nickel (solid line), as it can be seen, the gold structure has a much better Q-factor over frequency behavior than the nickel structure



the final inductors, except one, were made of gold. The reason that this one inductor (0.76 nH for 35 GHz) is made of nickel is that the width of nickel metal in the used technology can be made narrower compared to gold (10  $\mu\text{m}$  compared to 20  $\mu\text{m}$ ). So it is possible to make a physically smaller inductor having higher inductance with nickel by using a higher number of turns. Smaller inductor would mean less loss and less parallel shunt capacitance, due to less wiring length. Therefore, higher inductance and Q-factor values were attainable. But generally gold is better.

The above discussions also hold for the 35 GHz frequency, so the same strategy has been used to design the inductors for this frequency. In the following the method used to design the inductors is explained.

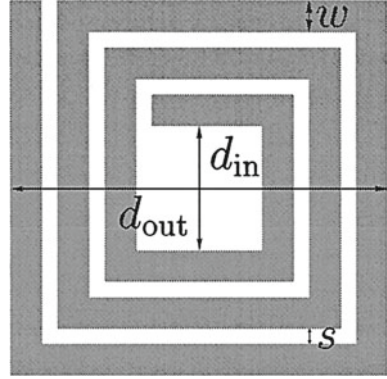
## 2.5 The Strategy for Inductor Library Design

While at lower frequencies (for example tens of MHz) it is relatively easy to attain an inductor design with an adequately large Q factor, at higher frequencies it is a challenge that the final design would feature a large enough (or at least positive) Q, due to the high effect of the parasitic components, especially the inter-turn capacitor  $C_S$ . At tens of MHz frequencies, the design of an inductor for a definite inductance value is possible through the application of the modified Wheeler expression [7]:

$$L_{mw} = K_1 \mu_0 \cdot \frac{n^2 d_{avg}}{1 + K_2 \rho} \quad (2.10)$$

$\mu_0 = 4\pi \times 10^{-7} \frac{\text{H}}{\text{m}}$  is the vacuum permeability and  $n$  is the number of turns.  $d_{avg}$  is the arithmetic mean value of the inner and outer diameters as shown for an square inductor in Fig. 2.8:

**Fig. 2.8** Square inductor topology



$$d_{avg} = \frac{1}{2} \cdot (d_{out} + d_{in}) \quad (2.11)$$

$\rho$  is the fill ratio which is dimensionless and is calculated by:

$$\rho = \frac{d_{out} - d_{in}}{d_{out} + d_{in}} \quad (2.12)$$

$K_1$  and  $K_2$  are layout-dependent coefficients. For square shape  $K_1 = 2.34$  and  $K_2 = 2.75$ .

However, for higher frequencies investigated here it was preferred to focus on increasing the Q factor and decreasing the area. The accurate inductance values were extracted at the end, after the design.

For two key parameters, conductor to conductor spacing and conductor metal width, the values were fixed in the previous section through a large number of simulations. Therefore, only two parameters are remaining: Inner diameter and the number of turns. The number of turns used was 1.5 and 2.5 turns. Integer numbers (like 1 and ) were not used for the number of turns simply because geometries corresponding to 1.5 and 2.5 turns are easier to draw and build.

Using 3.5 turns is not possible according to the simulations. Such an inductor, even with the least possible inner diameter of  $40\mu\text{m}$  (thus being small and having a small parasitic parallel capacitance) would already possess a resonance frequency below 24 GHz.

For the smallest inductor (0.3 nH) a small radius was used. However, this inductor does not have a complete turn, otherwise it becomes too large. The next larger inductor (0.53 nH) has 1.5 turns and a diameter of  $60\mu\text{m}$ . Because having a large inner diameter is advantageous, for the smaller inductors no 2.5 turns has been used, otherwise the inner diameter must be made small to acquire smaller values for the inductance, resulting in bad Q behavior.

As noted above, inner diameters larger than an optimal value will not improve the  $Q$  factor anymore. So for higher inductances, instead of having a very large inner diameter which in turn introduces lots of conductor losses and parasitic capacitances (due to the large size of the structure), another turn is added. The inductance value is proportional to the square of the number of turns, so it grows fast with adding more turns. Generally larger inductance values must have more turns rather than a very large inner diameter.

The largest inductors in 24 and 35 GHz frequencies have 2.5 turns.

## 2.6 Inductor Libraries

Finally two libraries of inductors for 25 and 35 GHz were developed. Pictures of some of these are illustrated later in Chap. 5.

In Table 2.2, the characteristics of the inductors designed for 24 GHz are seen. The label for each structure is visible in the table. Two  $Q$  values are available for each inductor. One is calculated from the accurate “two-port” formula for  $Q$  (Eq. 2.9) and the other is calculated from the common formulation for the  $Q$  (Eq. 2.8) which is more appropriate when the inductor is used as a shunt element.

All these inductors are made of gold. At 24 GHz no nickel was used as the structure material.

In Table 2.3 the characteristics of the inductors designed for 35 GHz are illustrated. The largest inductor has again 2.5 turns and is made of nickel, the only inductor made of nickel in these two libraries. Its value is not much higher than the next inductor in the group which is made of gold but it has a higher  $Q$ .

**Table 2.2** The characteristics of the inductors designed for 24 GHz operation frequency

Inductor label	L (nH)	Q (two port formula)	Q (common formula)
Piece of line	0.3	10.4	19.2
1.5_60_20_10	0.53	11	16.4
1.5_110_20_10	0.85	11.5	15.4
1.5_140_20_10	1	9.5	12
2.5_70_20_10	1.3	4.2	5

**Table 2.3** The characteristics of the inductor library for 35 GHz

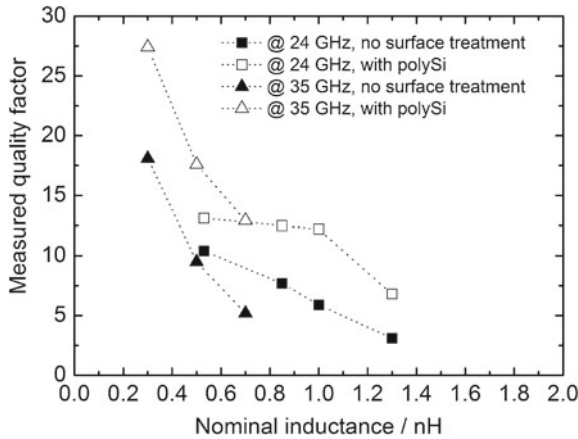
Inductor label	L (nH)	Q (two port formula)	Q (common formula)
Piece of line	0.3	9	18.5
1.5_40_20_20	0.5	8	13
1.5_90_20_10	0.7	4	6.2
2.5_40_10_10	0.76	3	4.3

It is visible in the tables that the  $Q$  values calculated from the formula for the inductor used in the shunt arrangement is always higher than the accurate two port value.

## 2.7 Measurement Results

Some of the designed inductors were fabricated using ISiT and measured for their  $Q$  factors, both with and without inversion channel suppression method. The results are depicted in Fig. 2.9. At 24 GHz, inductors with values of 0.53, 0.85 and 1.3 nH and at 35 GHz, 0.3, 0.5 and 0.7 nH, were measured. As can be seen from the figure, for the two-port formula and especially at 35 GHz, the inductors fabricated on the substrate having deposited poly-silicon feature larger  $Q$  factors than was expected from the simulations (Tables 2.2 and 2.3).

As it is seen in this figure, although the structures are elevated, the interaction between the inductor and the substrate still exists.



**Fig. 2.9** Measured quality factors for the two sets of elevated micromachined spiral inductors, optimized for the 24 and 35 GHz frequencies

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