

## Chapter 2

# On-Chip Protection Solution for Radio Frequency Integrated Circuits in Standard CMOS Process

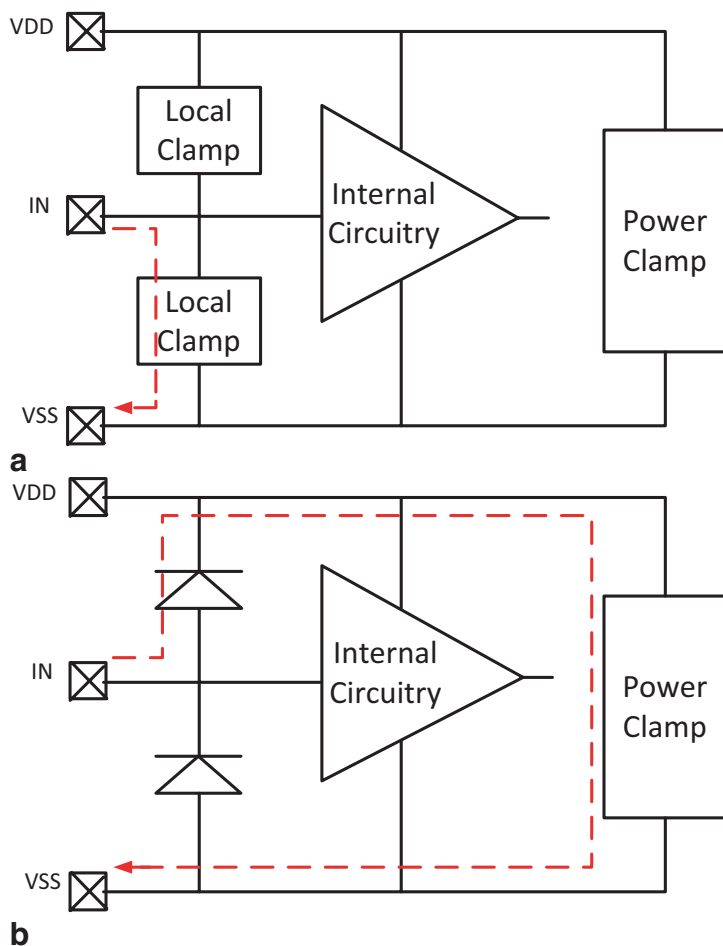
### 2.1 Introduction

Standard CMOS technologies have been increasingly used in RF IC applications mainly due to low manufacture cost and improvement in performance. Achieving sufficient ESD protection for RF and high-speed mixed signal ICs using mainstream CMOS processes imposes a major design and reliability challenge. Ideally ESD protection must be transparent to the protected core circuitry under normal operation conditions. In reality, interaction always exists between the ESD protection structures and the core circuits under protection due to parasitic resistance and capacitance associated with the ESD protection. Such parasitic may be tolerable in IC chips that operate in lower frequency. ESD protection devices for RF applications must hold very low-parasitic capacitance to minimize degradation to RF functionality from poor input/output impedance matching. This requirement poses one of the greatest challenges in RF ESD design, as a low capacitance typically means a small device area and consequently a poor robustness of the ESD-protection device. Other concerns in ESD design for RF ICs include the signal distortion due to the nonlinearity of the parasitic capacitance, the noise coupling as well as noise generation through the ESD protection structures.

In this chapter, various ESD protection options for CMOS RF ICs will be briefly discussed. Then a new SCR-based ESD protection clamp aimed for a very low parasitic capacitance will be presented. This clamp also provides a relatively low-trigger voltage for effectively protecting thin gate oxide as well as a relatively high-holding voltage for latch-up immunity. The capacitance variation across the operation voltage range is small. This linear capacitance is very desirable for RF circuit. The new device can be fabricated in a standard CMOS process without introducing extra processing steps.

## 2.2 ESD Protection Strategy of CMOS RF ICs

In standard CMOS processes, ESD protection circuits can be divided into rail-based clamps and local clamps. The local clamping strategy places clamp structures between I/O pad and supply buses VDD/VSS (Fig. 2.1a) and directly shunt negative and positive stress pulses to the grounded power bus (VDD or VSS). The clamps can exist either between the I/O pad and both the upper and lower supply buses (VDD and VSS) or between the I/O pad and one supply bus (VDD or VSS). The rail-based clamping strategy uses two diodes to connect I/O pad and VDD/VSS (Fig. 2.1b). The diodes operate only in forward biased mode and form ESD protection network along with the power clamp.



**Fig. 2.1** **a** Local clamping ESD protection strategy. **b** Rail-based clamping ESD protection strategy

A simple figure of merit (FOM) may be used to characterize an ESD protection for RF circuits:

$$FOM = Z_{shunt} \cdot V_{HBM} = \frac{V_{HBM}}{\omega C_{ESD}} \quad (2.1)$$

where  $Z_{shunt}$  is the impedance of the shunt path due to the parasitic capacitance of the ESD protection, and  $V_{HBM}$  is the HBM-ESD pass level. A typical tolerance requirement of return loss is 15 db for transmit/receive circuitry, which is corresponding a shunt impedance of 350  $\Omega$  to match a 50  $\Omega$  RF source impedance. The maximum loading capacitance for such requirement is about 200 fF, including the parasitic from bond pad itself, for a frequency as low as 2 GHz. Most RF circuits operate at much higher frequency. Therefore, it is a great challenge to minimize the capacitance of protection devices and improve the FOM.

Snapback-type devices, such as ground gate MOS (ggMOS), gate-coupled MOS (gcMOS), silicon-controlled rectifier (SCR), are the commonly used ESD protection devices as local clamps in CMOS technologies. MOS devices are not suitable for RF ESD protection since they are typically large in size and have significant parasitic capacitance. SCR devices can handle much higher current density than MOS structures. Efficient ESD protection has been achieved with various SCR devices in relatively small area, therefore small parasitic capacitance. Two main concerns in using normal SCRs are high-trigger voltage and latch-up issue due to low-holding voltage. A low-voltage-triggered SCR (LVTSCR) structure uses a MOS transistor as a trigger to lower the trigger voltage. Though there is an additional trigger MOS, LVTSCR ESD devices are more compact than the MOS devices with the same protection levels and can have much smaller parasitic capacitance. However, the capacitance of most SCR structures is still too high for many RF applications.

The approach of diodes with power clamp is by far the most widely used ESD protection strategy. While ESD stress is mainly suppressed by the VDD–VSS power clamp, the parasitic capacitance affecting RF performance is mainly from the two ESD diodes which normally can be smaller than the capacitance in local clamps. A large power clamp can be used without significantly impacting the pad capacitance. Snapback-type clamps may be used as the power clamps. Active clamps with large FET can also be used. In the optimization of the ESD diodes, the diode sizes should be large enough to have small on resistance to shunt the ESD current but small enough to meet the low capacitance requirement for RF applications. Another factor needs to be considered is that the diodes must have short turn-on time. Generally, poly-bounded diodes turn on faster than regular STI-bounded diodes. Though for the same active dimensions, poly-bounded diodes have higher capacitance than STI-bounded diodes, the latter one have better ESD performance and thus have better FOM values. Stacked diodes in series can be used to replace the single diodes in Fig. 2.1b to obtain lower (total) capacitance. The price is the increased voltage drop across the diodes as well as a large silicon area.

The FOM for ggNMOS, LVTSCR, and diode protections of a 90-nm CMOS process was compared in literature [26]. The ratio of FOMs was 12.5 (diode), 2.7 (ggNMOS),

and 5.4 (LVTSCR). It means that the diode solution far better than the ggNMOS and LVTSCR. However, in some RF circuits, the input voltage may swing to higher level than VDD. In such cases, no diode can be placed between the I/O and VDD terminals therefore the rail-based strategy cannot be used. On the other hand, the diode may couple noise from the input to the output through the VDD bus line. As the semiconductor industry moves to more advanced technologies, the bus lines become thinner and longer due to the increased chip size and smaller pitch size. This increases the voltage drop on the bus line and makes the ESD protection less effective, especially in high-current CDM domain. Thus the local clamps can be a more attractive option, even the only option in some cases, for RF ESD protection in CMOS technologies, providing that local clamps with very low capacitance can be developed.

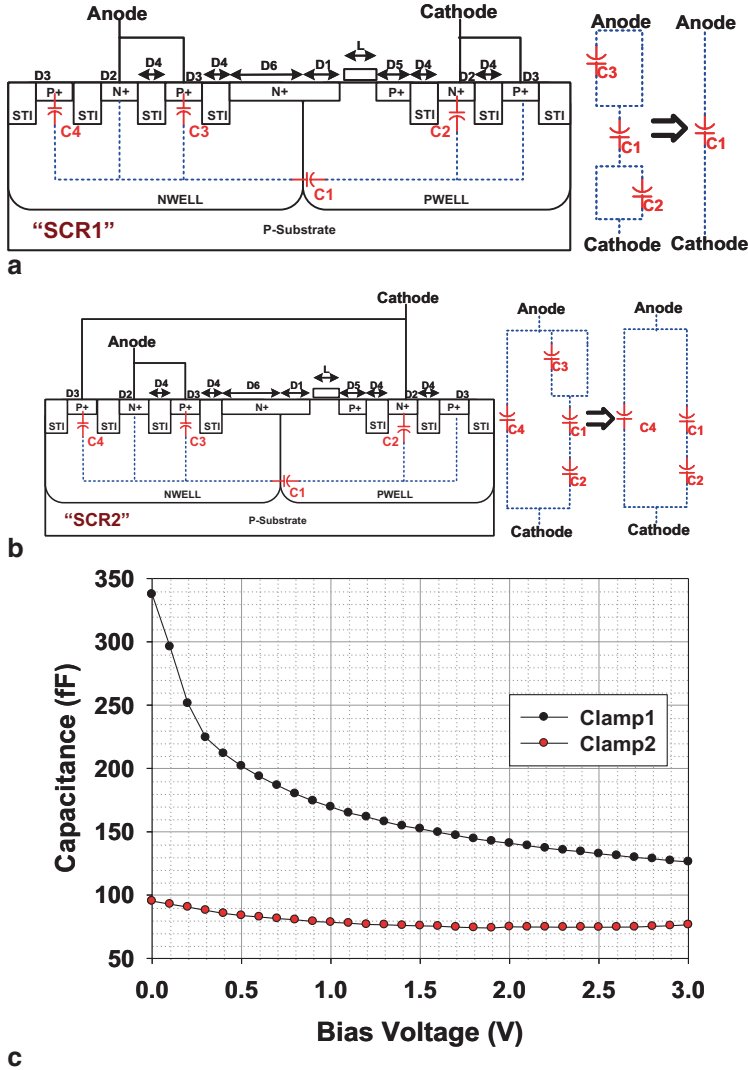
The RF protection design using inductors has been reported in the literature. One configuration uses inductors with power clamp [27]. It is a rail-based clamp in which the diodes are replaced by inductors. It can only have one inductor between the RF I/O pin and VSS and also can have two inductors between the I/O pad and both VDD and VSS. Another configuration combines inductor with capacitor to for a resonator to provide ESD protection [28].

Forward-biased diode chain has traditionally been used as ESD protection structures for RF ICs in CMOS process, as either power clamp or local clamp, because of its relative simple makeup and low-parasitic capacitance [29, 30]. But such a structure can have a large on-state resistance as well as a high leakage current [31]. Significant work has been reported on improving SCR as ESD clamps for RF applications. A polysilicon SCR was reported in [32] for its low capacitance and good ESD robustness. This ESD clamp is considered a better protection solution than the diode chain, but it requires a modification to the polysilicon deposition process which limits its application in the standard CMOS process. An SCR with a waffle layout and small parasitic capacitance was also developed recently [33]. Nevertheless, this structure exhibited a relatively large turn-on time and large trigger voltage (close to 13 V), rendering it unsuitable for ESD protection of low-voltage CMOS applications. In the next section, the development of a new SCR-based ESD protection clamp aimed for a very low parasitic capacitance will be presented.

## 2.3 High-Robustness and Low-Capacitance Silicon-Controlled Rectifier for Radio Frequency Protection

### 2.3.1 Device Structure

Figure 2.2a and b shows the cross-sectional views and equivalent junction capacitances of the conventional low-voltage SCR (Clamp1) and the proposed optimized SCR (Clamp2), respectively. These devices were fabricated in a 0.18- $\mu\text{m}$  CMOS process and have the same layout area of  $50 \times 10 \mu\text{m}^2$ . It is important to note that the



**Fig. 2.2** a Cross section and capacitance equivalent circuit of conventional-like SCR Clamp1. b Cross section and capacitance equivalent circuit of new optimum SCR Clamp2. c Measured capacitances versus anode–cathode voltage of Clamp1 and Clamp2

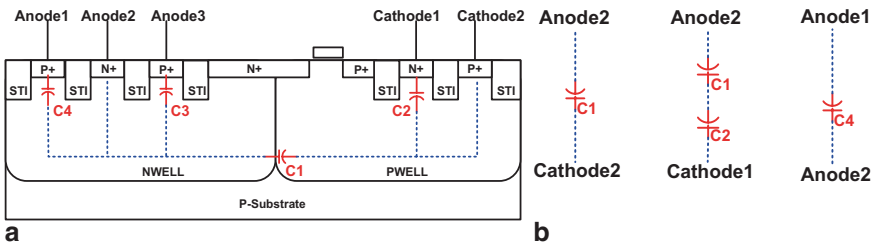
make-up of the two devices is identical, only the cathode terminal connections are different. Instead of connecting the cathode terminal to the P+ region in the P-Well region, as is conventionally done (see Fig. 2.2a), the cathode terminal of the new optimized SCR is connected to the P+ region in the N-Well region (see Fig. 2.2b). Due to this optimum configuration, the total capacitance of Clamp2 is equal to C4 in parallel with C1 in series with C2. On the other hand, the total capacitance in Clamp1 is dominated by C1, since C2 and C3 are shorted.

The aforementioned capacitances are the various junction capacitances imbedded in Clamp1 and Clamp2 shown in Fig. 2.2a and b. Since C1 is the largest among these capacitances due to the large N-Well/P-Well junction area, Clamp2 has a lower capacitance than Clamp1. The capacitances of Clamp1 and Clamp2 at different anode-to-cathode voltages were measured using HP 4284 and are shown in Fig. 2.2c. Notice that the capacitance of Clamp1 is larger than that of Clamp2 by a factor as large as 3.4. The results also show that the capacitance values for both Clamp1 and Clamp2 decrease when the voltage is increased. The trend is consistent with the fact that dominating capacitance C1 associated with the reverse biased N-Well/P-Well junction decreases with the increasing reverse voltage [34]. However, the change of capacitance across the voltage range in Clamp2 is significantly smaller than in Clamp1. This better linearity helps circuit a lot because constant capacitance is much easier to be offset compensated using proper techniques.

### 2.3.2 Measurements and Discussion

In order to analyze in more detail, the overall parasitic capacitances of Clamp1 and Clamp2, the same SCR-based structure but with isolated anode and cathode terminals was fabricated as shown in Fig. 2.3a. To isolate the various capacitances in the device, several isolated terminals (anode1, anode2, anode3, cathode1, and cathode2) were defined in the various N+ and P+ regions. The different pairings of these terminals allowed capturing the difference in capacitances, as illustrated in the equivalent circuits in Fig. 2.3b. For example, anode2–cathode2 pair yields C1. These different capacitances were measured and plotted in Fig. 2.4.

The results confirm the earlier statement that the main blocking junction capacitance C1 is the largest among all these capacitances. The parasitic capacitance of Clamp1 is about the same as the N-Well/P-Well capacitance C1, which is very large (335 fF at zero bias). In contrast, in the optimized Clamp2, the C1 is in series with C2, thus resulting in a small value of C1,2 (34 fF at zero bias). In addition, the capacitance of P+/N-Well junction C4 is also small (60 fF at zero bias) because of the small junction area. Hence the parasitic capacitance of Clamp2 is simply the



**Fig. 2.3** **a** SCR with isolated anode and cathode terminals. **b** Equivalent capacitances for the pairings of anode2–cathode2, anode2–cathode1, and anode1–anode2

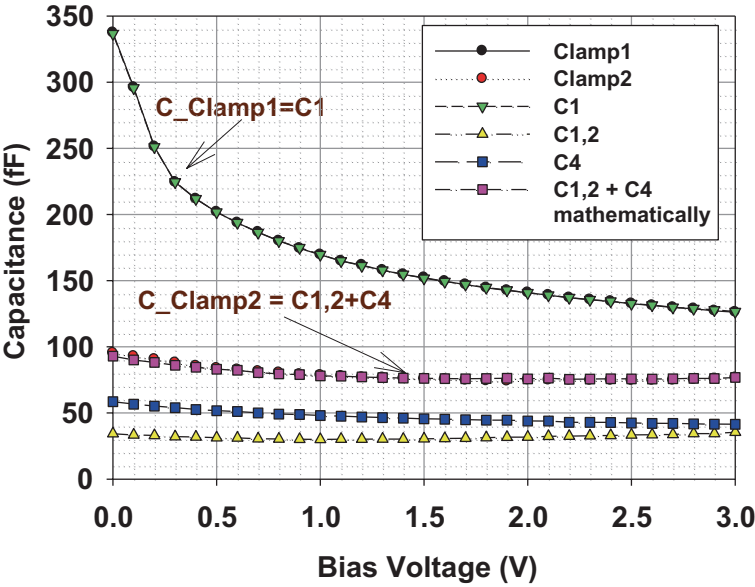
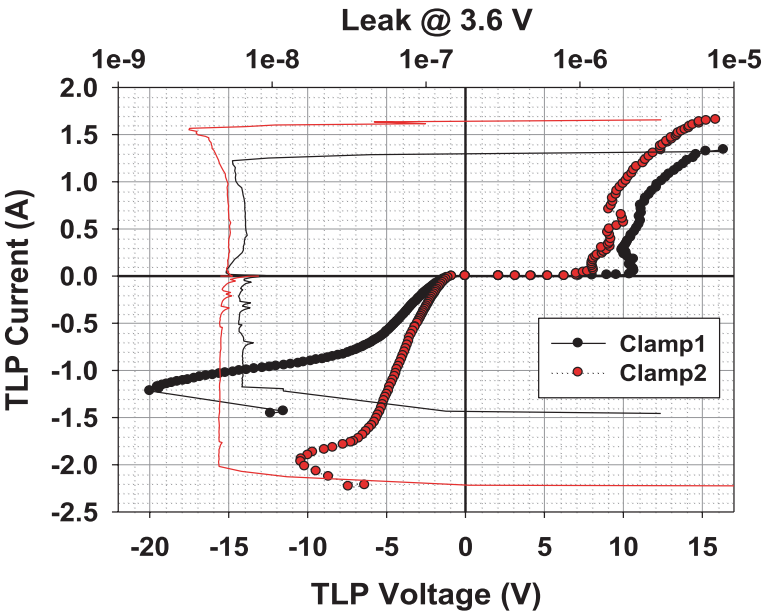


Fig. 2.4 Comparison of capacitances obtained from different anode–cathode connections shown in Fig. 2.3

addition of C4 and C1, 2 (see Fig. 2.4), and Clamp2 exhibits a much lower capacitance than Clamp1 (94 fF versus 335 fF).

To investigate the ESD robustness of Clamp1 and Clamp2 under the human body model (HBM) stress, transmission line-pulsing (TLP) measurements were conducted. Poststress leakage currents were measured at 3.6 V, which is the maximum operating voltage of the technology under consideration. Figure 2.5 shows the measured TLP current (y-axis) versus voltage (bottom x-axis) and leakage current (top x-axis) curves of Clamp1 and Clamp2. In the forward direction, Clamp2 has a smaller trigger voltage and higher failure current than Clamp1 (i.e., 8.1 V in Clamp2 versus 10.5 V in Clamp1 and 1.55 A in Clamp2 versus 1.2 A in Clamp1). These improved features are stemmed from the presence of the floating base of the N-Well/P-Well/N+ transistor in Clamp2. In the reverse direction, Clamp2 also possesses a smaller on-state resistance and higher failure current than Clamp1. This is owing to the different current conducting capabilities of the P-Well/N-Well diode in Clamp1 and the P+/N-Well diode in Clamp2.

Table 2.1 summarizes the characteristics of the two above-mentioned ESD devices (Clamp1 and Clamp2) as well as another low-capacitance clamp (Clamp3) reported previously [35]. Among the three devices, Clamp2 is the best candidate for RF ESD protection because of its all-around excellence in parasitic capacitance, current handling capability, trigger voltage, turn-on time, and voltage overshoot. It should be pointed out that the turn-on time and voltage overshoot were measured using the very-fast TLP and are important parameters for a fast ESD event like the charge device model (CDM). The voltage overshoot is the peak voltage of ESD



**Fig. 2.5** Bidirectional TLP current–voltage characteristics (*red and black closed circles*) and leakage currents (*red and black solid lines*) of Clamp1 and Clamp2

**Table 2.1** Comparison of results of Clamp1, Clamp2, and Clamp3

Parameter	Clamp1	Clamp2	Clamp3 [35]
Device Area ( $\mu\text{m}^2$ )	$50 \times 10$	$50 \times 10$	$45 \times 20$
Failure current-forward (A)	1.2	1.55	1.0
On-state resistance-forward ( $\Omega$ )	5.0	4.5	4.8
Trigger voltage-forward (V)	10.5	8.1	8.5
Failure current-reverse (A)	1.2	2.0	1.5
On-state resistance-reverse ( $\Omega$ )	13.0	2.0	2.5
Turn-on time (ns) @ 1 A	3.2	0.9	2.8
Voltage overshoot (V) @ 1 A	25	12	22
Capacitance @ 0 V bias (fF)	335	94	95

device in its turn-on transient, and the turn-on time is defined as the time from voltage overshoot point to 110% holding voltage point.

The typical capacitance of a ggNMOS for 2 kV HBM protection is about ~500–700 fF. The diode network in a rail-based clamp with the same ESD protection level has a typical capacitance around 100 fF. The failure current of the new clamp is 1.55 A which is equivalent to 2.3 kV HBM failure level. Thus the new clamp provides a desirable local clamp that has a better FOM of RF ESD protection than a typical rail-based diode network clamp.

## 2.4 Summary

In this chapter, various ESD protection options for CMOS RF ICs have been discussed. The local clamping strategy with low-capacitance clamps is a preferred RF ESD protection scheme. A new SCR-based ESD protection clamp device with a very low parasitic capacitance has been proposed and fabricated in a standard CMOS process without introducing extra processing steps. The new ESD structure has been characterized experimentally for the design of effective ESD protection solutions in high-frequency CMOS-based ICs. Such a new device can offer a relatively low-trigger voltage for effectively protecting thin gate oxide and a high-holding voltage for latch-up immunity. It also demonstrated the smallest peak voltage and fastest response time. The device showed a much lower parasitic capacitance, a better capacitance linear, and better ESD performance than the conventional SCR and a low-capacitance SCR reported in the literature. A theoretical analysis was also given to provide the physics underlying the low capacitance observed in the new ESD protection device.

On-Chip Electro-Static Discharge (ESD) Protection for  
Radio-Frequency Integrated Circuits

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